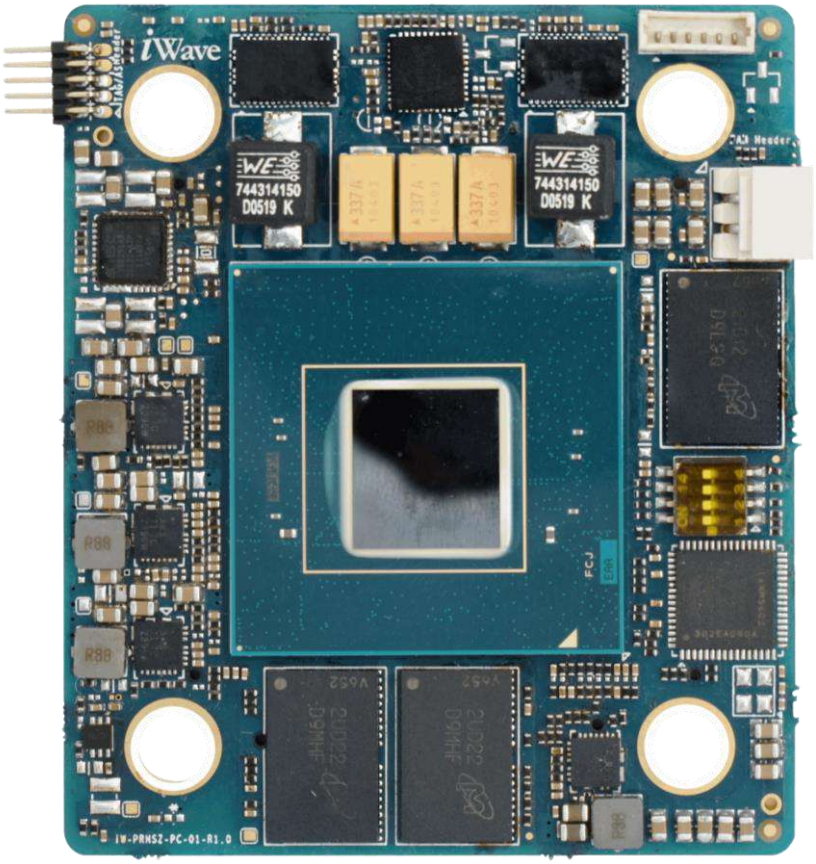
iW-RainboW-G58M
Agilex 5 SoC FPGA (B32A) SOM
Datasheet



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Bangalore, Karnataka,
India – 560076

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1. INTRODUCTION

1.1 Purpose

This document is the datasheet for the Agilex 5 SoC FPGA System on Module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Agilex 5 SoC FPGA System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The Agilex 5 SoC FPGA SOM has a form factor of 60mm x 70mm and provides the functional requirements for an embedded application with integrated Hard Processing System (HPS) and FPGA. Three High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Agilex 5 SoC FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BSP	Board Support Package
B2B	Board to Board Connector
CAN	Controller Area Network
CPU	Central Processing Unit
LPDDR4	Low- Power Double Data Rate
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
HPS	Hard Processing System
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
NPTH	Non-Plated Through hole
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
RX	Receiver
SD	Secure Digital
SDIO	Secure Digital Input Output
SoC	System On Chip
SPI	Serial Peripheral Interface
SOM	System On Module
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Intel® Agilex™ 5 Hard Processor System Technical Reference Manual
- Intel® Agilex™ 5 FPGAs and SoCs Device Data Sheet

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Agilex 5 SoC (B32A) FPGA SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Agilex 5 SoC FPGA (B32A) SOM Block Diagram

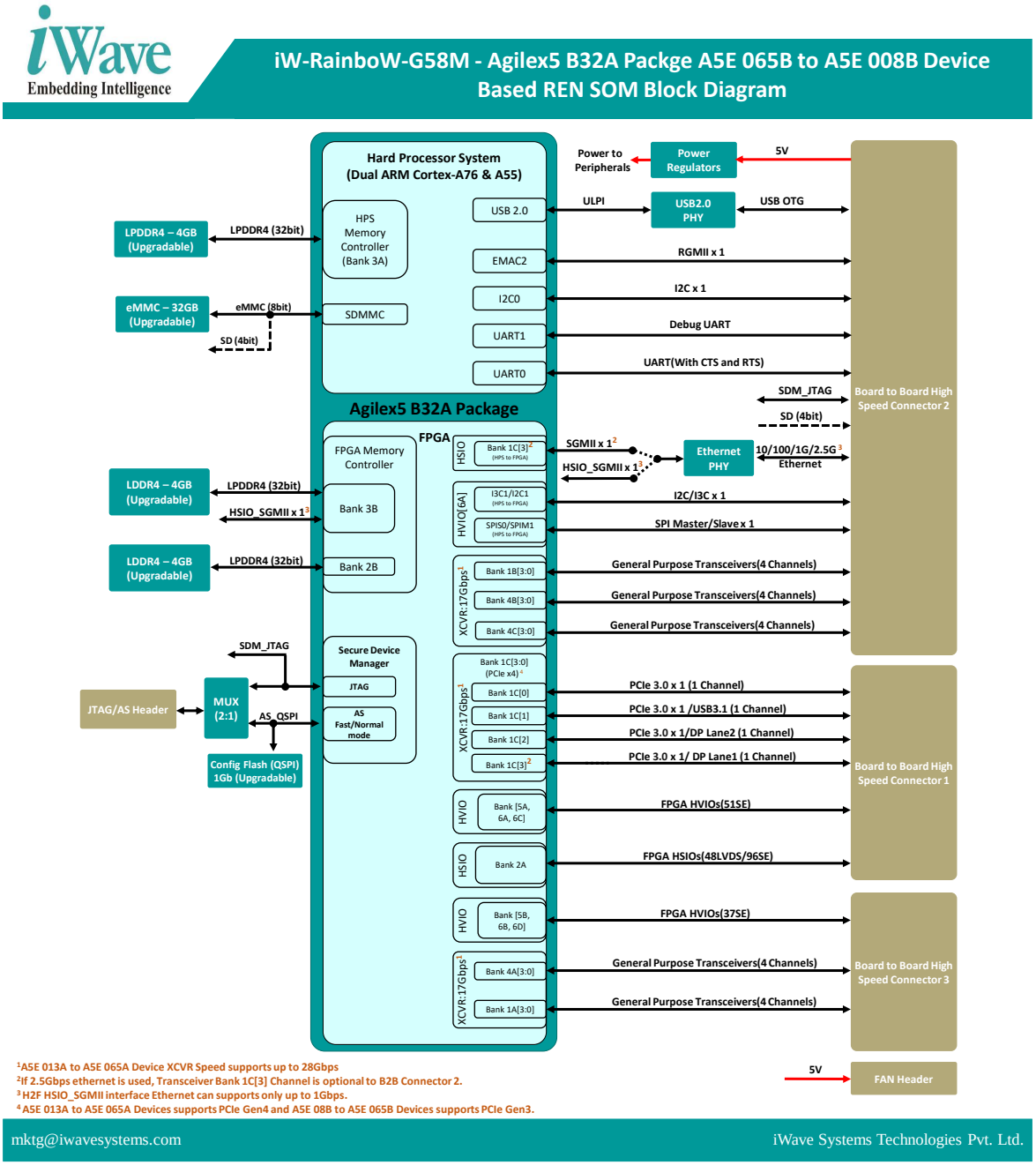

Figure 1: Agilex 5 SoC FPGA (B32A) SOM Block Diagram

2.2 Agilex 5 SoC FPGA SOM Features

The Agilex 5 SoC FPGA SOM supports the following features.

SoC FPGA

- Intel Agilex 5 SoC FPGA E-Series B32A Package Family
  - Group A FPGAs – A5E 065A/052A/043A/028A/013A SoC FPGA
  - Group B FPGAs – A5E 065B/052B/043B/028B/013B/008B SoC FPGA
- Hard Processing System (HPS)
  - Dual core Arm Cortex-A76 up to 1.4 GHz
  - Dual core Arm Cortex-A55 up to 1.25 GHz
- Field Programmable Gate Array (FPGA)
  - Up to 656,080 Logic elements
  - 24 x transceivers up to 28Gbps (17Gbps when using Group B devices)

Power

- Dialog's DA9062 PMIC
- Discrete Regulators

Memory

- 1Gb QSPI Flash (Expandable)[1]
- 32GB eMMC Flash (Expandable)[1]
- 2GB LPDDR4 for HPS (Expandable)[1]
- 2 x 2GB LPDDR4 for FPGA (Expandable)[1]

Clock Generator

- 10 output Clock synthesizer

Other On-SOM Features

- 10/100/1000/2500 Ethernet PHY Transceiver (Qualcomm QCA8081)
- USB2.0 PHY Transceiver
- FAN Header
- JTAG/Active Serial Header (Optional)
- Boot Selection Switch (Optional)

Board to Board Connector1 Interfaces (240pin)

From FPGA Block

- 1C Bank GTS transceivers up to 28Gbps x 4[2,3]
- 48 LVDS/96 Single ended signals from HSIO Bank 2A[4]
- 20 Single ended signals from HVIO Bank 5A[4]
- 20 Single ended signals from HVIO Bank 6C[4]
- 11 Single ended signals from HVIO Bank 6A
- Synchronous Clock In/Out
- 10MHz Reference Clock Input (Optional)

Board to Board Connector2 Interfaces (240pin)

From HPS/SDM Block

- USB2.0 OTG x 1 Port (through On-SOM USB2.0 PHY Transceiver)
- RGMII Interface x 1 Port
- Debug UART x 1 Port
- Data UART x 1 Port (With Flow Control)
- I2C x 1 Port
- JTAG x 1 Port
- Active Serial x 1 Port (Optional)
- SD1 (4bit) x1 Port (Optional)[5]

From HPS to FPGA Block

- Up to 2.5G Ethernet x 1 (through On-SOM Ethernet PHY) [6]
- USB3.0 x 1 Port
- I2C x 1 Port
- SPI x 1 Port (With 2 x Chip select)

From FPGA Block

- 10/100/1000/2500 Ethernet x 1 Port (through On-SOM Ethernet PHY transceiver)
- 1B Bank GTS transceivers up to 28Gbps x 4[3]
- 4B Bank GTS transceivers up to 28Gbps x 4[3]
- 4C Bank GTS transceivers up to 28Gbps x 4[3]

Board to Board Connector3 Interfaces (160pin)

From FPGA Block

- 4A Bank GTS transceivers up to 28Gbps x 4[3]
- 1A Bank GTS transceivers up to 28Gbps x 4[3]
- 16 Single ended signals from HVIO Bank 5B
- 20 Single ended signals from HVIO Bank 6D[4]
- 1 Single ended signal from HVIO Bank 6B

General Specification

- Power Supply : 5V (from Board-to-Board Connector2)
- Form Factor : 60mm x 70mm.

Note:

[1] The Expansion of LPDDR4, QSPI Flash and eMMC size/capacity are subject to availability of chips in market.

[2] By default Channel3 of GTS Transceiver Bank 1C is used for On-SOM Ethernet Transceiver and can be support on the Board-to-Board Connector when the On SOM Ethernet PHY transceiver is not used.

[3] In Agilex 5 SoC FPGA SOM, the maximum transceiver speed of 28Gbps can be achieved only when Group A devices are used. When Group B devices are used, the maximum speed is 17Gbps.

[4] In Agilex 5 SoC FPGA SOM, these BANKs support variable IO voltage setting which is configurable through software.

[5] 4-bit SDMMC optionally supported on Board-to-Board Connector -2 is muxed with On SOM eMMC. By default, on SOM eMMC is supported.

[6] On-SOM Ethernet PHY is connected to HPS MAC through FPGA serdes for SGMII interface.

2.3 Agilex 5 SoC FPGA

The Intel Agilex® 5 FPGA product family extends the innovations of the Intel Agilex FPGA portfolio to midrange FPGA applications. The Intel Agilex 5 FPGAs and SoCs serve a broad range of applications that require high performance, lower power consumption, smaller form factor, and lower logic densities.

- First enhanced DSP with AI Tensor block in the industry—delivers high-efficiency artificial intelligence (AI) and digital signal processing (DSP)
- First asymmetric applications processor system in the FPGA industry—a combination of a dual-core Arm* Cortex*-A76 and a dual-core Arm Cortex-A55 processors enables you to optimize the performance and power efficiency of processing workloads.
- Monolithic die architecture—provides higher system integration and lower power with smaller form factor packages.
- Advanced connectivity features:
    - ❖ High-speed GTS transceivers up to 28.1 Gbps
    - ❖ PCI Express* (PCIe*) 4.0 ×8 support
    - ❖ General purpose I/Os supporting voltages from 1.0 V to 3.3 V

The Intel Agilex 5 FPGA product family delivers on average 50% higher fabric performance and up to 42% lower total power consumption compared to previous generation Intel® FPGAs. To achieve this improvement, the product family leverages these key innovations and techniques:

- Advanced Intel 7 technology
- Second generation Intel Hyperflex® FPGA architecture
- High level of system integration
- SmartVID and fixed low core voltage device options
- Power islands, power gating, and other power reduction techniques

These capabilities and advanced features make the Intel Agilex 5 FPGA product family ideal for midrange FPGA applications across the edge and core. The applications span across many segments including wireless and wireline communications, video and broadcast equipment, industrial, test and measurement, medical electronics, data centres, and defence.

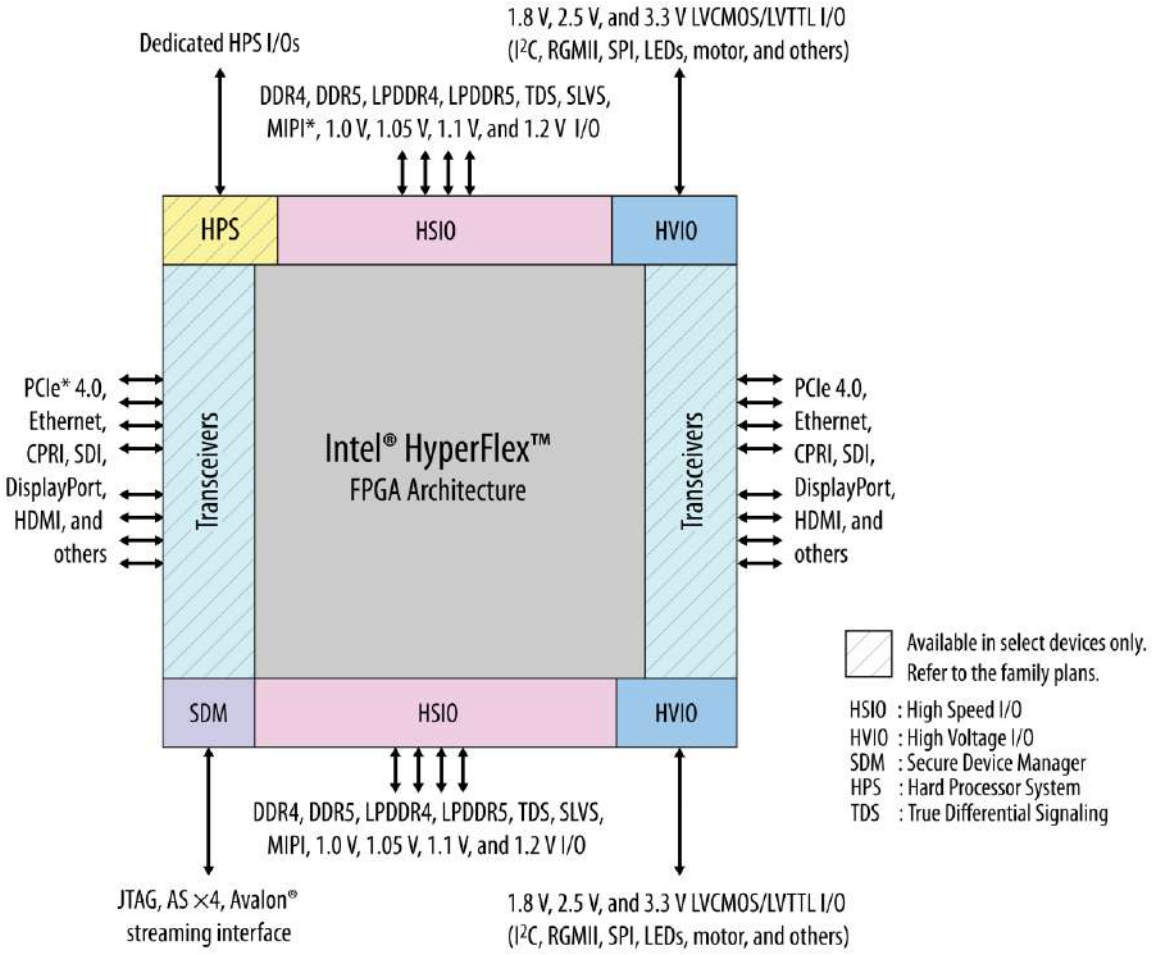

Figure 1: Agilex 5 FPGAs and SoCs Block Diagram

Note: Please refer the latest Agilex 5 Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Agilex 5 SOM is compatible for E-Series Group A FPGAs – A5E 065A/052A/043A/028A/013A SoC FPGA and Group B FPGAs – A5E 065B/052B/043B/028B/013B/008B devices coming in B32A Package. This B32A pin package is a 32mm x 32mm package with 0.65mm ball pitch. The feature Comparison for these devices is given below:

Features	E Series Device Group A Devices					E Series Device Group B Devices					
	A5E 013A	A5E 028A	A5E 043A	A5E 052A	A5E 065A	A5E 008B	A5E 013B	A5E 028B	A5E 043B	A5E 052B	A5E 065B
Process technology	Intel 7										
Architecture	Monolithic die										
Packaging	VPBGA package with minimum ball pitch of 0.65 mm for smaller form factor and to help reduce the number of PCB layers										
Core fabric	Second generation Intel Hyperflex core fabric										
On-chip RAM	38Mb										
Logic elements (LEs)	138,060	282,256	434,240	523,920	656,080	85,196	138,060	282,256	434,240	523,920	656,080
Adaptive logic modules (ALMs)	46,800	95,680	147,200	177,600	222,400	28,880	46,800	95,680	147,200	177,600	222,400
ALM registers	187,200	382,720	588,800	710,400	889,600	115,520	187,200	382,720	588,800	710,400	889,600
M20K memory blocks	358	716	1,050	1,288	1,611	229	358	716	1,050	1,288	1,611
M20K memory size (Mb)	6.99	13.98	20.51	25.16	31.46	4.47	6.99	13.98	20.51	25.16	31.46
MLAB memory count	2,340	4,784	6,720	8,440	11,120	1,780	2,340	4,784	6,720	8,440	11,120
MLAB memory size (Mb)	1.43	2.92	4.10	5.15	6.79	1.09	1.43	2.92	4.10	5.13	6.79
I/O PLL	4	4	8	8	8	4	4	4	8	8	8
Fabric-feeding I/O PLL[1]	8	10	13	13	13	8	8	10	13	13	13
Variable-precision DSP blocks	188	376	564	676	846	116	188	376	564	676	846
18 x 19 multipliers	376	752	1,128	1,352	1,692	232	376	752	1,128	1,352	1,692
Peak INT8 (TOPS)	5.78	11.55	17.33	20.78	25.99	3.05	4.93	9.85	14.78	17.72	22.17
LVDS pairs at 1.6 Gbps	96	96	192	192	192	96	96	96	192	192	192
DDR4/5 and LPDDR4/5 interfaces (x32)	2	2	4	4	4	2	2	2	4	4	4

Features	E Series Device Group A Devices					E Series Device Group B Devices					
	A5E 013A	A5E 028A	A5E 043A	A5E 052A	A5E 065A	A5E 008B	A5E 013B	A5E 028B	A5E 043B	A5E 052B	A5E 065B
MIPI D-PHY interface	14	14	28	28	28	14	14	14	28	28	28
Differential (RX or TX) pairs at 28 Gbps	4	12	16	24	24	4	4	12	16	24	24
PCIe 4.0 x4 instance	1	3	4	6	6	1	1	3	4	6	6
High-speed I/O (HSIO)	192	192	384	384	384	192	192	192	384	384	384
High-voltage I/O (HVIO)	200	200	120	120	120	200	200	200	120	120	120
Secure device manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support										
Hard processor system	Multi-core with 32-bit/64-bit dual-core Arm Cortex*-A55 up to 1.5 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.8 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2.										
Transceiver	PCI Express* (PCIe*) hard IP up to PCIe 4.0 x4 EP and RP Transceiver channel count: up to 24 channels at **28 Gbps (NRZ)** Ethernet IP: up to 6 x10/25 GbE hard IP (MAC, PCS, and FEC)					PCIe hard IP up to PCIe 4.0 x4 EP and RP Transceiver channel count: up to 24 channels at **17 Gbps (NRZ)** Ethernet IP: up to 6 x10 GbE hard IP (MAC, PCS, and FEC)					

2.3.1 SoC Power

The Agilex 5 SOM uses discrete power regulators along with one DA9062 PMIC from Dialog Semiconductor for SoC power management. In Intel Agilex 5 SoC FPGA SOM, Core power, Periphery circuitry power (VCC and VCCP) is connected to a SmartVID regulator, where the voltage can be varied between 0.70V – 0.90V based on Temperature & Performance. The HPS I/O voltage (VCCIO_HPS) is fixed to 1.8V. The I/O voltage details of each FPGA Bank & High-speed transceiver will be mentioned in the corresponding sections.

2.3.2 SoC Reset

The Intel Agilex 5 SoC FPGA SOM POR is taken care internally by SDM Block in device. Also, it supports warm reset input from Board-to-Board Connector2 pin B11 and connected to pin BW102, HPS_COLD_nRESET pin of the SDM Bank of the device.

2.3.3 Intel Agilex 5 SoC and FPGA Configuration & Status

The Intel Agilex 5 SoC and FPGA uses multi-stage boot process that supports both a non-secure and a secure boot. It supports different configuration schemes -JTAG-based configuration, AS Fast or Standard POR configuration. These configuration schemes are selected using the MSEL pin setting.

The SDM is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the First stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the HPS first and then configure the FPGA or it can be set to configure the FPGA first, then boot the HPS.

The Intel Agilex 5 SoC and FPGA SOM supports LED for the FPGA Configuration status indication namely CONFIG_DONE. LED interfaced to CONFIG_DONE and it is asserted when the FPGA configuration is complete. It is used to indicate if the FPGA is configured or not.

2.3.4 Agilex 5 Boot Mode Configuration

The Intel Agilex 5 SoC and FPGA always boots from SDM first and then boots the HPS or FPGA. Intel Agilex 5 SoC and FPGA supports the SDM QSPI or JTAG as the First Stage Bootloader in Standard or Fast Mode. Upon device reset, Intel Agilex 5 SoC and FPGA MSEL pins are read to determine the primary boot device. The optional On SOM Switch or by setting the MSEL pins Low or Floating as per the booting requirements given in below table supports to switch between the boot devices. When the optional JTAG/AS Header on SOM along with the optional on-board Switch is used, we can switch between AS or JTAG on the header.

By default, the JTAG and AS signals are made available on the Board-to-Board Connector -2. By making use of the MSEL bits Low or Floating in the Carrier Board, we can select the desired boot mode.

Note: The MSEL Pins are pulled up to 1.8V on SOM. So, these signals should be either left floating or made low in Carrier Card.

Table 3: Boot Mode Switch Truth Table

Intel Agilex 5 Configuration Scheme Selection	SW (4 Position Switch-POS1 &POS2)		
	B2B-2 Pin D14	B2B-2 Pin D13	B2B-2 Pin D12
	MSEL2	MSEL1	MSEL0
Active Serial - Fast Mode	Low	Low	Floating
Active Serial - Standard Mode	Low	Floating	Floating
JTAG Only	Floating	Floating	Floating

2.3.5 Clock Design

2.3.5.1 Clock Synthesizer

The Agilex 5 SOM supports on-Board 10-Bit Clock Synthesizer “SI5341B-D-GM” from Skyworks Solution. This clock synthesizer provides all clock source for whole SOM & other peripheral to make the system completely synchronized. These reference clock details are mentioned in the below table.

Table 4: Clock Synthesizer Input & Output

Sl. No	Clock Synthesizer In/Out	Frequency	Net Name	SoC Pin No	Signal Type/ Termination	Description
Input Reference Clock Options to Clock Synthesizer						
1	IN0/ IN0b	100 MHz	MSIO/SYS_SYNC_CLK_INP/MSIO/SYS_SYNC_CLK_INN	NA	1.8V, LVDS	External clock input from A15, A16th pin of B2B1 (optional)
2	IN1	10 MHz	10MHZ_REFCLK_IN	NA	1.8V, LVCMOS	External clock input from A12th pin of B2B1 (Optional)
3	XA/XB	48 MHz	CLK_GEN_XA/CLK_GEN_XB	NA	-	External Crystal input
Output Clock from Clock Synthesizer						
1	OUT0/ OUT0b	100MHz	MSIO/SYS_SYNC_CLK_OUTp/ MSIO/SYS_SYNC_CLK_OUTn	NA	1.8V, LVDS	Clock output though A31 & A32 pin of B2B1
2	OUT1	100MHz	FPGA_REFP_CLK_100MHz	BK31	1.8V, LVCMOS	Connected to HVIO Bank 6A IO9 as FPGA reference clock
3	OUT2	50MHz	ETH_CLK_50MHz	NA	1.8V, LVCMOS	Clock input for the On SOM Ethernet PHY.
4	OUT3	24MHz	USB2.0_TRANSCEIVER_CLK_24M	NA	1.8V, LVCMOS	Clock input for the USB2.0 Transceiver PHY
5	OUT4/ OUT4b	100MHz	SGMII_TXVR_REFCLK3P/ SGMII_TXVR_REFCLK3N	AP120/ AP115	1.8V, LVDS	Reference Clock input for Transceiver bank 1C- mainly for the on SOM Ethernet.
6	OUT5	25MHz	HPS_OSC_CLK_25MHz	T132	1.8V, LVCMOS	HPS Reference clock input
7	OUT6	125MHz	SDM_OSC_CLK_125MHz	BR102	1.8V, LVCMOS	SDM Reference clock input
8	OUT7/ OUT7b	199.95MHz	HPS_LPDDR4_CLKREFp/ HPS_LPDDR4_CLKREFn	M105/ K105	1.8V, LVDS	HPS LPDDR4 reference clock input
9	OUT8/ OUT8b	199.95MHz	FPGA1_LPDDR4_CLKREFp/ FPGA1_LPDDR4_CLKREFn	T65/ P65	1.8V, LVDS	FPGA LPDDR4 -1 reference clock input
10	OUT9/ OUT9b	199.95MHz	FPGA2_LPDDR4_CLKREFp/ FPGA2_LPDDR4_CLKREFn	CH38/ CF38	1.8V, LVDS	FPGA LPDDR4 -2 reference clock input

2.3.6 Agilex 5 SOM PMIC

The Agilex 5 SOM supports a Dialog semiconductor DA9062 PMIC for providing the IO power for the SoC FPGA.

2.3.6.1 DA9062 PMIC Regulator with RTC

The HPS I2C0 module of Agilex 5 SOM is used for the PMIC through HPS pins with I2C address 0x48.

PMIC's BUCK 1 & 2 are used in dual phase and is used for providing the VCCRCORE Power for the SoC FPGA. This is a fixed voltage and is set to 1.2V.

PMIC Buck 3 is used for powering the HSIO bank 2A. The IOs of this bank are made available on Board-to-Board Connector 1. This voltage is set to 1.2V during powerup. It can be also set to 1.05V or 1.1V voltage level through I2C during the bootup.

PMIC Buck 4 is used for powering the HVIO banks 6A and 6B. The voltage level of this bank is fixed to 1.8V and should not be changed to any other level.

PMIC LDO1 is unused and the LDO2 is used for powering the HVIO bank 5A. This bank IOs are available on the Board-to-Board Connectors. By default, the voltage is set to 1.8V. It can be set to any other supported voltage level through I2C during the bootup.

Similarly, LDO3 is used for powering the HVIO bank 6C. This bank IOs are available on the Board-to-Board Connectors. By default, the voltage is set to 1.8V. It can be set to any other supported voltage level through I2C during the bootup.

PMIC LDO4 is used for powering the HVIO banks 5B & 6D. This bank IOs are available on the Board-to-Board Connectors. By default, the voltage is set to 1.8V. It can be also set to 1.25V or 3.3V supported voltage level through I2C during the bootup.

The PMIC also supports Real Time Clock functionality. It uses the Coin cell battery power from D9 pin of Board-to-Board Connector2 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

Important Note: Every Power Off and On, The DA9062 PMIC work as initial OTP Setting

2.3.7 SOM Memory

2.3.7.1 LPDDR4 SDRAM

The Agilex 5 SOM supports 1 x 32bit, 2GB LPDDR4 RAM memory for HPS and 2 x 32bit, 2GB LPDDR4 RAM memory for FPGA. This can support a maximum of 6GB LPDDR4 memory on SOM. It is possible to increase the DRAM density on board by changing the chips to ones with higher density by the maximum density support will be dependent on the chip availability. These LPDDR4 devices operates at 2400MT/s data rate. Agilex 5 HSIO banks 3A, 3B and 2B are used for the LPDDR4 interface. Of these the HSIO bank 3A is connected to the HPS LPDDR4 memory and 3B and 2A are connected to the FPGA LPDDR4 memory 1 and 2 respectively.

The Agilex 5 SOM supports 199.95MHz LVDS clock from Clock synthesizer to the respective banks for LPDDR4 bank reference clock inputs. Refer the Clock section for more details.

2.3.7.2 QSPI Flash

The Intel Agilex 5 SoC and FPGA SOM supports 1Gb QSPI Flash memory for First Stage Boot & Storage. This QSPI Flash memory is directly connected to the SDM controller of the Intel Agilex 5 SoC and FPGA SDM bank and operates at 1.8V Voltage level. The QSPI Flash size can be expandable based on the availability of higher density chips.

Note: Refer Ordering Information *section for exact QSPI Flash size used on the SOM based on the Product Part Number.*

2.3.7.3 eMMC Flash

The Intel Agilex 5 SoC and FPGA SOM supports 32GB eMMC Flash memory for Second Stage Boot & Storage. This eMMC Flash memory is directly connected to the SDMMC controller in HPS Block of the Intel Agilex 5 SoC and FPGA and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC5.1 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

Note: Refer Ordering Information *section for exact QSPI Flash size used on the SOM based on the Product Part Number.*

2.4 On SOM Features

2.4.1 Fan Header

The Intel Agilex 5 SoC and FPGA SOM supports a Fan Header (J3) to connect cooling Fan if required. The Fan Header (J3) is physically located on topside of the SOM as shown below.

Number of Pins - 2

Connector Part - 52125-02-0200-01 from CNC

Mating Connector - 52225-02 from CNC

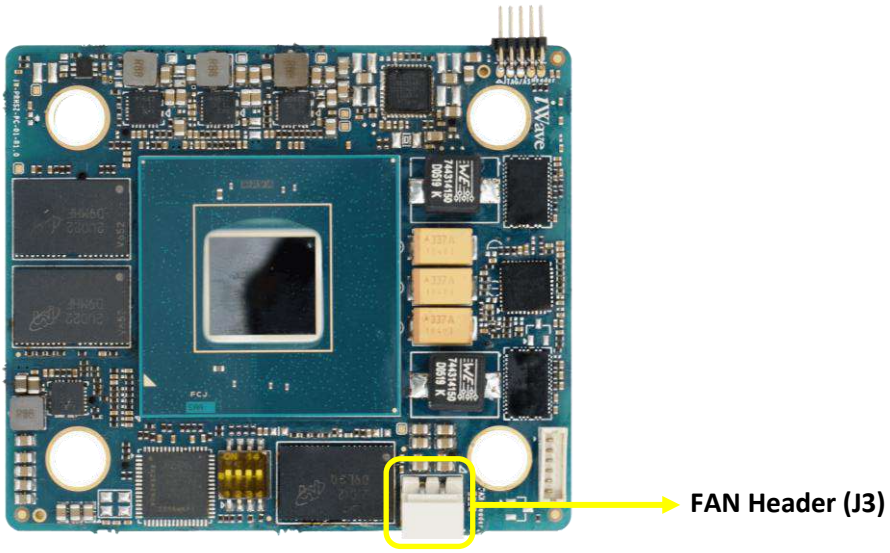

Figure 2: Fan Header

Table 5: Fan Header Pinout

Pin No	Signal Name	Pin Name	Bank No.	Pin No	Signal Type/ Termination	Description
1	VCC_5V	-	-	-	O, 5V Power	Supply Voltage.
2	GND	-	-	-	Power	Ground.

2.4.2 JTAG/ Active Serial Header (Optional)

The Intel Agilex 5 SoC and FPGA SOM supports 10Pin JTAG/Active Serial Header for JTAG or Active Serial interface. JTAG Interface Signals and Active Serial Signals from the SDM of Intel Agilex 5 SoC and FPGA is connected to the 10pin Header through a MUX switch. JTAG and Active Serial can be selected by toggling the POS4 of the option dip switch DIP Switch on SOM. The Intel Agilex 5 SoC and FPGA 's HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Intel Agilex 5 SoC and FPGA. These JTAG interface signals are at 1.8V Voltage level. The JTAG signals are made available for use on the Carrier Card through Board-to-Board Connector 2. Likewise, the Active serial signals are also made optionally available on the Board-to-Board Connector.

The JTAG/Active Serial Header is physically located on topside of the SOM. Custom cabling is needed for connecting the USB Blaster Programming Cable to this JTAG Header.

Number of Pins - 10

Connector Part - GRPB052MWCN-RC from Sullins Connector Solutions

Table 6: JTAG/Active Serial Header Pinout- JTAG is selected

Pin No	Signal Name	Signal Type/ Termination	Description
1	JTAG_TCK	I, 1.8V CMOS	JTAG test Clock.
2	GND	Power	Ground.
3	JTAG_TDO	O, 1.8V CMOS	JTAG test data output.
4	VCC(TRGT)	Power	Target Power Supply
5	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
6	JTAG_RESET	I, 1.8V CMOS /10K PU	JTAG RESET. Not connected to SoC or FPGA
7	NC	-	NC.
8	NC	-	NC.
9	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
10	GND	Power	Ground.

Table 7: JTAG/Active Serial Header Pinout- Active Serial is selected.

Pin No	Signal Name	Signal Type/ Termination	Description
1	AS_CLK	I, 1.8V CMOS/10K PD	Dedicated Serial clock to configure flash.
2	GND	Power	Ground.
3	AS_CONF_DONE	IO, 1.8V OD	Configuration status IO to Intel Agilex 5 SoC and FPGA.
4	VCC(TRGT)	Power	Target Power Supply
5	AS_nCONFIG	I, 1.8V CMOS/10K PU	Configuration input to Intel Agilex 5 SoC and FPGA
6	nCE	I, 1.8V CMOS/10K PU	Chip Enable input to Intel Agilex 5 SoC and FPGA
7	AS_DO	I, 1.8V CMOS	Serial Data input to Configuration flash
8	AS_CS0	I, 1.8V CMOS/10K PU	Chip select input to configuration flash.
9	AS_DI	O, 1.8V CMOS	Serial Data output from configuration flash.
10	GND	Power	Ground.

The Agilex 5 SOM supports two 240 pin and one 160pin high speed ruggedized terminal strip connectors for interfaces expansion. All the effort is made in Agilex 5 SOM design to provide the maximum interfaces of Agilex 5 SoC FPGA to the carrier board by adding these three Board to Board Connectors.

2.5 Board to Board Connector1

The Agilex 5 SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J6) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A-TR from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A-TR from Samtech

Staking Height - 5mm

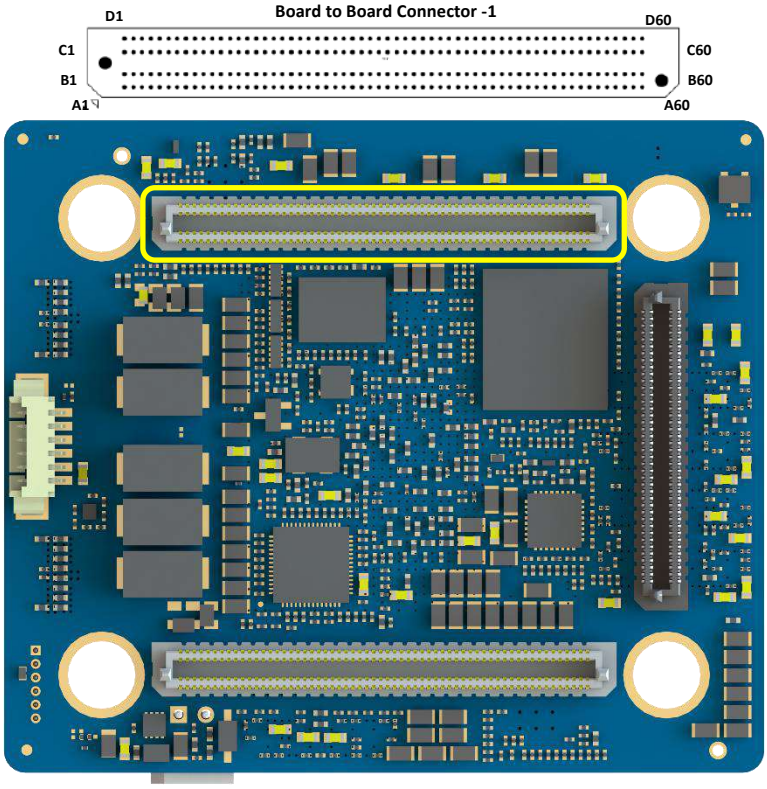

Figure 3: Board to Board Connector 1

Table 8: Board to Board Connector1 Pinout

B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name
A1	VCC_1V8_G3	B1	VIO_BANK2	C1	VCC_1V2_G3_IO	D1	VCC_1V2_G3_IO
A2	FPGA_BW69_LVDS2A_T_10P_IO76	B2	FPGA_CW59_LVDS2A_T_7P_IO82	C2	FPGA_CH69_LVDS2A_T_4P_IO88	D2	FPGA_CF59_LVDS2A_T_1P_IO94
A3	FPGA_CA69_LVDS2A_T_10N_IO77	B3	FPGA_CA59_LVDS2A_T_7N_IO83	C3	FPGA_CF69_LVDS2A_T_4N_IO89	D3	FPGA_CH59_LVDS2A_T_1N_IO95
A4	FPGA_BR71_LVDS2A_T_11P_IO74	B4	FPGA_BU59_LVDS2A_T_8P_IO80	C4	FPGA_CC71_LVDS2A_T_5P_IO86	D4	FPGA_CF62_LVDS2A_T_2P_IO92
A5	FPGA_BU71_LVDS2A_T_11N_IO75	B5	FPGA_BR59_LVDS2A_T_8N_IO81	C5	FPGA_CA71_LVDS2A_T_5N_IO87	D5	FPGA_CH62_LVDS2A_T_2N_IO93
A6	FPGA_BR69_LVDS2A_T_12P_IO72	B6	FPGA_BU62_LVDS2A_T_9P_IO78	C6	FPGA_CF71_LVDS2A_T_6P_IO84	D6	FPGA_CA62_LVDS2A_T_3P_IO90
A7	FPGA_BU69_LVDS2A_T_12N_IO73	B7	FPGA_BR62_LVDS2A_T_9N_IO79	C7	FPGA_CH71_LVDS2A_T_6N_IO85	D7	FPGA_CC62_LVDS2A_T_3N_IO91
A8	GND	B8	GND	C8	GND	D8	GND
A9	FPGA_BF86_LVDS2A_T_22P_IO52	B9	FPGA_BH69_LVDS2A_T_17P_IO62	C9	FPGA_BH62_LVDS2A_T_14P_IO68	D9	FPGA_BF75_LVDS2A_T_19P_IO58/CLKIN_0P
A10	FPGA_BE86_LVDS2A_T_22N_IO53	B10	FPGA_BH71_LVDS2A_T_17N_IO63	C10	FPGA_BH59_LVDS2A_T_14N_IO69	D10	FPGA_BF72_LVDS2A_T_19N_IO59/CLKIN_0N
A11	FPGA_BF93_LVDS2A_T_23P_IO50	B11	FPGA_BE79_LVDS2A_T_20P_IO56	C11	FPGA_BM62_LVDS2A_T_15P_IO66	D11	FPGA_BM71_LVDS2A_T_18P_IO60/CLKIN_1P
A12	B2B_A12	B12	FPGA_BE75_LVDS2A_T_20N_IO57	C12	FPGA_BP62_LVDS2A_T_15N_IO67	D12	FPGA_BP71_LVDS2A_T_18N_IO61/CLKIN_1N
A13	FPGA_BE96_LVDS2A_T_24P_IO48	B13	FPGA_BE83_LVDS2A_T_21P_IO54/CLKOUT_0P	C13	FPGA_BM69_LVDS2A_T_16P_IO64/CLKOUT_1P	D13	FPGA_BM59_LVDS2A_T_13P_IO70
A14	FPGA_BE93_LVDS2A_T_24N_IO49	B14	FPGA_BF83_LVDS2A_T_21N_IO55/CLKOUT_0N	C14	FPGA_BK69_LVDS2A_T_16N_IO65/CLKOUT_1N	D14	FPGA_BK59_LVDS2A_T_13N_IO71
A15	MSIO/SYS_SYNC_CLK_INP	B15	NC	C15	NC	D15	NC
A16	MSIO/SYS_SYNC_CLK_INN	B16	NC	C16	NC	D16	NC
A17	GND	B17	GND	C17	GND	D17	GND
A18	FPGA_BR89_LVDS2A_B_12P_IO24	B18	FPGA_BR81_LVDS2A_B_09P_IO30/CLKOUT_0P	C18	FPGA_BK89_LVDS2A_B_04P_IO40/CLKOUT_1P	D18	FPGA_BM78_LVDS2A_B_01P_IO46
A19	FPGA_BU89_LVDS2A_B_12N_IO25	B19	FPGA_BU81_LVDS2A_B_09N_IO31/CLKOUT_0N	C19	FPGA_BM89_LVDS2A_B_04N_IO41/CLKOUT_1N	D19	FPGA_BK78_LVDS2A_B_01N_IO47
A20	FPGA_CH78_LVDS2A_B_13P_IO22	B20	FPGA_BW89_LVDS2A_B_10P_IO28	C20	FPGA_BH89_LVDS2A_B_05P_IO38	D20	FPGA_BH81_LVDS2A_B_02P_IO44
A21	FPGA_CF78_LVDS2A_B_13N_IO23	B21	FPGA_CA89_LVDS2A_B_10N_IO29	C21	FPGA_BH92_LVDS2A_B_05N_IO39	D21	FPGA_BH78_LVDS2A_B_02N_IO45
A22	FPGA_BW78_LVDS2A_B_07P_IO34/CLKIN_0P	B22	FPGA_BR92_LVDS2A_B_11P_IO26	C22	FPGA_BR78_LVDS2A_B_08P_IO32	D22	FPGA_BM81_LVDS2A_B_03P_IO42
A23	FPGA_CA78_LVDS2A_B_07N_IO35/CLKIN_0N	B23	FPGA_BU92_LVDS2A_B_11N_IO27	C23	FPGA_CU78_LVDS2A_B_08N_IO33	D23	FPGA_BP81_LVDS2A_B_03N_IO43
A24	GND	B24	GND	C24	GND	D24	GND
A25	FPGA_CL88_LVDS2A_B_22P_IO4	B25	FPGA_CK76_LVDS2A_B_19P_IO10	C25	FPGA_CH89_LVDS2A_B_16P_IO16	D25	FPGA_BP92_LVDS2A_B_06P_IO36/CLKIN_1P
A26	FPGA_CK88_LVDS2A_B_22N_IO5	B26	FPGA_CL76_LVDS2A_B_19N_IO11	C26	FPGA_CF89_LVDS2A_B_16N_IO17	D26	FPGA_BM92_LVDS2A_B_06N_IO37/CLKIN_1N
A27	FPGA_CK97_LVDS2A_B_23P_IO2	B27	FPGA_CK80_LVDS2A_B_20P_IO8	C27	FPGA_CF92_LVDS2A_B_17P_IO14	D27	FPGA_CA81_LVDS2A_B_14P_IO20
A28	FPGA_CL97_LVDS2A_B_23N_IO3	B28	FPGA_CL82_LVDS2A_B_20N_IO9	C28	FPGA_CH92_LVDS2A_B_17N_IO15	D28	FPGA_CC81_LVDS2A_B_14N_IO21
A29	FPGA_CL91_LVDS2A_B_24P_IO0	B29	FPGA_CK85_LVDS2A_B_21P_IO6	C29	FPGA_CC92_LVDS2A_B_18P_IO12	D29	FPGA_CF81_LVDS2A_B_15P_IO18
A30	FPGA_CK94_LVDS2A_B_24N_IO1	B30	FPGA_CL85_LVDS2A_B_21N_IO7	C30	FPGA_CA92_LVDS2A_B_18N_IO13	D30	FPGA_CH81_LVDS2A_B_15N_IO19

B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name
A31	MSIO/SYS_SYNC_CLK_OUTP	B31	NC	C31	NC	D31	NC
A32	MSIO/SYS_SYNC_CLK_OUTN	B32	NC	C32	NC	D32	NC
A33	GND	B33	GND	C33	GND	D33	GND
A34	FPGA_F27_HVIO_6C_1	B34	FPGA_CA118_HVIO_5A_15	C34	FPGA_CF128_HVIO_5A_7	D34	FPGA_CD134_HVIO_5A_1
A35	FPGA_F24_HVIO_6C_2	B35	FPGA_BW118_HVIO_5A_16	C35	FPGA_CK134_HVIO_5A_8	D35	FPGA_CD135_HVIO_5A_2
A36	FPGA_CL125_HVIO_5A_10/REFCLK2	B36	FPGA_CL128_HVIO_5A_17	C36	FPGA_CF121_HVIO_5A_11	D36	FPGA_CG134_HVIO_5A_3
A37	FPGA_BK31_HVIO_6A_9/REFCLK1	B37	FPGA_CL130_HVIO_5A_18	C37	FPGA_CF118_HVIO_5A_12	D37	FPGA_CG135_HVIO_5A_4
A38	FPGA_CH128_HVIO_5A_9/REFCLK1	B38	FPGA_CK125_HVIO_5A_19	C38	FPGA_BU118_HVIO_5A_13	D38	FPGA_CH132_HVIO_5A_5
A39	FPGA_G1_HVIO_6C_20	B39	FPGA_CK128_HVIO_5A_20	C39	FPGA_BR118_HVIO_5A_14	D39	FPGA_CF132_HVIO_5A_6
A40	GND	B40	GND	C40	GND	D40	GND
A41	FPGA_J1_HVIO_6C_19	B41	FPGA_C2_HVIO_6C_13	C41	FPGA_H18_HVIO_6C_5	D41	FPGA_D8_HVIO_6C_9/REFCLK1
A42	FPGA_G1_HVIO_6C_20	B42	FPGA_D4_HVIO_6C_14	C42	FPGA_D15_HVIO_6C_6	D42	VCC_1V8_G3_6C_IO
A43	FPGA_BU28_HVIO_6A_1	B43	FPGA_F4_HVIO_6C_15	C43	FPGA_F18_HVIO_6C_7	D43	FPGA_K8_HVIO_6C_10/REFCLK2
A44	FPGA_BP31_HVIO_6A_2	B44	FPGA_K4_HVIO_6C_16	C44	FPGA_F15_HVIO_6C_8	D44	NC
A45	FPGA_BR28_HVIO_6A_3	B45	FPGA_G2_HVIO_6C_17	C45	FPGA_F8_HVIO_6C_11	D45	FPGA_H27_HVIO_6C_3
A46	FPGA_BR31_HVIO_6A_4	B46	FPGA_J2_HVIO_6C_18	C46	FPGA_H8_HVIO_6C_12	D46	FPGA_D24_HVIO_6C_4
A47	1PPS	B47	FPGA_BK28_HVIO_6A_11	C47	FPGA_BW28_HVIO_6A_7	D47	FPGA_BU31_HVIO_6A_5
A48	GND	B48	FPGA_BR22_HVIO_6A_12	C48	FPGA_BM31_HVIO_6A_8	D48	FPGA_BM28_HVIO_6A_6
A49	LS_TXVR_REFCLK3P	B49	GND	C49	LS_TXVR_REFCLK1P	D49	GND
A50	LS_TXVR_REFCLK3N	B50	GND	C50	LS_TXVR_REFCLK1N	D50	GND
A51	GND	B51	LS_TXVR_REFCLK2P	C51	GND	D51	REFCLK_GTSL1C_RX_P
A52	GND	B52	LS_TXVR_REFCLK2N	C52	GND	D52	REFCLK_GTSL1C_RX_N
A53	GTSL1C_RX_CH3P	B53	GND	C53	GTSL1C_RX_CH1P	D53	GND
A54	GTSL1C_RX_CH3N	B54	GND	C54	GTSL1C_RX_CH1N	D54	GND
A55	GND	B55	GTSL1C_RX_CH2P	C55	GND	D55	GTSL1C_RX_CH0P
A56	GND	B56	GTSL1C_RX_CH2N	C56	GND	D56	GTSL1C_RX_CH0N
A57	GTSL1C_TX_CH3P	B57	GND	C57	GTSL1C_TX_CH1P	D57	GND
A58	GTSL1C_TX_CH3N	B58	GND	C58	GTSL1C_TX_CH1N	D58	GND
A59	GND	B59	GTSL1C_TX_CH2P	C59	GND	D59	GTSL1C_TX_CH0P
A60	GND	B60	GTSL1C_TX_CH2N	C60	GND	D60	GTSL1C_TX_CH0N

2.5.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector1 of Agilex 5 SoC FPGA SOM, FPGA section is explained in the following section.

2.5.1.1 FPGA HSIOs – HSIO BANK 2A

The Agilex 5 SoC FPGA SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector1 from HSIO Bank 2A.

The IO voltage of HSIO Bank 2A is connected from Buck3 output of PMIC Regulator and it supports variable IO voltage setting. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC Buck3 output to appropriate IO voltage for HSIO Bank 2A. By default, IO voltage of HSIO Bank 2A is configured to 1.2V in Uboot. For more details about supported IO standard, refer the Agilex 5 datasheet.

In Agilex 5 SOM, HSIO Bank 2A signals are routed as LVDS IOs to Board-to-Board Connector1. Even though these signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A22, A23, D9, D10, D11, D12, D25 and D26 are Clock Input capable pins, while B13, B14, B18, B19, C13, C14, C18 and C19 are Clock Output capable pins of HSIO bank 2A.

For more details on HSIO Bank 2A pinouts on Board-to-Board Connector1, refer the below table.

Table 9: HSIO Bank 2A Pinouts

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A3	FPGA_CA69_LVDS2A_T_10N_IO77	IOB, DIFF_IO_2A_T10N, DQSN1	2A	CA69	IO, 1.2V	Bank 2A_T IO10 Differential negative or single ended I/O
A2	FPGA_BW69_LVDS2A_T_10P_IO76	IOB, DIFF_IO_2A_T10P, DQS1	2A	BW69	IO ,1.2V	Bank 2A_T IO10 Differential positive or single ended I/O
A5	FPGA_BU71_LVDS2A_T_11N_IO75	IOB, CDR, DIFF_IO_2A_T11N, DQ1	2A	BU71	IO, 1.2V	Bank 2A_T IO11 Differential negative or single ended I/O
A4	FPGA_BR71_LVDS2A_T_11P_IO74	IOB, CDR, DIFF_IO_2A_T11P, DQ1	2A	BR71	IO ,1.2V	Bank 2A_T IO11 Differential positive or single ended I/O
A7	FPGA_BU69_LVDS2A_T_12N_IO73	IOB, DIFF_IO_2A_T12N, DQ1	2A	BU69	IO, 1.2V	Bank 2A_T IO12 Differential negative or single ended I/O
A6	FPGA_BR69_LVDS2A_T_12P_IO72	IOB, DIFF_IO_2A_T12P, DQ1	2A	BR69	IO ,1.2V	Bank 2A_T IO12 Differential positive or single ended I/O
A10	FPGA_BE86_LVDS2A_T_22N_IO53	IOB, DIFF_IO_2A_T22N, DQSN3	2A	BE86	IO, 1.2V	Bank 2A_T IO22 Differential negative or single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A9	FPGA_BF86_LVDS2A_T_22P_IO52	IOB, DIFF_IO_2A_T22P, DQS3	2A	BF86	IO ,1.2V	Bank 2A_T IO22 Differential positive or single ended I/O
A12	FPGA_BF90_LVDS2A_T_23N_IO51	IOB, CDR, DIFF_IO_2A_T23N, DQ3	2A	BF90	IO, 1.2V	Bank 2A_T IO23 Differential negative or single ended I/O
A11	FPGA_BF93_LVDS2A_T_23P_IO50	IOB, CDR, DIFF_IO_2A_T23P, DQ3	2A	BF93	IO ,1.2V	Bank 2A_T IO23 Differential positive or single ended I/O
A14	FPGA_BE93_LVDS2A_T_24N_IO49	IOB, DIFF_IO_2A_T24N, DQ3	2A	BE93	IO, 1.2V	Bank 2A_T IO24 Differential negative or single ended I/O
A13	FPGA_BE96_LVDS2A_T_24P_IO48	IOB, DIFF_IO_2A_T24P, DQ3	2A	BE96	IO ,1.2V	Bank 2A_T IO24 Differential positive or single ended I/O
A19	FPGA_BU89_LVDS2A_B_12N_IO25	IOB, DIFF_IO_2A_B12N, DQ5	2A	BU89	IO, 1.2V	Bank 2A_B IO12 Differential negative or single ended I/O
A18	FPGA_BR89_LVDS2A_B_12P_IO24	IOB, DIFF_IO_2A_B12P, DQ5	2A	BR89	IO ,1.2V	Bank 2A_B IO12 Differential positive or single ended I/O
A21	FPGA_CF78_LVDS2A_B_13N_IO23	IOB, CDR, DIFF_IO_2A_B13N, DQ6	2A	CF78	IO, 1.2V	Bank 2A_B IO13 Differential negative or single ended I/O
A20	FPGA_CH78_LVDS2A_B_13P_IO22	IOB, CDR, DIFF_IO_2A_B13P, DQ6	2A	CH78	IO ,1.2V	Bank 2A_B IO13 Differential positive or single ended I/O
A23	FPGA_CA78_LVDS2A_B_07N_IO35/CLKIN_0N	IOB, CLK_B_2A_0N, CDR, DIFF_IO_2A_B7N, DQ5	2A	CA78	IO, 1.2V	Bank 2A_B IO7 Differential negative or single ended I/O
A22	FPGA_BW78_LVDS2A_B_07P_IO34/CLKIN_0P	IOB, CLK_B_2A_0P, CDR, DIFF_IO_2A_B7P, DQ5	2A	BW78	IO ,1.2V	Bank 2A_B IO7 Differential positive or single ended I/O
A25	FPGA_CL88_LVDS2A_B_22P_IO4	IOB, DIFF_IO_2A_B22P, DQS7	2A	CL88	IO, 1.2V	Bank 2A_B IO22 Differential positive or single ended I/O
A26	FPGA_CK88_LVDS2A_B_22N_IO5	IOB, DIFF_IO_2A_B22N, DQSN7	2A	CK88	IO ,1.2V	Bank 2A_B IO22 Differential negative or single ended I/O
A28	FPGA_CL97_LVDS2A_B_23N_IO3	IOB, CDR, DIFF_IO_2A_B23N, DQ7	2A	CL97	IO, 1.2V	Bank 2A_B IO23 Differential negative or single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A27	FPGA_CK97_LVDS2A_B_23P_IO2	IOB, CDR, DIFF_IO_2A_B23P, DQ7	2A	CK97	IO ,1.2V	Bank 2A_B IO23 Differential positive or single ended I/O
A30	FPGA_CK94_LVDS2A_B_24N_IO1	IOB, DIFF_IO_2A_B24N, DQ7	2A	CK94	IO, 1.2V	Bank 2A_B IO24 Differential negative or single ended I/O
A29	FPGA_CL91_LVDS2A_B_24P_IO0	IOB, DIFF_IO_2A_B24P, DQ7	2A	CL91	IO ,1.2V	Bank 2A_B IO24 Differential positive or single ended I/O
B3	FPGA_CA59_LVDS2A_T_7N_IO83	IOB, DIFF_IO_2A_T7N, DQ1	2A	CA59	IO, 1.2V	Bank 2A_T IO7 Differential negative or single ended I/O
B2	FPGA_CW59_LVDS2A_T_7P_IO82	IOB, DIFF_IO_2A_T7P, DQ1	2A	BW59	IO ,1.2V	Bank 2A_T IO7 Differential positive or single ended I/O
B5	FPGA_BR59_LVDS2A_T_8N_IO81	IOB, DIFF_IO_2A_T8N, DQ1	2A	BR59	IO, 1.2V	Bank 2A_T IO8 Differential negative or single ended I/O
B4	FPGA_BU59_LVDS2A_T_8P_IO80	IOB, DIFF_IO_2A_T8P, DQ1	2A	BU59	IO ,1.2V	Bank 2A_T IO8 Differential positive or single ended I/O
B7	FPGA_BR62_LVDS2A_T_9N_IO79	IOB, DIFF_IO_2A_T9N, DQ1	2A	BR62	IO, 1.2V	Bank 2A_T IO9 Differential negative or single ended I/O
B6	FPGA_BU62_LVDS2A_T_9P_IO78	IOB, DIFF_IO_2A_T9P, DQ1	2A	BU62	IO ,1.2V	Bank 2A_T IO9 Differential positive or single ended I/O
B10	FPGA_BH71_LVDS2A_T_17N_IO63	IOB, CDR, DIFF_IO_2A_T17N, DQ2	2A	BH71	IO, 1.2V	Bank 2A_T IO17 Differential negative or single ended I/O
B9	FPGA_BH69_LVDS2A_T_17P_IO62	IOB, RZQ_T_2A, CDR, DIFF_IO_2A_T17P, DQ2	2A	BH69	IO ,1.2V	Bank 2A_T IO17 Differential positive or single ended I/O
B12	FPGA_BE75_LVDS2A_T_20N_IO57	IOB, DIFF_IO_2A_T20N, DQ3	2A	BE75	IO, 1.2V	Bank 2A_T IO20 Differential negative or single ended I/O
B11	FPGA_BE79_LVDS2A_T_20P_IO56	IOB, DIFF_IO_2A_T20P, DQ3	2A	BE79	IO ,1.2V	Bank 2A_T IO20 Differential positive or single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B14	FPGA_BF83_LVDS2A_T_21N_IO55/CLKOUT_0N	IOB, PLL_2A_T_CLKOUT0N, DIFF_IO_2A_T21N, DQ3	2A	BF83	IO, 1.2V	Bank 2A_T IO21 Differential negative or single ended I/O
B13	FPGA_BE83_LVDS2A_T_21P_IO54/CLKOUT_0P	IOB, PLL_2A_T_CLKOUT0P, PLL_2A_T_CLKOUT0, PLL_2A_T_FB0,DIFF_IO_2A_T21P, DQ3	2A	BE83	IO ,1.2V	Bank 2A_T IO21 Differential positive or single ended I/O
B19	FPGA_BU81_LVDS2A_B_09N_IO31/CLKOUT_0N	IOB, PLL_2A_B_CLKOUT0N, DIFF_IO_2A_B9N, DQ5	2A	BU81	IO, 1.2V	Bank 2A_B IO9 Differential negative or single ended I/O
B18	FPGA_BR81_LVDS2A_B_09P_IO30/CLKOUT_0P	IOB, PLL_2A_B_CLKOUT0P, PLL_2A_B_CLKOUT0, PLL_2A_B_FB0, DIFF_IO_2A_B9P, DQ5	2A	BR81	IO ,1.2V	Bank 2A_B IO9 Differential positive or single ended I/O
B21	FPGA_CA89_LVDS2A_B_10N_IO29	IOB, DIFF_IO_2A_B10N, DQSN5	2A	CA89	IO, 1.2V	Bank 2A_B IO10 Differential negative or single ended I/O
B20	FPGA_BW89_LVDS2A_B_10P_IO28	IOB, DIFF_IO_2A_B10P, DQS5	2A	BW89	IO ,1.2V	Bank 2A_B IO10 Differential positive or single ended I/O
B23	FPGA_BU92_LVDS2A_B_11N_IO27	IOB, CDR, DIFF_IO_2A_B11N, DQ5	2A	BU92	IO, 1.2V	Bank 2A_B IO11 Differential negative or single ended I/O
B22	FPGA_BR92_LVDS2A_B_11P_IO26	IOB, CDR, DIFF_IO_2A_B11P, DQ5	2A	BR92	IO ,1.2V	Bank 2A_B IO11 Differential positive or single ended I/O
B26	FPGA_CL76_LVDS2A_B_19N_IO11	IOB, CDR, DIFF_IO_2A_B19N, DQ7	2A	CL76	IO, 1.2V	Bank 2A_B IO19 Differential negative or single ended I/O
B28	FPGA_CL82_LVDS2A_B_20N_IO9	IOB, DIFF_IO_2A_B20N, DQ7	2A	CL82	IO ,1.2V	Bank 2A_B IO20 Differential negative or single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B27	FPGA_CK80_LVDS2A_B_20P_IO8	IOB, DIFF_IO_2A_B20P, DQ7	2A	CK80	IO, 1.2V	Bank 2A_B IO20 Differential positive or single ended I/O
B30	FPGA_CL85_LVDS2A_B_21N_IO7	IOB, DIFF_IO_2A_B21N, DQ7	2A	CL85	IO ,1.2V	Bank 2A_B IO21 Differential negative or single ended I/O
B29	FPGA_CK85_LVDS2A_B_21P_IO6	IOB, DIFF_IO_2A_B21P, DQ7	2A	CK85	IO, 1.2V	Bank 2A_B IO21 Differential positive or single ended I/O
B25	FPGA_CK76_LVDS2A_B_19P_IO10	IOB, CDR, DIFF_IO_2A_B19P, DQ7	2A	CK76	IO ,1.2V	Bank 2A_B IO19 Differential positive or single ended I/O
C3	FPGA_CF69_LVDS2A_T_4N_IO89	IOB, DIFF_IO_2A_T4N, DQSN0	2A	CF69	IO, 1.2V	Bank 2A_T IO4 Differential negative or single ended I/O
C2	FPGA_CH69_LVDS2A_T_4P_IO88	IOB, DIFF_IO_2A_T4P, DQS0	2A	CH69	IO ,1.2V	Bank 2A_T IO4 Differential positive or single ended I/O
C5	FPGA_CA71_LVDS2A_T_5N_IO87	IOB, CDR, DIFF_IO_2A_T5N, DQ0	2A	CA71	IO, 1.2V	Bank 2A_T IO5 Differential negative or single ended I/O
C4	FPGA_CC71_LVDS2A_T_5P_IO86	IOB, CDR, DIFF_IO_2A_T5P, DQ0	2A	CC71	IO ,1.2V	Bank 2A_T IO5 Differential positive or single ended I/O
C7	FPGA_CH71_LVDS2A_T_6N_IO85	IOB, DIFF_IO_2A_T6N, DQ0	2A	CH71	IO, 1.2V	Bank 2A_T IO6 Differential negative or single ended I/O
C6	FPGA_CF71_LVDS2A_T_6P_IO84	IOB, DIFF_IO_2A_T6P, DQ0	2A	CF71	IO ,1.2V	Bank 2A_T IO6 Differential positive or single ended I/O
C10	FPGA_BH59_LVDS2A_T_14N_IO69	IOB, DIFF_IO_2A_T14N, DQ2	2A	BH59	IO, 1.2V	Bank 2A_T IO14 Differential negative or single ended I/O
C9	FPGA_BH62_LVDS2A_T_14P_IO68	IOB, DIFF_IO_2A_T14P, DQ2	2A	BH62	IO ,1.2V	Bank 2A_T IO14 Differential positive or single ended I/O
C12	FPGA_BP62_LVDS2A_T_15N_IO67	IOB, DIFF_IO_2A_T15N, DQ2	2A	BP62	IO, 1.2V	Bank 2A_T IO15 Differential negative or single ended I/O
C11	FPGA_BM62_LVDS2A_T_15P_IO66	IOB, DIFF_IO_2A_T15P, DQ2	2A	BM62	IO ,1.2V	Bank 2A_T IO15 Differential positive or single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C14	FPGA_BK69_LVDS2A_T_16N_IO65/CLKOUT_1N	IOB, PLL_2A_T_CLKOUT1N, DIFF_IO_2A_T16N, DQSN2	2A	BK69	IO, 1.2V	Bank 2A_T IO16 Differential negative or single ended I/O
C13	FPGA_BM69_LVDS2A_T_16P_IO64/CLKOUT_1P	IOB, PLL_2A_T_CLKOUT1P, PLL_2A_T_CLKOUT1, PLL_2A_T_FB1, DIFF_IO_2A_T16P, DQS2	2A	BM69	IO ,1.2V	Bank 2A_T IO16 Differential positive or single ended I/O
C19	FPGA_BM89_LVDS2A_B_04N_IO41/CLKOUT_1N	IOB, PLL_2A_B_CLKOUT1N, DIFF_IO_2A_B4N, DQSN4	2A	BM89	IO, 1.2V	Bank 2A_B IO4 Differential negative or single ended I/O
C18	FPGA_BK89_LVDS2A_B_04P_IO40/CLKOUT_1P	IOB, PLL_2A_B_CLKOUT1P, PLL_2A_B_CLKOUT1, PLL_2A_B_FB1, DIFF_IO_2A_B4P, DQS4	2A	BK89	IO ,1.2V	Bank 2A_B IO4 Differential positive or single ended I/O
C21	FPGA_BH92_LVDS2A_B_05N_IO39	IOB, CDR, DIFF_IO_2A_B5N, DQ4	2A	BH92	IO, 1.2V	Bank 2A_B IO5 Differential negative or single ended I/O
C20	FPGA_BH89_LVDS2A_B_05P_IO38	IOB, RZQ_B_2A, CDR, DIFF_IO_2A_B5P, DQ4	2A	BH39	IO ,1.2V	Bank 2A_T IO4 Differential positive or single ended I/O
C23	FPGA_CU78_LVDS2A_B_08N_IO33	IOB, DIFF_IO_2A_B8N, DQ5	2A	BU78	IO, 1.2V	Bank 2A_B IO8 Differential negative or single ended I/O
C22	FPGA_BR78_LVDS2A_B_08P_IO32	IOB, DIFF_IO_2A_B8P, DQ5	2A	BR78	IO ,1.2V	Bank 2A_B IO8 Differential positive or single ended I/O
C26	FPGA_CF89_LVDS2A_B_16N_IO17	IOB, DIFF_IO_2A_B16N, DQSN6	2A	CF89	IO, 1.2V	Bank 2A_B IO16 Differential negative or single ended I/O
C25	FPGA_CH89_LVDS2A_B_16P_IO16	IOB, DIFF_IO_2A_B16P, DQS6	2A	CH89	IO ,1.2V	Bank 2A_B IO16 Differential positive or single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C28	FPGA_CH92_LVDS2A_B_17N_IO15	IOB, CDR, DIFF_IO_2A_B17N, DQ6	2A	CH92	IO, 1.2V	Bank 2A_B IO17 Differential negative or single ended I/O
C27	FPGA_CF92_LVDS2A_B_17P_IO14	IOB, CDR, DIFF_IO_2A_B17P, DQ6	2A	CF92	IO ,1.2V	Bank 2A_B IO17 Differential positive or single ended I/O
C30	FPGA_CA92_LVDS2A_B_18N_IO13	IOB, DIFF_IO_2A_B18N, DQ6	2A	CA92	IO, 1.2V	Bank 2A_B IO18 Differential negative or single ended I/O
C29	FPGA_CC92_LVDS2A_B_18P_IO12	IOB, DIFF_IO_2A_B18P, DQ6	2A	CC92	IO ,1.2V	Bank 2A_B IO18 Differential positive or single ended I/O
D3	FPGA_CH59_LVDS2A_T_1N_IO95	IOB, DIFF_IO_2A_T1N, DQ0	2A	CH59	IO, 1.2V	Bank 2A_T IO1 Differential negative or single ended I/O
D2	FPGA_CF59_LVDS2A_T_1P_IO94	IOB, DIFF_IO_2A_T1P, DQ0	2A	CF59	IO ,1.2V	Bank 2A_T IO1 Differential positive or single ended I/O
D5	FPGA_CH62_LVDS2A_T_2N_IO93	IOB, DIFF_IO_2A_T2N, DQ0	2A	CH62	IO, 1.2V	Bank 2A_T IO2 Differential negative or single ended I/O
D4	FPGA_CF62_LVDS2A_T_2P_IO92	IOB, DIFF_IO_2A_T2P, DQ0	2A	CF62	IO ,1.2V	Bank 2A_T IO2 Differential positive or single ended I/O
D7	FPGA_CC62_LVDS2A_T_3N_IO91	IOB, DIFF_IO_2A_T3N, DQ0	2A	CC62	IO, 1.2V	Bank 2A_T IO3 Differential negative or single ended I/O
D6	FPGA_CA62_LVDS2A_T_3P_IO90	IOB, DIFF_IO_2A_T3P, DQ0	2A	CA62	IO ,1.2V	Bank 2A_T IO3 Differential positive or single ended I/O
D10	FPGA_BF72_LVDS2A_T_19N_IO59/CLKIN_0N	IOB, CLK_T_2A_0N, DIFF_IO_2A_T19N, DQ3	2A	BF72	IO, 1.2V	Bank 2A_T IO19 Differential negative or single ended I/O
D9	FPGA_BF75_LVDS2A_T_19P_IO58/CLKIN_0P	IOB, CLK_T_2A_0P, DIFF_IO_2A_T19P, DQ3	2A	BF75	IO ,1.2V	Bank 2A_T IO19 Differential positive or single ended I/O
D12	FPGA_BP71_LVDS2A_T_18N_IO61/CLKIN_1N	IOB, CLK_T_2A_1N, DIFF_IO_2A_T18N, DQ2	2A	BP71	IO, 1.2V	Bank 2A_T IO18 Differential negative or single ended I/O
D11	FPGA_BM71_LVDS2A_T_18P_IO60/CLKIN_1P	IOB, CLK_T_2A_1P, DIFF_IO_2A_T18P, DQ2	2A	BM71	IO ,1.2V	Bank 2A_T IO8 Differential positive or single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D14	FPGA_BK59_LVDS2A_T_13N_IO71	IOB, DIFF_IO_2A_T13N, DQ2	2A	BK59	IO, 1.2V	Bank 2A_T IO13 Differential negative or single ended I/O
D13	FPGA_BM59_LVDS2A_T_13P_IO70	IOB, DIFF_IO_2A_T13P, DQ2	2A	BM59	IO ,1.2V	Bank 2A_T IO13 Differential positive or single ended I/O
D19	FPGA_BK78_LVDS2A_B_01N_IO47	IOB, CDR, DIFF_IO_2A_B1N, DQ4	2A	BK78	IO, 1.2V	Bank 2A_B IO1 Differential negative or single ended I/O
D18	FPGA_BM78_LVDS2A_B_01P_IO46	IOB, CDR, DIFF_IO_2A_B1P, DQ4	2A	BM78	IO ,1.2V	Bank 2A_B IO1 Differential positive or single ended I/O
D21	FPGA_BH78_LVDS2A_B_02N_IO45	IOB, DIFF_IO_2A_B2N, DQ4	2A	BH78	IO, 1.2V	Bank 2A_B IO2 Differential negative or single ended I/O
D20	FPGA_BH81_LVDS2A_B_02P_IO44	IOB, DIFF_IO_2A_B2P, DQ4	2A	BH81	IO ,1.2V	Bank 2A_B IO2 Differential positive or single ended I/O
D23	FPGA_BP81_LVDS2A_B_03N_IO43	IOB, DIFF_IO_2A_B3N, DQ4	2A	BP81	IO, 1.2V	Bank 2A_B IO3 Differential negative or single ended I/O
D22	FPGA_BM81_LVDS2A_B_03P_IO42	IOB, DIFF_IO_2A_B3P, DQ4	2A	BM81	IO ,1.2V	Bank 2A_B IO3 Differential positive or single ended I/O
D26	FPGA_BM92_LVDS2A_B_06N_IO37/CLKIN_1N	IOB, CLK_B_2A_1N, DIFF_IO_2A_B6N, DQ4	2A	BM92	IO, 1.2V	Bank 2A_B IO6 Differential negative or single ended I/O
D25	FPGA_BP92_LVDS2A_B_06P_IO36/CLKIN_1P	IOB, CLK_B_2A_1P, DIFF_IO_2A_B6P, DQ4	2A	BP92	IO ,1.2V	Bank 2A_B IO6 Differential positive or single ended I/O
D28	FPGA_CC81_LVDS2A_B_14N_IO21	IOB, DIFF_IO_2A_B14N, DQ6	2A	CC81	IO, 1.2V	Bank 2A_B IO14 Differential negative or single ended I/O
D27	FPGA_CA81_LVDS2A_B_14P_IO20	IOB, DIFF_IO_2A_B14P, DQ6	2A	CA81	IO ,1.2V	Bank 2A_B IO14 Differential positive or single ended I/O
D30	FPGA_CH81_LVDS2A_B_15N_IO19	IOB, DIFF_IO_2A_B15N, DQ6	2A	CH81	IO, 1.2V	Bank 2A_B IO15 Differential negative or single ended I/O
D29	FPGA_CF81_LVDS2A_B_15P_IO18	IOB, DIFF_IO_2A_B15P, DQ6	2A	CF81	IO ,1.2V	Bank 2A_B IO15 Differential positive or single ended I/O

2.5.1.2 FPGA HVIOs – HVIO Bank 5A

The Agilex 5 SOM supports 20 Single Ended (SE) IOs on Board-to-Board Connector1 from HVIO Bank 5A. Upon these 20 SE IOs, two can be used as reference clocks. Both are directly connected to Board-to-Board Connector1.

The IO voltage of HVIO 5A is connected from LDO2 output of PMIC Regulator and it supports variable IO voltage setting. IO voltage is configured to 1.8V by default during power up. While using as Single Ended IOs, make sure to set the PMIC LDO2 output to appropriate IO voltage for Bank 5A. For more details about supported IO standard, refer the Agilex 5 datasheet.

For more details on HVIO Bank 5A pinouts on Board-to-Board Connector1, refer the below table.

Table 10: HVIO Bank 5A Pinouts

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D34	FPGA_CD134_HVIO_5A_1	HVIO_5A_1, SYSPLLREFCLK_L1A_0, TXCLK1, DATA_CTRL1	5A	CD134	I/O 1.8V	HVIO Bank 5A_1 Single Ended IO Signal
D35	FPGA_CD135_HVIO_5A_2	HVIO_5A_2, SYSPLLREFCLK_L1A_1, TXCLK2, DATA_CTRL2	5A	CD135	I/O 1.8V	HVIO Bank 5A_2 Single Ended IO Signal
D36	FPGA_CG134_HVIO_5A_3	HVIO_5A_3, SYSPLLREFCLK_L1B_0, TXCLK3, DATA_CTRL3	5A	CG134	I/O 1.8V	HVIO Bank 5A_3 Single Ended IO Signal
D37	FPGA_CG135_HVIO_5A_4	HVIO_5A_4, SYSPLLREFCLK_L1B_1, TXCLK4, DATA_CTRL4	5A	CG135	I/O 1.8V	HVIO Bank 5A_4 Single Ended IO Signal
D38	FPGA_CH132_HVIO_5A_5	HVIO_5A_5, PIN_PERST_N_CVP_L1A_0, TXCLK5, DATA_CTRL5	5A	CH132	I/O 1.8V	HVIO Bank 5A_5 Single Ended IO Signal
D39	FPGA_CF132_HVIO_5A_6	HVIO_5A_6, PIN_PERST_N_CVP_L1B_0, TXCLK6, DATA_CTRL6	5A	CF132	I/O 1.8V	HVIO Bank 5A_6 Single Ended IO Signal
C34	FPGA_CF128_HVIO_5A_7	HVIO_5A_7, PIN_PERST_N_CVP_L1C_0, TXCLK7, DATA_CTRL7	5A	CF128	I/O 1.8V	HVIO Bank 5A_7 Single Ended IO Signal
C35	FPGA_CK134_HVIO_5A_8	HVIO_5A_8, TXCLK8, DATA_CTRL8	5A	CK134	I/O 1.8V	HVIO Bank 5A_8 Single Ended IO Signal

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A38	FPGA_CH128_HVIO_5A_9/REFCLK1	HVIO_5A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9	5A	CH128	I/O 1.8V	HVIO Bank 5A_9 Single Ended IO Signal and can also be used as Reference Clock
A36	FPGA_CL125_HVIO_5A_10/REFCLK2	HVIO_5A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10	5A	CL125	I/O 1.8V	HVIO Bank 5A_10 Single Ended IO Signal and can also be used as Reference clock
C36	FPGA_CF121_HVIO_5A_11	HVIO_5A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11	5A	CF121	I/O 1.8V	HVIO Bank 5A_11 Single Ended IO Signal
C37	FPGA_CF118_HVIO_5A_12	HVIO_5A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12	5A	CF118	I/O 1.8V	HVIO Bank 5A_12 Single Ended IO Signal
C38	FPGA_BU118_HVIO_5A_13	HVIO_5A_13, TXCLK13, DATA_CTRL13	5A	BU118	I/O 1.8V	HVIO Bank 5A_13 Single Ended IO Signal
C39	FPGA_BR118_HVIO_5A_14	HVIO_5A_14, TXCLK14, DATA_CTRL14	5A	BR118	I/O 1.8V	HVIO Bank 5A_14 Single Ended IO Signal
B34	FPGA_CA118_HVIO_5A_15	HVIO_5A_15, TXCLK15, DATA_CTRL15	5A	CA118	I/O 1.8V	HVIO Bank 5A_15 Single Ended IO Signal
B35	FPGA_BW118_HVIO_5A_16	HVIO_5A_16, TXCLK16, DATA_CTRL16	5A	BW118	I/O 1.8V	HVIO Bank 5A_16 Single Ended IO Signal
B36	FPGA_CL128_HVIO_5A_17	HVIO_5A_17, TXCLK17, DATA_CTRL17	5A	CL128	I/O 1.8V	HVIO Bank 5A_17 Single Ended IO Signal
B37	FPGA_CL130_HVIO_5A_18	HVIO_5A_18, TXCLK18, DATA_CTRL18	5A	CL130	I/O 1.8V	HVIO Bank 5A_18 Single Ended IO Signal
B38	FPGA_CK125_HVIO_5A_19	HVIO_5A_19, SYSPLLREFCLK_L1C_0, TXCLK19, DATA_CTRL19	5A	CK125	I/O 1.8V	HVIO Bank 5A_19 Single Ended IO Signal
B39	FPGA_CK128_HVIO_5A_20	HVIO_5A_20, TXCLK20, DATA_CTRL20	5A	CK128	I/O 1.8V	HVIO Bank 5A_20 Single Ended IO Signal

2.5.1.3 FPGA HVIOs – HVIO Bank 6A & 6C

The Agilex 5 SOM supports 20 Single Ended (SE) IOs on Board-to-Board Connector1 from HVIO Bank 6C and 11 Single Ended (SE) IOs from HVIO Bank 6A. Upon these 3 SE IOs, up to 3 are Reference Clocks.

The IO voltage of HVIO Bank 6A is connected from Buck4 output of the PMIC Regulator, and it fixed to 1.8V. Likewise, the IO Voltage of HVIO Bank 6C is connected from LDO3 output of the PMIC Regulator and supports variable IO voltage setting with set to 1.8V during bootup. While using these Single Ended IOs, make sure to set the PMIC output to appropriate IO voltage for HVIO Bank 6C. For more details about supported IO standard, refer the Agilex 5 datasheet.

In the Agilex 5 SOM HVIO Bank 6A and 6C signals are routed as Single Ended (SE) IOs to Board-to-Board Connector1. The Board-to-Board Connector1 pins D41, D43 and A37 are Reference Clock capable pins.

Table 11: HVIO Bank 6A and 6C

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
HVIO Bank 6A						
A43	FPGA_BU28_HVIO_6A_1	HVIO_6A_1, SYSPLLREFCLK_R4A_0, TXCLK1, DATA_CTRL1	6A	BU28	I/O, 1.8V	HVIO Banck 6A_1 Single Ended IO Signal
A44	FPGA_BP31_HVIO_6A_2	HVIO_6A_2, SYSPLLREFCLK_R4A_1, TXCLK2, DATA_CTRL2	6A	BP31	I/O, 1.8V	HVIO Banck 6A_2 Single Ended IO Signal
A45	FPGA_BR28_HVIO_6A_3	HVIO_6A_3, SYSPLLREFCLK_R4B_0, TXCLK3, DATA_CTRL3	6A	BR28	I/O, 1.8V	HVIO Banck 6A_3 Single Ended IO Signal
A46	FPGA_BR31_HVIO_6A_4	HVIO_6A_4, SYSPLLREFCLK_R4B_1, TXCLK4, DATA_CTRL4	6A	BR31	I/O, 1.8V	HVIO Banck 6A_4 Single Ended IO Signal
D47	FPGA_BU31_HVIO_6A_5	HVIO_6A_5, PIN_PERST_N_R4A_0, TXCLK5, DATA_CTRL5	6A	BU31	I/O, 1.8V	HVIO Banck 6A_5 Single Ended IO Signal
D48	FPGA_BM28_HVIO_6A_6	HVIO_6A_6, PIN_PERST_N_R4B_0, TXCLK6, DATA_CTRL6	6A	BM28	I/O, 1.8V	HVIO Banck 6A_6 Single Ended IO Signal
C47	FPGA_BW28_HVIO_6A_7	HVIO_6A_7, PIN_PERST_N_R4C_0, TXCLK7, DATA_CTRL7	6A	BW28	I/O, 1.8V	HVIO Banck 6A_7 Single Ended IO Signal

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C48	FPGA_BM31_HVIO_6A_8	HVIO_6A_8, TXCLK8, DATA_CTRL8	6A	BM31	I/O, 1.8V	HVIO Banck 6A_8 Single Ended IO Signal
A37	FPGA_BK31_HVIO_6A_9/REFCLK1	HVIO_6A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10	6A	BP22	I/O, 1.8V	HVIO Banck 6A_9 Single Ended IO Signal and also can be used as Reference Clock
B47	FPGA_BK28_HVIO_6A_11	HVIO_6A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11	6A	BK28	I/O, 1.8V	HVIO Banck 6A_11 Single Ended IO Signal
B48	FPGA_BR22_HVIO_6A_12	HVIO_6A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12	6A	BR22	I/O, 1.8V	HVIO Banck 6A_12 Single Ended IO Signal
HVIO Bank 6C						
A34	FPGA_F27_HVIO_6C_1	HVIO_6C_1, TXCLK1, DATA_CTRL1	6C	F27	I/O, 1.8V	HVIO Banck 6C_1 Single Ended IO Signal
A35	FPGA_F24_HVIO_6C_2	HVIO_6C_2, TXCLK2, DATA_CTRL2	6C	F24	I/O, 1.8V	HVIO Banck 6C_2 Single Ended IO Signal
D45	FPGA_H27_HVIO_6C_3	HVIO_6C_3, TXCLK3, DATA_CTRL3	6C	H27	I/O, 1.8V	HVIO Banck 6C_3 Single Ended IO Signal
D46	FPGA_D24_HVIO_6C_4	HVIO_6C_4, TXCLK4, DATA_CTRL4	6C	D24	I/O, 1.8V	HVIO Banck 6C_4 Single Ended IO Signal
C41	FPGA_H18_HVIO_6C_5	HVIO_6C_5, TXCLK5, DATA_CTRL5	6C	H18	I/O, 1.8V	HVIO Banck 6C_5 Single Ended IO Signal
C42	FPGA_D15_HVIO_6C_6	HVIO_6C_6, TXCLK6, DATA_CTRL6	6C	D15	I/O, 1.8V	HVIO Banck 6C_6 Single Ended IO Signal
C43	FPGA_F18_HVIO_6C_7	HVIO_6C_7, TXCLK7, DATA_CTRL7	6C	F18	I/O, 1.8V	HVIO Banck 6C_7 Single Ended IO Signal
C44	FPGA_F15_HVIO_6C_8	HVIO_6C_8, TXCLK8, DATA_CTRL8	6C	F15	I/O, 1.8V	HVIO Banck 6C_8 Single Ended IO Signal

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D41	FPGA_D8_HVIO_6C_9/REFCLK1	HVIO_6C_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9	6C	D8	I/O, 1.8V	HVIO Banck 6C_9 Single Ended IO Signal
D43	FPGA_K8_HVIO_6C_10/REFCLK2	HVIO_6C_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10	6C	K8	I/O, 1.8V	HVIO Banck 6C_10 Single Ended IO Signal
C45	FPGA_F8_HVIO_6C_11	HVIO_6C_11, SOURCE_SYNC_CLK 1, TXCLK11, RXCLK3, DATA_CTRL11	6C	F8	I/O, 1.8V	HVIO Banck 6C_11 Single Ended IO Signal
C46	FPGA_H8_HVIO_6C_12	HVIO_6C_12, SOURCE_SYNC_CLK 2, TXCLK12, RXCLK4, DATA_CTRL12	6C	H8	I/O, 1.8V	HVIO Banck 6C_12 Single Ended IO Signal
B41	FPGA_C2_HVIO_6C_13	HVIO_6C_13, TXCLK13, DATA_CTRL13	6C	C2	I/O, 1.8V	HVIO Banck 6C_13 Single Ended IO Signal
B42	FPGA_D4_HVIO_6C_14	HVIO_6C_14, TXCLK14, DATA_CTRL14	6C	D4	I/O, 1.8V	HVIO Banck 6C_14 Single Ended IO Signal
B43	FPGA_F4_HVIO_6C_15	HVIO_6C_15, TXCLK15, DATA_CTRL15	6C	F4	I/O, 1.8V	HVIO Banck 6C_15 Single Ended IO Signal
B44	FPGA_K4_HVIO_6C_16	HVIO_6C_16, TXCLK16, DATA_CTRL16	6C	K4	I/O, 1.8V	HVIO Banck 6C_16 Single Ended IO Signal
B45	FPGA_G2_HVIO_6C_17	HVIO_6C_17, TXCLK17, DATA_CTRL17	6C	G2	I/O, 1.8V	HVIO Banck 6C_17 Single Ended IO Signal
B46	FPGA_J2_HVIO_6C_18	HVIO_6C_18, TXCLK18, DATA_CTRL18	6C	J2	I/O, 1.8V	HVIO Banck 6C_18 Single Ended IO Signal
A41	FPGA_J1_HVIO_6C_19	HVIO_6C_19, TXCLK19, DATA_CTRL19	6C	J1	I/O, 1.8V	HVIO Banck 6C_19 Single Ended IO Signal
A42	FPGA_G1_HVIO_6C_20	HVIO_6C_20, TXCLK20, DATA_CTRL20	6C	G1	I/O, 1.8V	HVIO Banck 6C_20 Single Ended IO Signal

2.5.1.4 High Speed Transceivers

The Intel Agilex 5 SoC and FPGA SOM supports 4 high speed transceiver channels from GTSR Bank 1C. Out of these 4 lanes, one lane is optional as it is used for the on SOM Ethernet PHY and can be made available on the B2B connector when the Ethernet PHY is not used. The Transceivers connected to Board-to-Board Connector1 is capable of running up to a maximum speed of 28Gbps in NRZ Format. These transceivers can be used to interface to multiple high-speed interface protocols. Each 4 Channel Transceiver Bank supports two reference clock input pairs.

Table 12: Transceiver Bank 1C Pinouts

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination*	Description
A54	GTSL1C_RX_CH3N	GTSL1C_RX_CH3N	1C	AK133	I, DIFF	GTSL Bank1C Channel 3 differential Receiver Negative. *Note: By default this signal is not supported on the Board to Board Connector and is connected to On SOM Ethernet PHY for Ethernet support.*
A53	GTSL1C_RX_CH3P	GTSL1C_RX_CH3P	1C	AK135	I, DIFF	GTSL Bank1C Channel 3 differential Receiver Positive *Note: By default this signal is not supported on the Board to Board Connector and is connected to On SOM Ethernet PHY for Ethernet support.*
A58	GTSL1C_TX_CH3N	GTSL1C_TX_CH3N	1C	AL126	O, DIFF	GTSL Bank1C Channel 3 differential Transmitter Negative *Note: By default this signal is not supported on the Board to Board Connector and is connected to On SOM Ethernet PHY for Ethernet support.*
A57	GTSL1C_TX_CH3P	GTSL1C_TX_CH3P	1C	AL129	O, DIFF	GTSL Bank1C Channel 3 differential Transmitter Positive *Note: By default this signal is not supported on the Board to Board Connector and is connected to On SOM Ethernet PHY for Ethernet support.*
B56	GTSL1C_RX_CH2N	GTSL1C_RX_CH2N	1C	AM133	I, DIFF	GTSL Bank1C Channel 2 differential Receiver Negative
B55	GTSL1C_RX_CH2P	GTSL1C_RX_CH2P	1C	AM135	I, DIFF	GTSL Bank1C Channel 2 differential Receiver Positive
B60	GTSL1C_TX_CH2N	GTSL1C_TX_CH2N	1C	AN126	O, DIFF	GTSL Bank1C Channel 2 differential Transmitter Negative

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination*	Description
B59	GTSL1C_TX_CH2P	GTSL1C_TX_CH2P	1C	AN129	O, DIFF	GTSL Bank1C Channel 2 differential Transmitter Positive
C54	GTSL1C_RX_CH1N	GTSL1C_RX_CH1N	1C	AP133	I, DIFF	GTSL Bank1C Channel 1 differential Receiver Negative
C53	GTSL1C_RX_CH1P	GTSL1C_RX_CH1P	1C	AP135	I, DIFF	GTSL Bank1C Channel 1 differential Receiver Positive
C58	GTSL1C_TX_CH1N	GTSL1C_TX_CH1N	1C	AR126	O, DIFF	GTSL Bank1C Channel 1differential Transmitter Negative
C57	GTSL1C_TX_CH1P	GTSL1C_TX_CH1P	1C	AR129	O, DIFF	GTSL Bank1C Channel 1 differential Transmitter Positive
D56	GTSL1C_RX_CH0N	GTSL1C_RX_CH0N	1C	AT133	I, DIFF	GTSL Bank1C Channel 0 differential Receiver Negative
D55	GTSL1C_RX_CH0P	GTSL1C_RX_CH0P	1C	AT135	I, DIFF	GTSL Bank1C Channel 0 differential Receiver Positive
D60	GTSL1C_TX_CH0N	GTSL1C_TX_CH0N	1C	AU126	O, DIFF	GTSL Bank1C Channel 0 differential Transmitter Negative
D59	GTSL1C_TX_CH0P	GTSL1C_TX_CH0P	1C	AU129	O, DIFF	GTSL Bank1C Channel 0 differential Transmitter Positive
D52	REFCLK_GTSL1C_RX_N	REFCLK_GTSL1C_RX_N	1C	AT115	I, DIFF	GTSL Bank1C Reference Clock Negative
D51	REFCLK_GTSL1C_RX_P	REFCLK_GTSL1C_RX_P	1C	AT120	I, DIFF	GTSL Bank1C Reference Clock Positive
C50	LS_TXVR_REFCLK1N	REFCLK_GTSL1C_CH1N	1C	AP115	I, DIFF	GTSL Bank1C Reference Clock Negative *Note: By default this signal is not supported on the Board to Board Connector and is connected to On SOM Clock Synthesizer for Ethernet support.*
C49	LS_TXVR_REFCLK1P	REFCLK_GTSL1C_CH1P	1C	AP120	I, DIFF	GTSL Bank1C Reference Clock Positive *Note: By default this signal is not supported on the Board to Board Connector and is connected to On SOM Clock Synthesizer for Ethernet support.*

2.5.2 Power Control Output

The Agilex 5 SOM, Board to Board Connector1 is assigned with HSIO 2A and HVIO 5A voltage for HSIO and HVIO signals connected to the connector. Also, in Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance. For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

Table 13: Board to Board Connector Power Pins

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B1	VCC_1V8_G3_5A_IO	NA	NA	NA	Power O, 1.8V(50mA)	HVIO Bank 5A IO Voltage
C1	VCC_1V2_G3_IO	NA	NA	NA	Power O, 1.2V(50mA)	HSIO Bank 2A IO Voltage
D1	VCC_1V2_G3_IO	NA	NA	NA	Power O, 1.2V(50mA)	HSIO Bank 2A IO Voltage
A8, A17, A24, A33, A40, A48, A51, A52, A55, A56, A59, A60, B8, B17, B24, B33, B40, B49, B50, B53, B54, B57, B58, C8, C17, C24, C33, C40, C51, C52, C55, C56, C59, C60, D8, D17, D24, D33, D40, D49, D50, D53, D54, D57, D58	GND	NA	NA	NA	Power	Ground.

2.6 Board to Board Connector2

The Agilex 5 SOM Board to Board Connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector2 (J5) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A-TR from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A-TR from Samtech

Staking Height - 5mm

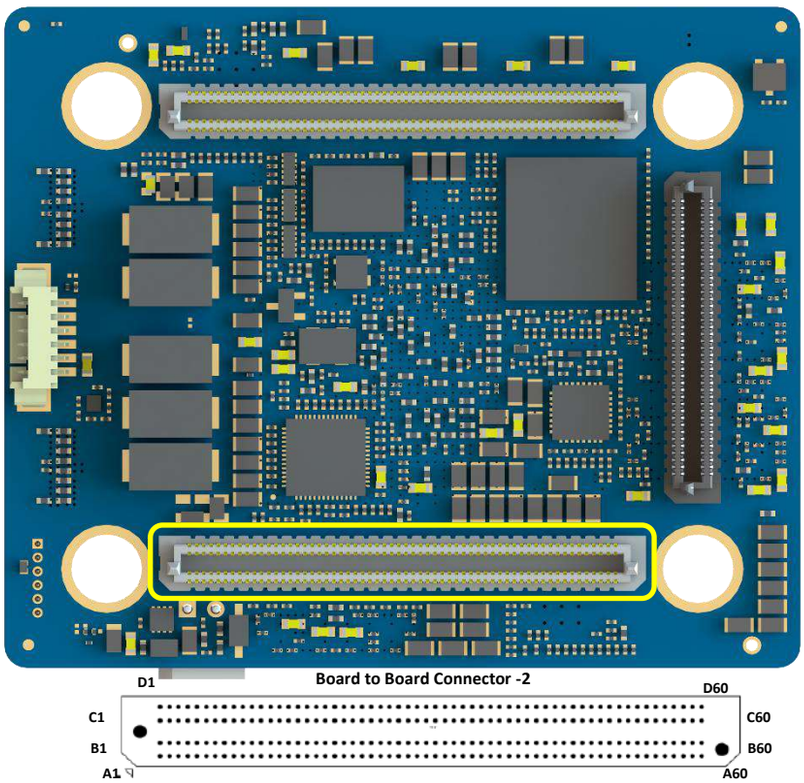

Figure 4: Board to Board Connector 2

Table 14: Board to Board Connector2 Pinout

B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name
A1	VCC_5V_SOM	B1	VCC_5V_SOM	C1	VCC_5V_SOM	D1	VCC_5V_SOM
A1	VCC_5V_SOM	B1	VCC_5V_SOM	C1	VCC_5V_SOM	D1	VCC_5V_SOM
A2	VCC_5V_SOM	B2	VCC_5V_SOM	C2	VCC_5V_SOM	D2	VCC_5V_SOM
A3	VCC_5V_SOM	B3	VCC_5V_SOM	C3	VCC_5V_SOM	D3	VCC_5V_SOM
A4	VCC_5V_SOM	B4	VCC_5V_SOM	C4	VCC_5V_SOM	D4	VCC_5V_SOM
A5	VCC_5V_SOM	B5	VCC_5V_SOM	C5	VCC_5V_SOM	D5	VCC_5V_SOM
A6	GND	B6	GND	C6	GND	D6	GND
A7	GND	B7	GND	C7	GND	D7	GND
A8		B8	SOM_PWR_EN	C8	HPS_I2C0_SCL_1V8	D8	NC
A9	SDM_TCK_B2B	B9	SOM_PWR_OK_1V8	C9	HPS_I2C0_SDA_1V8	D9	VRTC_3V0
A10	SDM_TMS_B2B	B10	HPS_RESET_OUT(GPIO1_3)	C10	F_I2CL	D10	TEMP_CORE_AP
A11	SDM_TDO_B2B	B11	SDM_HPS_NRESET_1V8	C11	F_I2CD	D11	TEMP_CORE_AN
A12	SDM_TDI_B2B	B12	SDM_AS_CONFIG_DONE	C12	HPS_EMAC2_SCL	D12	JTAG_AS_SEL
A13	HPS_UART1_TX	B13	MSIO_PWRBTN#	C13	HPS_EMAC2_SDA	D13	SDM_MSEL1
A14	HPS_UART1_RX	B14	HPS_GPIO0_10_ETH_INT	C14	SD_WP(GPIO1_19)	D14	SDM_MSEL2
A15	GND	B15	GND	C15	GND	D15	GND
A16	USB_OTG_DM	B16	USB_PWR_EN	C16	HPS_EMAC2_TX_CLK	D16	SPI_SCK
A17	USB_OTG_DP	B17	USB_OTG_ID	C17	HPS_EMAC2_TXD0	D17	SPI_IO0
A18	GND	B18	VBUS_USB	C18	HPS_EMAC2_TXD1	D18	SPI_IO1
A19	GPHY_ATXRXM	B19	GPHY_ACTIVITY_LED1	C19	HPS_EMAC2_TXD2	D19	SPI_IO2
A20	GPHY_ATXRXP	B20	GPHY_LINK_LED2	C20	HPS_EMAC2_TXD3	D20	SPI_IO3
A21	GND	B21	SD_PWR_EN(GPIO1_20)	C21	HPS_EMAC2_TX_CTL	D21	SPI_CS0
A22	GPHY_BTXRXM	B22	GND	C22	GND	D22	GND
A23	GPHY_BTXRXP	B23	SD_CLK(GPIO1_12)	C23	HPS_EMAC2_RX_CLK	D23	HPS_UART0_TX
A24	GND	B24	SD_CMD(GPIO1_07)	C24	HPS_EMAC2_RXD0	D24	HPS_UART0_RX
A25	GPHY_CTXRXM	B25	SD_DATA0(GPIO1_00)	C25	HPS_EMAC2_RXD1	D25	HPS_UART0_CTS
A26	GPHY_CTXRXP	B26	SD_DATA1(GPIO1_01)	C26	HPS_EMAC2_RXD2	D26	HPS_UART0_RTS
A27	GND	B27	SD_DATA2(GPIO1_05)	C27	HPS_EMAC2_RXD3	D27	NC
A28	GPHY_DTXRXM	B28	SD_DATA3(GPIO1_06)	C28	HPS_EMAC2_RX_CTL	D28	NC
A29	GPHY_DTXRXP	B29	SD_CD(GPIO1_18)	C29	LS_PCIE_RSTN	D29	NC
A30	GND	B30	HS_PCIE_RSTN	C30	GND	D30	CAN1_TX
A31	REFCLK_GTSL1B_CH1P	B31	GND	C31	REFCLK_GTSL1B_RX_P	D31	GND
A32	REFCLK_GTSL1B_CH1N	B32	GND	C32	REFCLK_GTSL1B_RX_N	D32	GND

B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name
A33	GND	B33	GTSL1B_RX_CH1P	C33	GND	D33	GTSL1B_RX_CH3P
A34	GND	B34	GTSL1B_RX_CH1N	C34	GND	D34	GTSL1B_RX_CH3N
A35	GTSL1B_RX_CH0P	B35	GND	C35	GTSL1B_RX_CH2P	D35	GND
A36	GTSL1B_RX_CH0N	B36	GND	C36	GTSL1B_RX_CH2N	D36	GND
A37	GND	B37	GTSL1B_TX_CH1P	C37	GND	D37	GTSL1B_TX_CH3P
A38	GND	B38	GTSL1B_TX_CH1N	C38	GND	D38	GTSL1B_TX_CH3N
A39	GTSL1B_TX_CH0P	B39	GND	C39	GTSL1B_TX_CH2P	D39	GND
A40	GTSL1B_TX_CH0N	B40	GND	C40	GTSL1B_TX_CH2N	D40	GND
A41	GND	B41	REFCLK_GTSR4B_CH1P	C41	GND	D41	REFCLK_GTSR4B_RX_P
A42	GND	B42	REFCLK_GTSR4B_CH1N	C42	GND	D42	REFCLK_GTSR4B_RX_N
A43	GTSR4B_RX_CH0P	B43	GND	C43	GTSR4B_RX_CH2P	D43	GND
A44	GTSR4B_RX_CH0N	B44	GND	C44	GTSR4B_RX_CH2N	D44	GND
A45	GND	B45	GTSR4B_RX_CH1P	C45	GND	D45	GTSR4B_RX_CH3P
A46	GND	B46	GTSR4B_RX_CH1N	C46	GND	D46	GTSR4B_RX_CH3N
A47	GTSR4B_TX_CH0P	B47	GND	C47	GTSR4B_TX_CH2P	D47	GND
A48	GTSR4B_TX_CH0N	B48	GND	C48	GTSR4B_TX_CH2N	D48	GND
A49	GND	B49	GTSR4B_TX_CH1P	C49	GND	D49	GTSR4B_TX_CH3P
A50	GND	B50	GTSR4B_TX_CH1N	C50	GND	D50	GTSR4B_TX_CH3N
A51	REFCLK_GTSR4C_CH1P	B51	GND	C51	REFCLK_GTSR4C_RX_P	D51	GND
A52	REFCLK_GTSR4C_CH1N	B52	GND	C52	REFCLK_GTSR4C_RX_N	D52	GND
A53	GND	B53	GTSR4C_RX_CH1P	C53	GND	D53	GTSR4C_RX_CH3P
A54	GND	B54	GTSR4C_RX_CH1N	C54	GND	D54	GTSR4C_RX_CH3N
A55	GTSR4C_RX_CH0P	B55	GND	C55	GTSR4C_RX_CH2P	D55	GND
A56	GTSR4C_RX_CH0N	B56	GND	C56	GTSR4C_RX_CH2N	D56	GND
A57	GND	B57	GTSR4C_TX_CH1P	C57	GND	D57	GTSR4C_TX_CH3P
A58	GND	B58	GTSR4C_TX_CH1N	C58	GND	D58	GTSR4C_TX_CH3N
A59	GTSR4C_TX_CH0P	B59	GND	C59	GTSR4C_TX_CH2P	D59	GND
A60	GTSR4C_TX_CH0N	B60	GND	C60	GTSR4C_TX_CH2N	D60	GND

2.6.1 SDM Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Agilex 5 SDM is explained in the following section.

2.6.1.1 JTAG Interface

The Agilex 5 SOM supports JTAG interface on Board-to-Board Connector2. The JTAG interface is a multipurpose interface used for both boot and programming function. The Intel Agilex 5 SoC and FPGA ’s HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Intel Agilex 5 SoC and FPGA. These JTAG interface signals are at 1.8V Voltage level.

For more details on JTAG Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 15: JTAG Interface Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A9	SDM_TCK	TCK	SDM	CA109	I, 1.8V LVCMOS/ 1K, PD	JTAG Test Clock.
A12	SDM_TDI	TDI	SDM	BW112	I, 1.8V LVCMOS/ 10K, PU	JTAG Test Data Input.
A11	SDM_TDO	TDO	SDM	BW109	O, 1.8V LVCMOS	JTAG Test Data Output.
A10	SDM_TMS	TMS	SDM	CA112	I, 1.8V LVCMOS/ 10K, PU	JTAG Test Mode Select.

2.6.1.2 Active Serial Interface (Optional)

The Agilex 5 SoC FPGA SOM optionally supports the Active serial signals on Board-to-Board Connector2. The Active Serial controller of Agilex 5 SDM is used for AS interface through SDM IO pins. It can be used as the boot media for the first stage boot loader and storage. The same pins are utilized for supporting the HPS to FPGA SPI interface and so when Active Serial is supported, HPS to FPGA SPI will become optional.

For more details on Active Serial Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 16: Active Serial Interface Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D16	SDM_AS_CLK	SDM_IO2	SDM	BK99	O, 1.8V LVCMOS	NC. Optionally connected to Active Serial clock.
D17	SDM_AS_DATA0	SDM_IO4	SDM	BH99	IO, 1.8V LVCMOS	NC. Optionally connected to Active Serial Data0.
D18	SDM_AS_DATA1	SDM_IO1	SDM	BK102	IO, 1.8V LVCMOS	NC. Optionally connected to Active Serial Data1.
D19	SDM_AS_DATA2	SDM_IO3	SDM	CH99	IO, 1.8V LVCMOS	NC. Optionally connected to Active Serial Data2.
D20	SDM_AS_DATA3	SDM_IO6	SDM	CF102	IO, 1.8V LVCMOS	NC. Optionally connected to Active Serial Data3.
D21	SDM_AS_nCSO0/MSEL0	SDM_IO5	SDM	CF112	O, 1.8V LVCMOS	NC. Optionally connected to Active Serial Chip Select0.
D30	SDM_nCONFIG	NCONFIG	SDM	BU99	I, 1.8V LVCMOS/ 10K PU	NC. Optionally connected to SDM nConfig.

2.6.2 HPS Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Agilex 5 HPS is explained in the following section.

2.6.2.1 USB2.0 OTG Interface

The Agilex 5 SOM supports one USB2.0 OTG interface on Board-to-Board Connector2. USB OTG controller of Agilex 5 HPS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the HPS IO pins. The Agilex 5 SOM supports "USB3320" ULPI transceiver from Microchip and works at 1.8V IO voltage level. It supports active high power enable signal on Board-to-Board Connector2 from USB PHY for external VBUS power control.

Also, Agilex 5 SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 17: USB 2.0 Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A17	USB_OTG_DP	NA	NA	NA	IO, USB	USB OTG data Positive.
A16	USB_OTG_DM	NA	NA	NA	IO, USB	USB OTG data negative.
B17	USB_OTG_ID	NA	NA	NA	I,3.3V CMOS	USB OTG ID input for USB host or device detection.
B16	USB_PWR_EN	NA	NA	NA	O, 3.3V CMOS	USB active high power enable output to control external USB Vbus.
B18	VBUS_USB	NA	NA	NA	I, 5V Power	USB VBUS for VBUS monitoring.

2.6.2.2 RGMII Interface

The Agilex 5 SOM supports RGMII interface on Board-to-Board Connector2. This RGMII is interface with EMAC2 interface of Agilex 5 HPS pins and works at 1.8V IO voltage level. These RGMII signals are directly connected from Agilex 5 SoC FPGA to Board-to-Board Connector2.

The Agilex 5 Gigabit Ethernet controller (EMAC2) implements a 10/100/1000 Mb/s Ethernet MAC that is compatible with the IEEE Standard for Ethernet (IEEE Std 802.3-2008). The EMAC controller also supports MDIO interface for external PHY Management and it can be used through the HPS IOs in SOM.

For more details on RGMII Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 18: EMAC2 Board to Board Connector2 Pinouts

B2B-1 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C16	HPS_EMAC2_TX_CLK	HPS_IOB_13	HPS	M127	O, 1.8V LVCMOS	EMAC2 RGMII Transmit Clock.
C17	HPS_EMAC2_TXD0	HPS_IOB_17	HPS	K124	O, 1.8V LVCMOS	EMAC2 RGMII Transmit DATA0.
C18	HPS_EMAC2_TXD1	HPS_IOB_18	HPS	Y127	O, 1.8V LVCMOS	EMAC2 RGMII Transmit DATA1.
C19	HPS_EMAC2_TXD2	HPS_IOB_21	HPS	F127	O, 1.8V LVCMOS	EMAC2 RGMII Transmit DATA2.
C20	HPS_EMAC2_TXD3	HPS_IOB_22	HPS	Y124	O, 1.8V LVCMOS	EMAC2 RGMII Transmit DATA3.
C21	HPS_EMAC2_TX_CTL	HPS_IOB_14	HPS	K127	O, 1.8V LVCMOS	EMAC2 RGMII Transmit Control.
C23	HPS_EMAC2_RX_CLK	HPS_IOB_15	HPS	M124	I, 1.8V LVCMOS	EMAC2 RGMII Receive Clock.
C24	HPS_EMAC2_RXD0	HPS_IOB_19	HPS	H127	I, 1.8V LVCMOS	EMAC2 RGMII Receive DATA0
C25	HPS_EMAC2_RXD1	HPS_IOB_20	HPS	AB124	I, 1.8V LVCMOS	EMAC2 RGMII Receive DATA1.
C26	HPS_EMAC2_RXD2	HPS_IOB_23	HPS	F124	I, 1.8V LVCMOS	EMAC2 RGMII Receive DATA2.
C27	HPS_EMAC2_RXD3	HPS_IOB_24	HPS	D124	I, 1.8V LVCMOS	EMAC2 RGMII Receive DATA3.
C28	HPS_EMAC2_RX_CTL	HPS_IOB_16	HPS	AB127	I, 1.8V LVCMOS	EMAC2 RGMII Receive control.
C12	HPS_EMAC2_SCL	HPS_IOB_10	HPS	Y132	O, 1.8V LVCMOS	MDC Clock Output
C13	HPS_EMAC2_SDA	HPS_IOB_9	HPS	T127	IO, 1.8V LVCMOS	MDIO Data In/Out

2.6.2.3 Debug UART Interface

The Agilex 5 SOM supports one Debug UART interface on Board-to-Board Connector2. The UART1 controller of Agilex 5 HPS is used for Debug UART interface through HPS IO pins. This controller supports full-duplex asynchronous receiver and transmitter that support a wide range of programmable baud rates.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

Table 19:Debug UART Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A14	HPS_UART1_RX	HPS_IOA_8	HPS	AG115	I, 1.8V LVCMOS	UART1 Receive data line for Debug.
A13	HPS_UART1_TX	HPS_IOA_7	HPS	R134	O, 1.8V LVCMOS	UART1 Transmit data line for Debug.

2.6.2.4 Data UART Interface

The Agilex 5 SOM supports one Data UART interface on Board-to-Board Connector2. The UART01 controller of Agilex 5 HPS is used for UART interface through HPS IO pins. This controller supports full-duplex asynchronous receiver and transmitter and flow control signals that support a wide range of programmable baud rates.

For more details on UART pinouts on Board-to-Board Connector2, refer the below table.

Table 20:Data UART Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D23	HPS_UART0_TX	HPS_IOA_3	HPS	W134	O, 1.8V LVCMOS	UART0 Receive data
D24	HPS_UART0_RX	HPS_IOA_4	HPS	AK115	I, 1.8V LVCMOS	UART0 Transmit data
D26	HPS_UART0_RTS	HPS_IOA_2	HPS	U135	O, 1.8V LVCMOS	UART0 Request to send data
D25	HPS_UART0_CTS	HPS_IOA_1	HPS	W135	I, 1.8V LVCMOS	UART0 Clear to send data

2.6.2.5 I2C Interface

The Agilex 5 SOM supports one I2C interface on Board-to-Board Connector2. The I2C0 module of Agilex 5 HPS is used for I2C interface through HPS IO pins. The controller supports multi-master mode for 7-bit and extended 10-bit addressing and also supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C interface is also connected to On-SOM PMIC with I2C address 0x58 and also connected with Clock Synthesizer with I2C address of 0x74 in the Agilex 5 SOM.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 21: I2C Interface Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C8	HPS_I2C0_SCL_1V8	HPS_IOA_6	HPS	AL120	O, 1.8V OD/ 4.7K PU	I2C Serial Clock.
C9	HPS_I2C0_SDA_1V8	HPS_IOA_5	HPS	U134	IO, 1.8V OD/ 4.7K PU	I2C Serial Data.

2.6.2.6 SD/SDIO Interface (Optional)

The Agilex 5 SOM optionally supports SD/SDIO interface on Board-to-Board Connector2. The SD1 controller of Agilex 5 SoC FPGA is used for SD/SDIO interface through HPS pins. By default, these signals are used for supporting On board eMMC and as a result the SDIO interface on the Board to Board Connector can be supported only when eMMC is unused. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (25MHz), High Speed mode (50MHz), SDR12 (25MHz), SDR25 (50MHz), SDR50 (100MHz), SDR104 (200MHz) & DDR50 mode (50MHz). Also in SD mode, data transfers in 1-bit and 4-bit modes. The Agilex 5 SOM supports Card Detect & Power Enable/Voltage Select pins through HPS IO pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 22: SD/SDIO Interface Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B23	SD_CLK(GPIO1_12)	HPS_IOB_3	HPS	D132	O, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD Clock.
B24	SD_CMD(GPIO1_07)	HPS_IOB_8	HPS	AB132	IO, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD Command.
B25	SD_DATA0(GPIO1_00)	HPS_IOB_1	HPS	E135	IO, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD DATA0.
B26	SD_DATA1(GPIO1_01)	HPS_IOB_2	HPS	F132	IO, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD DATA1.
B27	SD_DATA2(GPIO1_05)	HPS_IOB_6	HPS	AA135	IO, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD DATA2.
B28	SD_DATA3(GPIO1_06)	HPS_IOB_7	HPS	V127	IO, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD DATA3.
B29	SD_CD(GPIO1_18)	HPS_IOA_9	HPS	N135	I, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD Card Detect.
C14	SD_WP(GPIO1_19)	HPS_IOA_10	HPS	AK120	I, 1.8V LVCMOS/ 10K PU	By default, NC. Optionally connected to SD Write Protect.
B21	SD_PWR_EN(GPIO1_20)	HPS_IOB_11	HPS	T124	O, 1.8V LVCMOS 10K PU	By default, NC. Optionally connected to SD Power Enable/Voltage select through HPS GPIO.

2.6.3 HPS to FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Agilex 5 SDM is explained in the following section.

2.6.3.1 Gigabit Ethernet Interface

The Agilex 5 SOM supports one 10/100/1000/2500 Mbps Ethernet interface on Board-to-Board Connector2. The SGMII MAC is integrated in the Agilex 5 HPS to FPGA and connected to the external Gigabit Ethernet PHY "QCA8081" on SOM. This Gigabit Ethernet PHY is interfaced with Transceiver Bank 1C Channel3 interface of Agilex 5 SoC FPGA.

In Agilex 5 SOM, HVIO 6B Bank IO3 is used for Ethernet PHY reset. Also, SOM supports Ethernet PHY interrupt and Wake-on-Lan through HVIO 6B Bank IO1 and IO2 respectively This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics and connector are required on the carrier board.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 23: Ethernet Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A20	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
A19	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
A23	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
A22	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
A26	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
A25	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
A29	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
A28	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
B19	GPHY_ACTIVITY_LED1	NA	NA	NA	O, GBE	Gigabit Ethernet Activity LED (Active High).
B20	GPHY_LINK_LED2	NA	NA	NA	O, GBE	Gigabit Ethernet 1000Mbps Link status LED (Active High).

2.6.3.2 I2C Interface

The Agilex 5 SOM supports one I2C interface on Board-to-Board Connector2. The I2C1 module of Agilex 5 HPS is used for I2C1 interface through HVIO 6A bank pins by having the controller internally routed from HPS to FPGA. The controller supports multi-master mode for 7-bit and extended 10-bit addressing and also supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C interface is also optionally connected to On-SOM PMIC with I2C address 0x58 and Clock Synthesizer with I2C address of 0x74 in the Agilex 5 SOM.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 24: I2C Interface Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C10	H2F_I2C1_SCL_1V8	HVIO_6A_14	HVIO_ 6A	BU22	O, 1.8V OD/ 4.7K PU	I2C Serial Clock.
C11	H2F_I2C1_SDA_1V8	HVIO_6A_13	HVIO_ 6A	CH12	IO, 1.8V OD/ 4.7K PU	I2C Serial Data.

2.6.3.3 SPI Interface

The Agilex 5 SoC FPGA SOM supports the SPI1 signals on Board-to-Board Connector2. The SPI1 module of Agilex 5 HPS is used for the SPI interface through HVIO 6A bank pins by having the controller internally routed from HPS to FPGA.

For more details on SPI Interface pinouts on Board-to-Board Connector2, refer the below table.

Table 25: SPI Interface Board to Board Connector2 Pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D16	H2F_SPI1_SCK	HVIO_6A_17	HVIO_6A	BM22	O, 1.8V LVCMOS	HPS to FPGA SPI Clock
D17	H2F_SPI1_MOSI	HVIO_6A_15	HVIO_6A	BW19	O, 1.8V LVCMOS	HPS to FPGA SPI Data Out
D18	H2F_SPI1_MISO	HVIO_6A_16	HVIO_6A	BH28	I, 1.8V LVCMOS	HPS to FPGA SPI Data In
D20	H2F_SPI1_CS1_1V8	HVIO_6A_19	HVIO_6A	BK19	O, 1.8V LVCMOS	HPS to FPGA SPI Chip Select 1
D21	H2F_SPI1_CS0_1V8	HVIO_6A_18	HVIO_6A	CF12	O, 1.8V LVCMOS	HPS to FPGA SPI Chip Select 0

2.6.4 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Agilex 5, FPGA is explained in the following section.

2.6.4.1 High Speed Transceivers

The Intel Agilex 5 SoC and FPGA SOM supports 12 high speed transceiver channels from GTSR Bank 1B, GTSL Bank 4B and GTSL Bank 4C (4 channels from each bank). These Transceivers connected to Board-to-Board Connector2 are capable of running up to a maximum speed of 28Gbps in NRZ Format. These transceivers can be used to interface to multiple high-speed interface protocols. Each 4 Channel Transceiver Bank supports two reference clock input pairs.

Table 26: Transceiver Bank 1B, 4B and 4C Pinouts

B2B-2 Pin No	B2B-2 Signal Name	Soc Pin Name	Soc Bank	Soc Pin No	Signal Type/Termination	Description
Transceiver Bank 1B						
A36	GTSL1B_RX_CH0N	GTSL1B_RX_CH0N	1B	BD133	I, DIFF	GTSL Bank1B Channel 0 differential Receiver Negative
A35	GTSL1B_RX_CH0P	GTSL1B_RX_CH0P	1B	BD135	I, DIFF	GTSL Bank1B Channel 0 differential Receiver Positive
A40	GTSL1B_TX_CH0N	GTSL1B_TX_CH0N	1B	BE126	O, DIFF	GTSL Bank1B Channel 0 differential Transmitter Negative
A39	GTSL1B_TX_CH0P	GTSL1B_TX_CH0P	1B	BE129	O, DIFF	GTSL Bank1B Channel 0 differential Transmitter Positive
B34	GTSL1B_RX_CH1N	GTSL1B_RX_CH1N	1B	BB133	I, DIFF	GTSL Bank1B Channel 1 differential Receiver Negative
B33	GTSL1B_RX_CH1P	GTSL1B_RX_CH1P	1B	BB135	I, DIFF	GTSL Bank1B Channel 1 differential Receiver Positive
B38	GTSL1B_TX_CH1N	GTSL1B_TX_CH1N	1B	BC126	O, DIFF	GTSL Bank1B Channel 1 differential Transmitter Negative
B37	GTSL1B_TX_CH1P	GTSL1B_TX_CH1P	1B	BC129	O, DIFF	GTSL Bank1B Channel 1 differential Transmitter Positive
C36	GTSL1B_RX_CH2N	GTSL1B_RX_CH2N	1B	AY133	I, DIFF	GTSL Bank1B Channel 2 differential Receiver Negative
C35	GTSL1B_RX_CH2P	GTSL1B_RX_CH2P	1B	AY135	I, DIFF	GTSL Bank1B Channel 2 differential Receiver Positive
C40	GTSL1B_TX_CH2N	GTSL1B_TX_CH2N	1B	BA126	O, DIFF	GTSL Bank1B Channel 2 differential Transmitter Negative
C39	GTSL1B_TX_CH2P	GTSL1B_TX_CH2P	1B	BA129	O, DIFF	GTSL Bank1B Channel 2 differential Transmitter Positive
D34	GTSL1B_RX_CH3N	GTSL1B_RX_CH3N	1B	AV133	I, DIFF	GTSL Bank1B Channel 3 differential Receiver Negative
D33	GTSL1B_RX_CH3P	GTSL1B_RX_CH3P	1B	AV135	I, DIFF	GTSL Bank1B Channel 3 differential Receiver Positive
D38	GTSL1B_TX_CH3N	GTSL1B_TX_CH3N	1B	AW126	O, DIFF	GTSL Bank1B Channel 3 differential Transmitter Negative

B2B-2 Pin No	B2B-2 Signal Name	Soc Pin Name	Soc Bank	Soc Pin No	Signal Type/Termination	Description
D37	GTSL1B_TX_CH3P	GTSL1B_TX_CH3P	1B	AW129	O, DIFF	GTSL Bank1B Channel 3 differential Transmitter Positive
C32	REFCLK_GTSL1B_RX_N	REFCLK_GTSL1B_RX_N	1B	AY115	I, DIFF	GTSL Bank1B Reference clock Negative
C31	REFCLK_GTSL1B_RX_P	REFCLK_GTSL1B_RX_P	1B	AY120	I, DIFF	GTSL Bank1B Reference clock Positive
A32	REFCLK_GTSL1B_CH1N	REFCLK_GTSL1B_CH1N	1B	AV115	I, DIFF	GTSL Bank1B Reference clock Negative
A31	REFCLK_GTSL1B_CH1P	REFCLK_GTSL1B_CH1P	1B	AV120	I, DIFF	GTSL Bank1B Reference clock Positive
Transceiver Bank 4B						
A44	GTSR4B_RX_CH0N	GTSR4B_RX_CH0N	4B	BF3	I, DIFF	GTSR Bank4B Channel 0 differential Receiver Negative
A43	GTSR4B_RX_CH0P	GTSR4B_RX_CH0P	4B	BF1	I, DIFF	GTSR Bank4B Channel 0 differential Receiver Positive
A48	GTSR4B_TX_CH0N	GTSR4B_TX_CH0N	4B	BE10	O, DIFF	GTSR Bank4B Channel 0 differential Transmitter Negative
A47	GTSR4B_TX_CH0P	GTSR4B_TX_CH0P	4B	BE7	O, DIFF	GTSR Bank4B Channel 0 differential Transmitter Positive
B46	GTSR4B_RX_CH1N	GTSR4B_RX_CH1N	4B	BD3	I, DIFF	GTSR Bank4B Channel1 differential Receiver Negative
B45	GTSR4B_RX_CH1P	GTSR4B_RX_CH1P	4B	BD1	I, DIFF	GTSR Bank4B Channel1 differential Receiver Positive
B50	GTSR4B_TX_CH1N	GTSR4B_TX_CH1N	4B	BC10	O, DIFF	GTSR Bank4B Channel1 differential Tranmitter Negative
B49	GTSR4B_TX_CH1P	GTSR4B_TX_CH1P	4B	BC7	O, DIFF	GTSR Bank4B Channel1 differential Transmitter Positive
C44	GTSR4B_RX_CH2N	GTSR4B_RX_CH2N	4B	BB3	I, DIFF	GTSR Bank4B Channel2 differential Receiver Negative
C43	GTSR4B_RX_CH2P	GTSR4B_RX_CH2P	4B	BB1	I, DIFF	GTSR Bank4B Channel2 differential Receiver Positive
C48	GTSR4B_TX_CH2N	GTSR4B_TX_CH2N	4B	BA10	O, DIFF	GTSR Bank4B Channel2 differential Transmitter Negative
C47	GTSR4B_TX_CH2P	GTSR4B_TX_CH2P	4B	BA7	O, DIFF	GTSR Bank4B Channel2 differential Transmitter Positive
D46	GTSR4B_RX_CH3N	GTSR4B_RX_CH3N	4B	AY3	I, DIFF	GTSR Bank4B Channel 3 differential Receiver Negative
D45	GTSR4B_RX_CH3P	GTSR4B_RX_CH3P	4B	AY1	I, DIFF	GTSR Bank4B Channel 3 differential Receiver Positive
D50	GTSR4B_TX_CH3N	GTSR4B_TX_CH3N	4B	AW10	O, DIFF	GTSR Bank4B Channel 3 differential Transmitter Negative
D49	GTSR4B_TX_CH3P	GTSR4B_TX_CH3P	4B	AW7	O, DIFF	GTSR Bank4B Channel 3 differential Transmitter Positive

B2B-2 Pin No	B2B-2 Signal Name	Soc Pin Name	Soc Bank	Soc Pin No	Signal Type/Termination	Description
D42	REFCLK_GTSR4B_RX_N	REFCLK_GTSR4B_RX_N	4B	AY21	I, DIFF	GTSR Bank4B Reference clock Negative
D41	REFCLK_GTSR4B_RX_P	REFCLK_GTSR4B_RX_P	4B	AY16	I, DIFF	GTSR Bank4B Reference clock positive
B42	REFCLK_GTSR4B_CH1N	REFCLK_GTSR4B_CH1N	4B	AV21	I, DIFF	GTSR Bank4B Channel 1 Reference clock Negative
B41	REFCLK_GTSR4B_CH1P	REFCLK_GTSR4B_CH1P	4B	AV16	I, DIFF	GTSR Bank4B Channel 1 Reference clock Positive
Transceiver Bank 4C						
A56	GTSR4C_RX_CH0N	GTSR4C_RX_CH0N	4C	AV3	I, DIFF	GTSR Bank4B Channel 0 differential Receiver Negative
A55	GTSR4C_RX_CH0P	GTSR4C_RX_CH0P	4C	AV1	I, DIFF	GTSR Bank4B Channel 0 differential Receiver Positive
A60	GTSR4C_TX_CH0N	GTSR4C_TX_CH0N	4C	AU10	O, DIFF	GTSR Bank4B Channel 0 differential Transmitter Negative
A59	GTSR4C_TX_CH0P	GTSR4C_TX_CH0P	4C	AU7	O, DIFF	GTSR Bank4B Channel 0 differential Transmitter Positive
B54	GTSR4C_RX_CH1N	GTSR4C_RX_CH1N	4C	AT3	I, DIFF	GTSR Bank4C Channel 1 differential Receiver Negative
B53	GTSR4C_RX_CH1P	GTSR4C_RX_CH1P	4C	AT1	I, DIFF	GTSR Bank4B Channel 1 differential Receiver Positive
B58	GTSR4C_TX_CH1N	GTSR4C_TX_CH1N	4C	AR10	O, DIFF	GTSR Bank4B Channel 1 differential Transmitter Negative
B57	GTSR4C_TX_CH1P	GTSR4C_TX_CH1P	4C	AR7	O, DIFF	GTSR Bank4B Channel 1 differential Transmitter Positive
B54	GTSR4C_RX_CH1N	GTSR4C_RX_CH1N	4C	AT3	I, DIFF	GTSR Bank4C Channel 1 differential Receiver Negative
C56	GTSR4C_RX_CH2N	GTSR4C_RX_CH2N	4C	AP3	I, DIFF	GTSR Bank4C Channel 2 differential Receiver Negative
C55	GTSR4C_RX_CH2P	GTSR4C_RX_CH2P	4C	AP1	I, DIFF	GTSR Bank4B Channel 2 differential Receiver Positive
C60	GTSR4C_TX_CH2N	GTSR4C_TX_CH2N	4C	AN10	O, DIFF	GTSR Bank4B Channel 2 differential Transmitter Negative
C59	GTSR4C_TX_CH2P	GTSR4C_TX_CH2P	4C	AN7	O, DIFF	GTSR Bank4B Channel 2 differential Transmitter Positive
D54	GTSR4C_RX_CH3N	GTSR4C_RX_CH3N	4C	AM3	I, DIFF	GTSR Bank4B Channel 3 differential Receiver Negative
D53	GTSR4C_RX_CH3P	GTSR4C_RX_CH3P	4C	AM1	I, DIFF	GTSLR Bank4B Channel 3 differential Receiver Positive
D58	GTSR4C_TX_CH3N	GTSR4C_TX_CH3N	4C	AL10	O, DIFF	GTSR Bank4B Channel 3 differential Transmitter Negative
D57	GTSR4C_TX_CH3P	GTSR4C_TX_CH3P	4C	AL7	O, DIFF	GTSR Bank4B Channel 3 differential Transmitter Positive

B2B-2 Pin No	B2B-2 Signal Name	Soc Pin Name	Soc Bank	Soc Pin No	Signal Type/Termination	Description
C52	REFCLK_GTSR4C_RX_N	REFCLK_GTSR4C_RX_N	4C	AT21	I, DIFF	GTSR Bank4B Reference clock Negative
C51	REFCLK_GTSR4C_RX_P	REFCLK_GTSR4C_RX_P	4C	AT16	I, DIFF	GTSR Bank4B Reference clock positive
A52	REFCLK_GTSR4C_CH1N	REFCLK_GTSR4C_CH1N	4C	AP21	I, DIFF	GTSR Bank4B Channel1 Reference Clock
A51	REFCLK_GTSR4C_CH1P	REFCLK_GTSR4C_CH1P	4C	AP16	I, DIFF	GTSR Bank4B Channel1 Reference Clock

2.6.5 Power, Reset & Control Signals

The Agilex 5 SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (pin B8) in Board-to-Board Connector2. Also, in Board-to-Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Agilex 5 SOM supports VCC_RTC coin cell power input from Board-to-Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

Table 27: Board to Board connector2 Control & Power Pins

B2B-2 Pin No	B2B Connector2 Pin Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B8	SOM_PWR_EN	NA	NA	NA	I, 5V	Active High SOM power enable. *Important Note:* *High – SOM power ON* *Low – SOM Power OFF*
B10	HPS_RESET_OUT(GPIO1_3)	HPS_IOB_4	HPS	AG123	O, 1.8V LVCMOS	Reset Pin
B11	SDM_HPS_nRESET	SDM_IO13	SDM	BW102	I, 3.3V 10K PU	Active low reset input.
B30	HS_PCIe_RSTN	HVIO_5B_6	5B	BU109	IO, 1.8V LVCMOS/ 10K PU	PCIe Reset for EP Mode.
B13	MSIO_PWRBTN#	NA	NA	NA	I, 3.3V 10K PU	NC Optionally connected to PMIC PWRON Pin
B12	SDM_AS_CONFIG_DONE	SDM_IO16	SDM	BP102	O, 1.8V LVCMOS/ 10K PU	Configuration done pin.
D12	SDM_AS_nCSO0/ MSEL0	SDM_IO5	SDM	CF112	I, 1.8V LVCMOS 10K PU	Boot Mode0 Select pin
D13	SDM_MSEL1	SDM_IO7	SDM	BM99	I, 1.8V LVCMOS 10K PU	Boot Mode1 Select pin
D14	SDM_MSEL2	SDM_IO9	SDM	BM102	I, 1.8V LVCMOS 10K PU	Boot Mode2 Select pin
D9	VRTC_3V0	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.

B2B-2 Pin No	B2B Connector2 Pin Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A1, A2, A3, A4, A5 B1, B2, B3, B4, B5 C1, C2, C3, C4, C5 D1, D2, D3, D4, D5	VCC_5V	NA	NA	NA	I, 5V	Supply Voltage.
A6, A7, A15, A18, A21, A24, A27, A30, A33, A34, A37, A38, A41, A42, A45, A46, A49, A50, A53, A54, A57, A58, B6, B7, B15, B22, B31, B32, B35, B36, B39, B40, B43, B44, B47, B48, B51, B52, B55, B56, B59,B60, C6, C7, C15, C22, C30, C33, C34, C37, C38, C41, C42, C45, C46, C49, C50, C53, C54,C57, C58, D6, D7, D15, D22, D31, D32, D35, D36, D39, D40, D43, D44, D47, D48, D51, D52, D55, D56, D59, D60	GND	NA	NA	NA	Power	Ground

2.7 Board to Board Connector3

The Agilex 5 SOM Board to Board Connector3 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector3 are explained in the following sections. The Board-to-Board Connector3 (J7) is physically located on bottom side of the SOM as shown below.

Number of Pins - 160

Connector Part Number - ADM6-40-01.5-L-4-2-A-TR from Samtech

Mating Connector - ADF6-40-03.5-L-4-2-A-TR from Samtech

Staking Height - 5mm

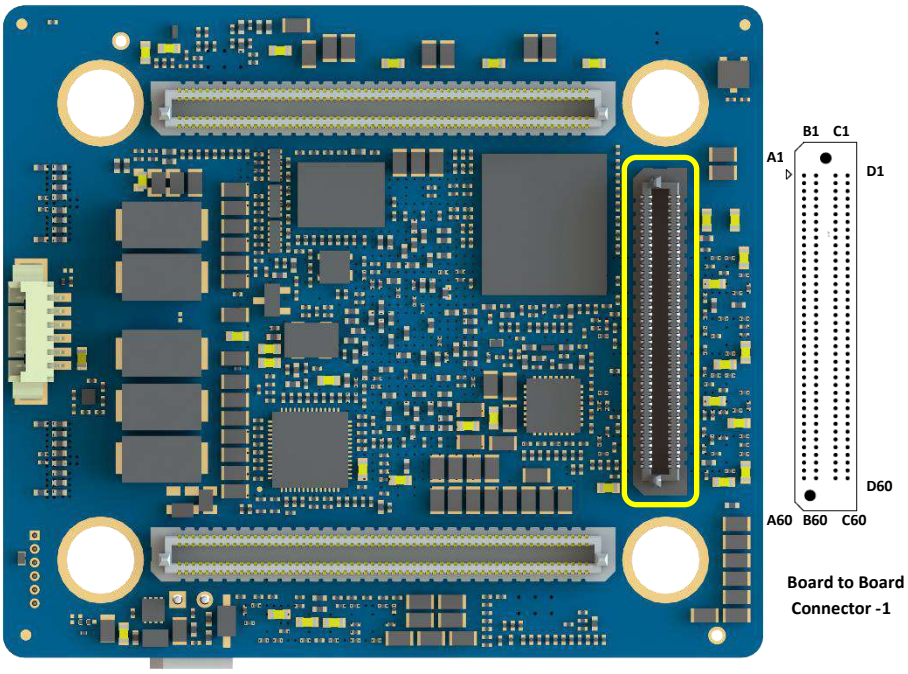

Figure 5: Board to Board Connector 3

Table 28: : Board to Board Connector3 Pinout

B2B-1 Pin	Signal Name	B2B-3 Pin	Signal Name	B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name
A1	GND	B1	GTSL1A_TX_CH3N	C1	GND	D1	REFCLK_GTSR4A_RX_P
A2	GND	B2	GTSL1A_TX_CH3P	C2	GND	D2	REFCLK_GTSR4A_RX_N
A3	GTSL1A_TX_CH2N	B3	GND	C3	REFCLK_GTSL1A_RX_P	D3	GND
A4	GTSL1A_TX_CH2P	B4	GND	C4	REFCLK_GTSL1A_RX_N	D4	GND
A5	GND	B5	GTSL1A_TX_CH0N	C5	GND	D5	NCATTRIP_1V8
A6	GND	B6	GTSL1A_TX_CH0P	C6	GND	D6	ETH_TOD_IN
A7	GTSL1A_TX_CH1N	B7	GND	C7	REFCLK_GTSL1A_CH1P	D7	GND
A8	GTSL1A_TX_CH1P	B8	GND	C8	REFCLK_GTSL1A_CH1N	D8	GND
A9	GND	B9	GTSR4A_TX_CH2N	C9	GND	D9	REFCLK_GTSR4A_CH1P
A10	GND	B10	GTSR4A_TX_CH2P	C10	GND	D10	REFCLK_GTSR4A_CH1N
A11	GTSR4A_TX_CH3N	B11	GND	C11	FPGA_1PPS_OUT	D11	GND
A12	GTSR4A_TX_CH3P	B12	GND	C12		D12	GND
A13	GND	B13	GTSR4A_TX_CH0N	C13	GND	D13	VCC_1V8_G3_5B_6D_IO
A14	GND	B14	GTSR4A_TX_CH0P	C14	FPGA_BE111_HVIO_5B_11	D14	FPGA_BF11_HVIO_5B_1
A15	GTSR4A_TX_CH1N	B15	GND	C15	FPGA_BM109_HVIO_5B_12	D15	FPGA_BH109_HVIO_5B_2
A16	GTSR4A_TX_CH1P	B16	GND	C16	FPGA_BR112_HVIO_5B_13	D16	FPGA_BE115_HVIO_5B_3
A17	GND	B17	GTSL1A_RX_CH2P	C17	FPGA_BK118_HVIO_5B_14	D17	FPGA_BF115_HVIO_5B_4
A18	GND	B18	GTSL1A_RX_CH2N	C18	FPGA_BM118_HVIO_5B_15	D18	FPGA_BF107_HVIO_5B_5
A19	GTSL1A_RX_CH3P	B19	GND	C19	FPGA_BP112_HVIO_5B_16	D19	FPGA_BR109_HVIO_5B_8
A20	GTSL1A_RX_CH3N	B20	GND	C20	GND	D20	GND
A21	GND	B21	GTSL1A_RX_CH0P	C21	FPGA_B14_HVIO_6D_5	D21	FPGA_BM112_HVIO_5B_17
A22	GND	B22	GTSL1A_RX_CH0N	C22	FPGA_A14_HVIO_6D_6	D22	FPGA_BK112_HVIO_5B_18
A23	GTSL1A_RX_CH1P	B23	GND	C23	FPGA_BK109_HVIO_5B_10/REFCLK2	D23	FPGA_A8_HVIO_6D_1
A24	GTSL1A_RX_CH1N	B24	GND	C24	NC	D24	FPGA_B4_HVIO_6D_2
A25	GND	B25	SDM_ADC_VSIGP_1	C25	FPGA_B20_HVIO_6D_10/REFCLK2	D25	FPGA_A11_HVIO_6D_3
A26	GND	B26	SDM_ADC_VSIGN_1	C26	NC	D26	FPGA_B11_HVIO_6D_4
A27	SDM_ADC_VSIGP_0	B27	GND	C27	GND	D27	GND
A28	SDM_ADC_VSIGN_0	B28	GND	C28	FPGA_B23_HVIO_6D_11	D28	FPGA_BE107_HVIO_5B_9/REFCLK1
A29	GND	B29	GTSR4A_RX_CH3P	C29	FPGA_B26_HVIO_6D_12	D29	FPGA_BF29_HVIO_6B_9/REFCLK1
A30	GND	B30	GTSR4A_RX_CH3N	C30	FPGA_B30_HVIO_6D_13	D30	FPGA_A23_HVIO_6D_9/REFCLK1
A31	GTSR4A_RX_CH2P	B31	GND	C31	FPGA_A30_HVIO_6D_14	D31	NC
A32	GTSR4A_RX_CH2N	B32	GND	C32	FPGA_A35_HVIO_6D_15	D32	FPGA_A20_HVIO_6D_7
A33	GND	B33	GTSR4A_RX_CH1P	C33	FPGA_A33_HVIO_6D_16	D33	FPGA_A17_HVIO_6D_8
A34	GND	B34	GTSR4A_RX_CH1N	C34	GND	D34	GND
A35	GTSR4A_RX_CH0P	B35	GND	C35	NC	D35	FPGA_A39_HVIO_6D_17
A36	GTSR4A_RX_CH0N	B36	GND	C36	NC	D36	FPGA_B35_HVIO_6D_18
A37	GND	B37	FPGA_BE29_HVIO_6B_5	C37	NC	D37	FPGA_B34_HVIO_6D_19
A38	NC	B38	LS_PCIe_1C_RSTN_IN	C38	NC	D38	FPGA_B39_HVIO_6D_20
A39	NC	B39	HS_PCIe_1B_RSTN_IN	C39	NC	D39	NC
A40	GND	B40	VCC_1V8_G3	C40	NC	D40	NC

2.7.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector3 of Agilex 5 SoC FPGA SOM, FPGA section is explained in the following section.

2.7.1.1 FPGA HVIOs – HVIO Bank 5B

The Agilex 5 SOM supports 16 Single Ended (SE) IOs on Board-to-Board Connector3 from HVIO Bank 5B. Upon these 16 SE IOs, two can be used as reference clocks. Both are directly connected to Board-to-Board Connector3.

The IO voltage of HVIO 5B is connected from LDO4 output of PMIC Regulator and it supports variable IO voltage setting. IO voltage is configured to 1.8V by default during power up. While using as Single Ended IOs, make sure to set the PMIC LDO4 output to appropriate IO voltage for Bank 5B. For more details about supported IO standard, refer the Agilex 5 datasheet.

For more details on HVIO Bank 5B pinouts on Board-to-Board Connector3, refer the below table.

Table 29: HVIO Bank 5A Pinouts

B2B-3 Pin No	B2B Connector3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D14	FPGA_BF11_HVIO_5B_1	HVIO_5B_1, SYSPLLREFCLK_L1A_2, TXCLK1, DATA_CTRL1	5B	BF111	I/O, 1.8V	HVIO Bank 5B_1 Single Ended IO Signal
D15	FPGA_BH109_HVIO_5B_2	HVIO_5B_2, SYSPLLREFCLK_L1A_3, TXCLK2, DATA_CTRL2	5B	BH109	I/O, 1.8V	HVIO Bank 5B_2 Single Ended IO Signal
D16	FPGA_BE115_HVIO_5B_3	HVIO_5B_3, SYSPLLREFCLK_L1B_2, TXCLK3, DATA_CTRL3	5B	BE115	I/O, 1.8V	HVIO Bank 5B_3 Single Ended IO Signal
D17	FPGA_BF115_HVIO_5B_4	HVIO_5B_4, SYSPLLREFCLK_L1B_3, TXCLK4, DATA_CTRL4	5B	BF115	I/O, 1.8V	HVIO Bank 5B_4 Single Ended IO Signal
D18	FPGA_BF107_HVIO_5B_5	HVIO_5B_5, PIN_PERST_N_CVP_L1A_1, TXCLK5, DATA_CTRL5	5B	BF107	I/O, 1.8V	HVIO Bank 5B_5 Single Ended IO Signal
D19	FPGA_BR109_HVIO_5B_8	HVIO_5B_8, TXCLK8, DATA_CTRL8	5B	BR109	I/O, 1.8V	HVIO Bank 5B_8 Single Ended IO Signal

B2B-3 Pin No	B2B Connector3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D28	FPGA_BE107_HVIO_5B_9 /REFCLK1	HVIO_5B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9	5B	BE107	I/O, 1.8V	HVIO Bank 5B_9 Single Ended IO Signal
C23	FPGA_BK109_HVIO_5B_10/REFCLK2	HVIO_5B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10	5B	BK109	I/O, 1.8V	HVIO Bank 5B_10 Single Ended IO Signal
C14	FPGA_BE111_HVIO_5B_11	HVIO_5B_11, SOURCE_SYNC_CLK 1, TXCLK11, RXCLK3, DATA_CTRL11	5B	BE111	I/O, 1.8V	HVIO Bank 5B_11 Single Ended IO Signal
C15	FPGA_BM109_HVIO_5B_12	HVIO_5B_12, SOURCE_SYNC_CLK 2, TXCLK12, RXCLK4, DATA_CTRL12	5B	BM109	I/O, 1.8V	HVIO Bank 5B_12 Single Ended IO Signal
C16	FPGA_BR112_HVIO_5B_13	HVIO_5B_13, TXCLK13, DATA_CTRL13	5B	BR112	I/O, 1.8V	HVIO Bank 5B_13 Single Ended IO Signal
C17	FPGA_BK118_HVIO_5B_14	HVIO_5B_14, TXCLK14, DATA_CTRL14	5B	BK118	I/O, 1.8V	HVIO Bank 5B_14 Single Ended IO Signal
C18	FPGA_BM118_HVIO_5B_15	HVIO_5B_15, TXCLK15, DATA_CTRL15	5B	BM118	I/O, 1.8V	HVIO Bank 5B_15 Single Ended IO Signal
C19	FPGA_BP112_HVIO_5B_16	HVIO_5B_16, TXCLK16, DATA_CTRL16	5B	BP112	I/O, 1.8V	HVIO Bank 5B_16 Single Ended IO Signal
D21	FPGA_BM112_HVIO_5B_17	HVIO_5B_17, TXCLK17, DATA_CTRL17	5B	BM112	I/O, 1.8V	HVIO Bank 5B_17 Single Ended IO Signal
D22	FPGA_BK112_HVIO_5B_18	HVIO_5B_18, TXCLK18, DATA_CTRL18	5B	BK112	I/O, 1.8V	HVIO Bank 5B_18 Single Ended IO Signal

2.7.1.2 FPGA HVIOs – HVIO Bank 6B & 6D

The Agilex 5 SOM supports 20 Single Ended (SE) IOs on Board-to-Board Connector3 from HVIO Bank 6D and 2 Single Ended (SE) IOs from HVIO Bank 6B. Upon these SE IOs, up to 3 are Reference Clocks.

The IO voltage of HVIO Bank 6D is connected from LDO4 output of the PMIC Regulator, and it fixed to 1.8V. Likewise, the IO Voltage of HVIO Bank 6B is connected from Buck4 output of the PMIC Regulator set to 1.8V during bootup. While using these Single Ended IOs, make sure to set the PMIC output to appropriate IO voltage. For more details about supported IO standard, refer the Agilex 5 datasheet.

In the Agilex 5 SOM HVIO Bank 6B and 6D signals are routed as Single Ended (SE) IOs to Board-to-Board Connector3. The Board-to-Board Connector3 pins D29, D30 and C25 are Reference Clock capable pins.

Table 30: HVIO Bank 6B and 6D

B2B-3 Pin No	B2B Connector3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
HVIO Bank 6D						
D23	FPGA_A8_HVIO_6D_1	HVIO_6D_1, TXCLK1, DATA_CTRL1	6D	A8	I/O, 1.8V	HVIO Bank 6D_1 Single Ended IO Signal
D24	FPGA_B4_HVIO_6D_2	HVIO_6D_2, TXCLK2, DATA_CTRL2	6D	B4	I/O, 1.8V	HVIO Bank 6D_2 Single Ended IO Signal
D25	FPGA_A11_HVIO_6D_3	HVIO_6D_3, TXCLK3, DATA_CTRL3	6D	A11	I/O, 1.8V	HVIO Bank 6D_3 Single Ended IO Signal
D26	FPGA_B11_HVIO_6D_4	HVIO_6D_4, TXCLK4, DATA_CTRL4	6D	B11	I/O, 1.8V	HVIO Bank 6D_4 Single Ended IO Signal
C21	FPGA_B14_HVIO_6D_5	HVIO_6D_5, TXCLK5, DATA_CTRL5	6D	B14	I/O, 1.8V	HVIO Bank 6D_5 Single Ended IO Signal
C22	FPGA_A14_HVIO_6D_6	HVIO_6D_6, TXCLK6, DATA_CTRL6	6D	A14	I/O, 1.8V	HVIO Bank 6D_6 Single Ended IO Signal
D32	FPGA_A20_HVIO_6D_7	HVIO_6D_7, TXCLK7, DATA_CTRL7	6D	A20	I/O, 1.8V	HVIO Bank 6D_7 Single Ended IO Signal
D33	FPGA_A17_HVIO_6D_8	HVIO_6D_8, TXCLK8, DATA_CTRL8	6D	A17	I/O, 1.8V	HVIO Bank 6D_8 Single Ended IO Signal
D30	FPGA_A23_HVIO_6D_9/REFCLK1	HVIO_6D_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9	6D	A23	I/O, 1.8V	HVIO Bank 6D_9 Single Ended IO Signal
C25	FPGA_B20_HVIO_6D_10/REFCLK2	HVIO_6D_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10	6D	B20	I/O, 1.8V	HVIO Bank 6D_10 Single Ended IO Signal

B2B-3 Pin No	B2B Connector3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C28	FPGA_B23_HVIO_6D_11	HVIO_6D_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11	6D	B23	I/O, 1.8V	HVIO Bank 6D_11 Single Ended IO Signal
C29	FPGA_B26_HVIO_6D_12	HVIO_6D_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12	6D	B26	I/O, 1.8V	HVIO Bank 6D_12 Single Ended IO Signal
C30	FPGA_B30_HVIO_6D_13	HVIO_6D_13, TXCLK13, DATA_CTRL13	6D	B30	I/O, 1.8V	HVIO Bank 6D_13 Single Ended IO Signal
C31	FPGA_A30_HVIO_6D_14	HVIO_6D_14, TXCLK14, DATA_CTRL14	6D	A30	I/O, 1.8V	HVIO Bank 6D_14 Single Ended IO Signal
C32	FPGA_A35_HVIO_6D_15	HVIO_6D_15, TXCLK15, DATA_CTRL15	6D	A35	I/O, 1.8V	HVIO Bank 6D_15 Single Ended IO Signal
C33	FPGA_A33_HVIO_6D_16	HVIO_6D_16, TXCLK16, DATA_CTRL16	6D	A33	I/O, 1.8V	HVIO Bank 6D_16 Single Ended IO Signal
D35	FPGA_A39_HVIO_6D_17	HVIO_6D_17, TXCLK17, DATA_CTRL17	6D	A39	I/O, 1.8V	HVIO Bank 6D_17 Single Ended IO Signal
D36	FPGA_B35_HVIO_6D_18	HVIO_6D_18, TXCLK18, DATA_CTRL18	6D	B35	I/O, 1.8V	HVIO Bank 6D_18 Single Ended IO Signal
D37	FPGA_B34_HVIO_6D_19	HVIO_6D_19, TXCLK19, DATA_CTRL19	6D	D34	I/O, 1.8V	HVIO Bank 6D_19 Single Ended IO Signal
D38	FPGA_B39_HVIO_6D_20	HVIO_6D_20, TXCLK20, DATA_CTRL20	6D	B39	I/O, 1.8V	HVIO Bank 6D_20 Single Ended IO Signal
HVIO Bank 6B						
D29	FPGA_BF29_HVIO_6B_9/REFCLK1	HVIO_6B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9	6B	BF29	I/O, 1.8V	HVIO Bank 6B_9 Single ended IO Signal
B37	FPGA_BE29_HVIO_6B_5	HVIO_6B_5, PIN_PERST_N_R4A_1, TXCLK5, DATA_CTRL5	6B	BE29	I/O, 1.8V	HVIO Bank 6B_5 Single ended IO Signal

2.7.1.3 High Speed Transceivers

The Intel Agilex 5 SoC and FPGA SOM supports 8 high speed transceiver channels from GTSR Bank 1A and GTSL Bank 4A (4 channels from each bank). These Transceivers connected to Board-to-Board Connector3 are capable of running up to a maximum speed of 28Gbps in NRZ Format. These transceivers can be used to interface to multiple high-speed interface protocols. Each 4 Channel Transceiver Bank supports two reference clock input pairs.

Table 31: Transceiver Bank 1A, 4A Pinouts

B2B-3 Pin No	B2B Connector3 Signal Name	Soc Pin Name	Soc Bank	Soc Pin No	Signal Type/Termination	Description
Transceiver Bank 1A						
B22	GTSL1A_RX_CH0N	GTSL1A_RX_CH0N	1A	BV133	I, DIFF	GTSL Bank1A Channel 0 differential Receiver Negative
B21	GTSL1A_RX_CH0P	GTSL1A_RX_CH0P	1A	BV135	I, DIFF	GTSL Bank1A Channel 0 differential Receiver Positive
B5	GTSL1A_TX_CH0N	GTSL1A_TX_CH0N	1A	BY126	O, DIFF	GTSL Bank1A Channel 0 differential Transmitter Negative
B6	GTSL1A_TX_CH0P	GTSL1A_TX_CH0P	1A	BY129	O, DIFF	GTSL Bank1A Channel 0 differential Transmitter Positive
A24	GTSL1A_RX_CH1N	GTSL1A_RX_CH1N	1A	BN133	I, DIFF	GTSL Bank1A Channel 1 differential Receiver Negative
A23	GTSL1A_RX_CH1P	GTSL1A_RX_CH1P	1A	BN135	I, DIFF	GTSL Bank1A Channel 1 differential Receiver Positive
A7	GTSL1A_TX_CH1N	GTSL1A_TX_CH1N	1A	BT126	O, DIFF	GTSL Bank1A Channel 1 differential Transmitter Negative
A8	GTSL1A_TX_CH1P	GTSL1A_TX_CH1P	1A	BT129	O, DIFF	GTSL Bank1A Channel 1 differential Transmitter Positive
B18	GTSL1A_RX_CH2N	GTSL1A_RX_CH2N	1A	BJ133	I, DIFF	GTSL Bank1A Channel 2 differential Receiver Negative
B17	GTSL1A_RX_CH2P	GTSL1A_RX_CH2P	1A	BJ135	I, DIFF	GTSL Bank1A Channel 2 differential Receiver Positive
A3	GTSL1A_TX_CH2N	GTSL1A_TX_CH2N	1A	BL126	O, DIFF	GTSL Bank1A Channel 2 differential Transmitter Negative
A4	GTSL1A_TX_CH2P	GTSL1A_TX_CH2P	1A	BL129	O, DIFF	GTSL Bank1A Channel 2 differential Transmitter Positive
A20	GTSL1A_RX_CH3N	GTSL1A_RX_CH3N	1A	BF133	I, DIFF	GTSL Bank1A Channel 3 differential Receiver Negative
A19	GTSL1A_RX_CH3P	GTSL1A_RX_CH3P	1A	BF135	I, DIFF	GTSL Bank1A Channel 3 differential Receiver Positive
B1	GTSL1A_TX_CH3N	GTSL1A_TX_CH3N	1A	BG126	O, DIFF	GTSL Bank1A Channel 3 differential Transmitter Negative
B2	GTSL1A_TX_CH3P	GTSL1A_TX_CH3P	1A	BG129	O, DIFF	GTSL Bank1A Channel 3 differential Transmitter Positive

B2B-3 Pin No	B2B Connector3 Signal Name	Soc Pin Name	Soc Bank	Soc Pin No	Signal Type/Termination	Description
C8	REFCLK_GTSL1A_CH1N	REFCLK_GTSL1A_CH1N	1A	BB115	I, DIFF	GTSL Bank1A Reference clock Negative
C7	REFCLK_GTSL1A_CH1P	REFCLK_GTSL1A_CH1P	1A	BB120	I, DIFF	GTSL Bank1A Reference clock Positive
C4	REFCLK_GTSL1A_RX_N	REFCLK_GTSL1A_RX_N	1A	BC107	I, DIFF	GTSL Bank1A Reference clock Negative
C3	REFCLK_GTSL1A_RX_P	REFCLK_GTSL1A_RX_P	1A	BC111	I, DIFF	GTSL Bank1A Reference clock positive
Transceiver Bank 4C						
A36	GTSR4A_RX_CH0N	GTSR4A_RX_CH0N	4A	CB3	I, DIFF	GTSR Bank4A Channel 0 differential Receiver Negative
A35	GTSR4A_RX_CH0P	GTSR4A_RX_CH0P	4A	CB1	I, DIFF	GTSR Bank4A Channel 0 differential Receiver Positive
B13	GTSR4A_TX_CH0N	GTSR4A_TX_CH0N	4A	BY10	O, DIFF	GTSR Bank4A Channel 0 differential Transmitter Negative
B14	GTSR4A_TX_CH0P	GTSR4A_TX_CH0P	4A	BY7	O, DIFF	GTSR Bank4A Channel 0 differential Transmitter Positive
B34	GTSR4A_RX_CH1N	GTSR4A_RX_CH1N	4A	BV3	I, DIFF	GTSR Bank4A Channel 1 differential Receiver Negative
B33	GTSR4A_RX_CH1P	GTSR4A_RX_CH1P	4A	BV1	I, DIFF	GTSR Bank4A Channel 1 differential Receiver Positive
A15	GTSR4A_TX_CH1N	GTSR4A_TX_CH1N	4A	BT10	O, DIFF	GTSR Bank4A Channel 1 differential Transmitter Negative
A16	GTSR4A_TX_CH1P	GTSR4A_TX_CH1P	4A	BT7	O, DIFF	GTSR Bank4A Channel 1 differential Transmitter Positive
A32	GTSR4A_RX_CH2N	GTSR4A_RX_CH2N	4A	BN3	I, DIFF	GTSR Bank4A Channel 2 differential Receiver Negative
A31	GTSR4A_RX_CH2P	GTSR4A_RX_CH2P	4A	BN1	I, DIFF	GTSR Bank4A Channel 2 differential Receiver Positive
B9	GTSR4A_TX_CH2N	GTSR4A_TX_CH2N	4A	BL10	O, DIFF	GTSR Bank4A Channel 2 differential Transmitter Negative
B10	GTSR4A_TX_CH2P	GTSR4A_TX_CH2P	4A	BL7	O, DIFF	GTSR Bank4A Channel 2 differential Transmitter Positive
A11	GTSR4A_TX_CH3N	GTSR4A_TX_CH3N	4A	BG10	O, DIFF	GTSR Bank4A Channel 3 differential Transmitter Negative
A12	GTSR4A_TX_CH3P	GTSR4A_TX_CH3P	4A	BG7	O, DIFF	GTSR Bank4A Channel 3 differential Transmitter Positive
B30	GTSR4A_RX_CH3N	GTSR4A_RX_CH3N	4A	BJ3	I, DIFF	GTSR Bank4A Channel 3 differential Receiver Negative
B29	GTSR4A_RX_CH3P	GTSR4A_RX_CH3P	4A	BJ1	I, DIFF	GTSR Bank4A Channel 3 differential Receiver Positive
D10	REFCLK_GTSR4A_CH1N	REFCLK_GTSR4A_CH1N	4A	BB21	I, DIFF	GTSR Bank4A Reference clock Negative

B2B-3 Pin No	B2B Connector3 Signal Name	Soc Pin Name	Soc Bank	Soc Pin No	Signal Type/Termination	Description
D9	REFCLK_GTSR4A_CH1P	REFCLK_GTSR4A_CH1P	4A	BB16	I, DIFF	GTSR Bank4A Reference clock positive
D2	REFCLK_GTSR4A_RX_N	REFCLK_GTSR4A_RX_N	4A	BC25	I, DIFF	GTSR Bank4A Reference clock Negative
D1	REFCLK_GTSR4A_RX_P	REFCLK_GTSR4A_RX_P	4A	BC29	I, DIFF	GTSR Bank4A Reference clock positive

2.8 Agilex 5 HPS & SDM Pin Multiplexing on Board-to-Board Connectors

The Agilex 5 HPS & SDM IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of Agilex 5 HPS IO pins can be configured as GPIO if required. The below table provides the details of HPS pin connections on Agilex 5 CPU with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring HPS I/O configuration in the Quartus Tool. To know the complete available alternate functions, refer the HPS I/O configuration in the latest Quartus Tool

Table 32: HPS IOMUX on Agilex 5 SOM

Interface/ Function	B2B Connector Pin Number	Intel Agilex 5 SoC & FPGA Pin Name	Intel Agilex 5 SoC & FPGA Pin Number	GPIO	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9
On SOM Features from Intel Agilex 5 SoC HPS														
eMMC FLASH	NA	HPS_IOB_3	D132	GPIO1_IO2	EMAC1_RX_CLK		TRACE_D8	SDMMC_CLK	I2C0_SDA	UART0_TX		SPIM1_MISO	GPIO1_IO2	CM_HPS_OSC_CLK
	NA	HPS_IOB_8	AB132	GPIO1_IO7	EMAC1_RXD1	I3C0_SCL	TRACE_D15	SDMMC_CMD	I2C1_SCL	UART1_RX	SPIS1_MISO		GPIO1_IO7	CM_HPS_OSC_CLK
	NA	HPS_IOB_1	E135	GPIO1_IO0	EMAC1_TX_CLK		TRACE_D10	SDMMC_DATA0	EMAC0_PPS0	UART0_CTS_N		SPIM1_CLK	GPIO1_IO0	CM_HPS_OSC_CLK
	NA	HPS_IOB_2	F132	GPIO1_IO1	EMAC1_TX_CTL		TRACE_D9	SDMMC_DATA1	EMAC0_PPSTRIG0	UART0_RTS_N		SPIM1_MOSI	GPIO1_IO1	CM_HPS_OSC_CLK
	NA	HPS_IOB_6	AA135	GPIO1_IO5	EMAC1_TXD1	I3C1_SCL	TRACE_D5	SDMMC_DATA2	EMAC2_PPSTRIG2	UART1_RTS_N	SPIS1_MOSI		GPIO1_IO5	CM_HPS_OSC_CLK
	NA	HPS_IOB_7	V127	GPIO1_IO6	EMAC1_RXD0	I3C0_SDA	TRACE_D4	SDMMC_DATA3	I2C1_SDA	UART1_TX	SPIS1_SS0_N		GPIO1_IO6	CM_HPS_OSC_CLK
	NA	HPS_IOA_9	N135	GPIO0_IO8	I3C1_SDA	USB0_DATA4	TRACE_D14	SDMMC_DATA4	I2C_EMAC1_SDA	MDIO1_MDIO	SPIS1_CLK	SPIM1_CLK	GPIO0_IO8	CM_HPS_OSC_CLK
	NA	HPS_IOA_10	AK120	GPIO0_IO9	I3C1_SCL	USB0_DATA5	TRACE_D13	SDMMC_DATA5	I2C_EMAC1_SCL	MDIO1_MDC	SPIS1_MOSI	SPIM1_MOSI	GPIO0_IO9	CM_HPS_OSC_CLK
	NA	HPS_IOB_11	T124	GPIO1_IO10	EMAC1_RXD2		TRACE_D12	SDMMC_DATA6	I2C_EMAC0_SDA	MDIO0_MDIO	SPIS0_SS0_N	JTAG_TDO	GPIO1_IO10	CM_HPS_OSC_CLK
	NA	HPS_IOB_12	P124	GPIO1_IO11	EMAC1_RXD3		TRACE_D11	SDMMC_DATA7	I2C_EMAC0_SCL	MDIO0_MDC	SPIS0_MISO	JTAG_TDI	GPIO1_IO11	CM_HPS_OSC_CLK
	NA	HPS_IOB_5	B134	GPIO1_IO4	EMAC1_TXD0	I3C1_SDA	TRACE_D6	SDMMC_WRITE_PROTECT	EMAC2_PPS2	UART1_CTS_N	SPIS1_CLK	SPIM1_SS1_N	GPIO1_IO4	CM_HPS_OSC_CLK
USB2.0	NA	HPS_IOA_13	P132	GPIO0_IO12	EMAC0_TX_CLK	USB1_CLK	TRACE_D10	SDMMC_PU_PD_DATA2					GPIO0_IO12	CM_HPS_OSC_CLK
	NA	HPS_IOA_14	L135	GPIO0_IO13	EMAC0_TX_CTL	USB1_STP	TRACE_D9	SDMMC_PWR_ENA					GPIO0_IO13	CM_HPS_OSC_CLK
	NA	HPS_IOA_15	J135	GPIO0_IO14	EMAC0_RX_CLK	USB1_DIR	TRACE_D8						GPIO0_IO14	CM_HPS_OSC_CLK
	NA	HPS_IOA_16	AD135	GPIO0_IO15	EMAC0_RX_CTL	USB1_DATA0	TRACE_D7	SDMMC_DATA_STROBE					GPIO0_IO15	CM_HPS_OSC_CLK
	NA	HPS_IOA_17	M132	GPIO0_IO16	EMAC0_TXD0	USB1_DATA1	TRACE_D6		I3C1_SDA				GPIO0_IO16	CM_HPS_OSC_CLK
	NA	HPS_IOA_18	AD134	GPIO0_IO17	EMAC0_TXD1	USB1_NXT	TRACE_D5		I3C1_SCL				GPIO0_IO17	CM_HPS_OSC_CLK
	NA	HPS_IOA_19	K132	GPIO0_IO18	EMAC0_RXD0	USB1_DATA2	TRACE_D4		I3C0_SDA				GPIO0_IO18	CM_HPS_OSC_CLK
	NA	HPS_IOA_20	AG129	GPIO0_IO19	EMAC0_RXD1	USB1_DATA3	TRACE_CLK		I3C0_SCL			SPIM1_SS1_N	GPIO0_IO19	CM_HPS_OSC_CLK
	NA	HPS_IOA_21	J134	GPIO0_IO20	EMAC0_TXD2	USB1_DATA4	TRACE_D0		I2C1_SDA	UART0_CTS_N	SPIS0_CLK	SPIM1_CLK	GPIO0_IO20	CM_HPS_OSC_CLK
	NA	HPS_IOA_22	AG120	GPIO0_IO21	EMAC0_TXD3	USB1_DATA5	TRACE_D1		I2C1_SCL	UART0_RTS_N	SPIS0_MOSI	SPIM1_MOSI	GPIO0_IO21	CM_HPS_OSC_CLK
	NA	HPS_IOA_23	G134	GPIO0_IO22	EMAC0_RXD2	USB1_DATA6	TRACE_D2		I2C1_SCL	UART0_TX	SPIS0_SS0_N	SPIM1_MISO	GPIO0_IO22	CM_HPS_OSC_CLK
	NA	HPS_IOA_24	G135	GPIO0_IO23	EMAC0_RXD3	USB1_DATA7	TRACE_D3		I2C0_SCL	UART0_RX	SPIS0_MISO	SPIM1_SS0_N	GPIO0_IO23	CM_HPS_OSC_CLK
Board-to-Board Connector2 Features from Intel Agilex 5 SoC HPS														
UART0	D25	HPS_IOA_1	W135	GPIO0_IO0	EMAC0_PPS0	USB0_CLK	TRACE_D10	SDMMC_DATA0		UART0_CTS_N	SPIS0_CLK	SPIM0_SS1_N	GPIO0_IO0	CM_HPS_OSC_CLK
	D26	HPS_IOA_2	U135	GPIO0_IO1	EMAC0_PPSTRIG0	USB0_STP	TRACE_D9	SDMMC_DATA1		UART0_RTS_N	SPIS0_MOSI	SPIM1_SS1_N	GPIO0_IO1	CM_HPS_OSC_CLK
	D23	HPS_IOA_3	W134	GPIO0_IO2	EMAC1_PPS1	USB0_DIR	TRACE_D8	SDMMC_CLK	I2C1_SDA	UART0_TX	SPIS0_SS0_N		GPIO0_IO2	CM_HPS_OSC_CLK
	D24	HPS_IOA_4	AK115	GPIO0_IO3	EMAC1_PPSTRIG1	USB0_DATA0	TRACE_D7		I2C1_SCL	UART0_RX	SPIS0_MISO		GPIO0_IO3	CM_HPS_OSC_CLK
I2C	C9	HPS_IOA_5	U134	GPIO0_IO4	EMAC2_PPS2	USB0_DATA1	TRACE_D6	SDMMC_WRITE_PROTECT	I2C0_SDA	UART1_CTS_N		SPIM0_CLK	GPIO0_IO4	CM_HPS_OSC_CLK
	C8	HPS_IOA_6	AL120	GPIO0_IO5	EMAC2_PPSTRIG2	USB0_NXT	TRACE_D5	SDMMC_DATA2	I2C0_SCL	UART1_RTS_N		SPIM0_MOSI	GPIO0_IO5	CM_HPS_OSC_CLK
Debug UART	A13	HPS_IOA_7	R134	GPIO0_IO6		USB0_DATA2	TRACE_D4	SDMMC_DATA3	I2C_EMAC2_SDA	UART1_TX	MDIO2_MDIO	SPIM0_MISO	GPIO0_IO6	CM_HPS_OSC_CLK
	A14	HPS_IOA_8	AG115	GPIO0_IO7		USB0_DATA3	TRACE_D15	SDMMC_CMD	I2C_EMAC2_SCL	UART1_RX	MDIO2_MDC	SPIM0_SS0_N	GPIO0_IO7	CM_HPS_OSC_CLK
ENET	C13	HPS_IOB_9	T127	GPIO1_IO8	EMAC1_TXD2		TRACE_D14	SDMMC_DATA4	I2C_EMAC2_SDA	MDIO2_MDIO	SPIS0_CLK	JTAG_TCK	GPIO1_IO8	CM_HPS_OSC_CLK
	C12	HPS_IOB_10	Y132	GPIO1_IO9	EMAC1_TXD3		TRACE_D13	SDMMC_DATA5	I2C_EMAC2_SCL	MDIO2_MDC	SPIS0_MOSI	JTAG_TMS	GPIO1_IO9	CM_HPS_OSC_CLK
	C16	HPS_IOB_13	M127	GPIO1_IO12	EMAC2_TX_CLK		TRACE_D10	SDMMC_PU_PD_DATA2	I2C1_SDA				GPIO1_IO12	CM_HPS_OSC_CLK
	C21	HPS_IOB_14	K127	GPIO1_IO13	EMAC2_TX_CTL		TRACE_D9	SDMMC_PWR_ENA	I2C1_SCL				GPIO1_IO13	CM_HPS_OSC_CLK
	C23	HPS_IOB_15	M124	GPIO1_IO14	EMAC2_RX_CLK	I3C1_SDA	TRACE_D8			UART1_TX			GPIO1_IO14	CM_HPS_OSC_CLK
	C28	HPS_IOB_16	AB127	GPIO1_IO15	EMAC2_RX_CTL	I3C1_SCL	TRACE_D7	SDMMC_DATA_STROBE		UART1_RX			GPIO1_IO15	CM_HPS_OSC_CLK
	C17	HPS_IOB_17	K124	GPIO1_IO16	EMAC2_TXD0	I3C0_SDA	TRACE_D6			UART1_CTS_N			GPIO1_IO16	CM_HPS_OSC_CLK
	C18	HPS_IOB_18	Y127	GPIO1_IO17	EMAC2_TXD1	I3C0_SCL	TRACE_D5			UART1_RTS_N		SPIM0_SS1_N	GPIO1_IO17	CM_HPS_OSC_CLK
	C24	HPS_IOB_19	H127	GPIO1_IO18	EMAC2_RXD0		TRACE_D4		I2C_EMAC1_SDA	MDIO1_MDIO		SPIM0_MISO	GPIO1_IO18	CM_HPS_OSC_CLK
	C25	HPS_IOB_20	AB124	GPIO1_IO19	EMAC2_RXD1		TRACE_CLK		I2C_EMAC1_SCL	MDIO1_MDC		SPIM0_SS0_N	GPIO1_IO19	CM_HPS_OSC_CLK
	C19	HPS_IOB_21	F127	GPIO1_IO20	EMAC2_TXD2		TRACE_D0		I2C_EMAC2_SDA		SPIS1_CLK	SPIM0_CLK	GPIO1_IO20	CM_HPS_OSC_CLK
	C20	HPS_IOB_22	Y124	GPIO1_IO21	EMAC2_TXD3		TRACE_D1		I2C_EMAC2_SCL		SPIS1_MOSI	SPIM0_MOSI	GPIO1_IO21	CM_HPS_OSC_CLK
	C26	HPS_IOB_23	F124	GPIO1_IO22	EMAC2_RXD2		TRACE_D2		I2C_EMAC0_SDA	MDIO0_MDIO	SPIS1_SS0_N	SPIM0_MISO	GPIO1_IO22	CM_HPS_OSC_CLK
	C27	HPS_IOB_24	D124	GPIO1_IO23	EMAC2_RXD3		TRACE_D3		I2C_EMAC0_SCL	MDIO0_MDC	SPIS1_MISO	SPIM0_SS0_N	GPIO1_IO23	CM_HPS_OSC_CLK

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Agiulex 5 SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Agilex 5 SOM .

Table 33: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[2]	0V	3V	3.15V	±20mV

[1]Agilex 5 SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector2.

[2]Agilex 5 SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

The Agilex 5 SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOM_PWR_EN signal from Board-to-Board Connector2 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOM_PWR_EN signal from Board-to-Board Connector2 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

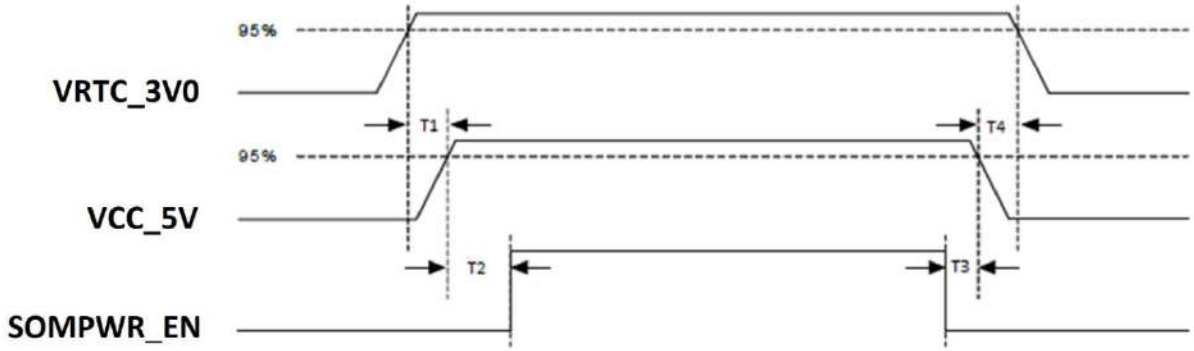

Figure 6: Power Input Sequencing

Table 34: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.

3.1.3 Power Consumption

TBD.

For more accurate power estimation, iWave recommends to use Intel Power Estimator (IPE) tool and calculate the SoC and FPGA power. Also add extra power for other On-SOM peripherals power.

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Agilex 5 SOM

Table 35: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.

3.2.3 RoHS Compliance

iWave's Agilex 5 SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's Agilex 5 SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 Agilex 5 SOM Mechanical Dimensions

Agilex 5 SOM PCB size is 60mm x 70mm x 1.83mm. The dimensional details of the SOM will be updated in future releases.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Agilex 5 SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 36: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G58M Agilex 5 SoC FPGA SOM		
iG58M-E065B5-4L004G-E0032G-EAA	A5E065B (-5 speed) B32A Agilex 5 SOC SOM with 2GB HPS LPDDR4, Dual 2GB FPGA LPDDR4, 32GB eMMC SOM	-0°C to 85°C

5. APPENDIX

5.1 Agilex 5 SOM Development Platform

iWave Systems supports iG-RainboW-G58M– Agilex 5 SOM Development Platform which is targeted for quick validation of the SOM. iWave's Agilex 5 Development Board incorporates Agilex 5 SOM and High-performance Carrier board with complete BSP support.

Contact iWave for more details on Agilex 5 SOM Development Platform.

Link : https://www.iwavesystems.com/product/agilex-5-soc-fpga-system-on-module/

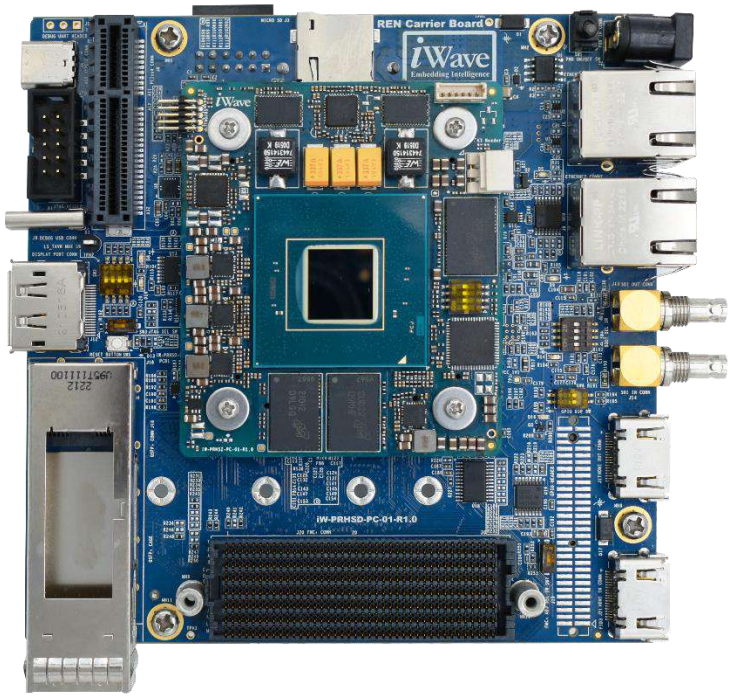

Figure 7: Agilex 5 Development Platform