iW-RainboW-G43M
Intel Agilex 7 SoC FPGA (R31B/R31C) SOM
Hardware Datasheet

Embedding Intelligence

Document Revision History

Document Number		iW-PRGTZ-UM-01-R2.0-REL0.3-Hardware
Release	**Date**	**Description**
0.3	06th Mar 2024	Draft Version

Disclaimer

iWave Systems reserves the right to change details in this publication including but not limited to any Product specification without notice.

No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by iWave Systems, its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.

CPU and other major components used in this product may have several silicon errata associated with it. Under no circumstances, iWave Systems shall be liable for the silicon errata and associated issues.

Trademarks

All registered trademarks, product names mentioned in this publication are the property of their respective owners and used for identification purposes only.

Certification

iWave Systems Technologies Pvt. Ltd. is an ISO 9001:2015 Certified Company.

Warranty & RMA

Warranty support for Hardware: 1 Year from iWave or iWave's EMS partner.
For warranty terms, go through the below web link,
http://www.iwavesystems.com/support/warranty.html

For Return Merchandise Authorization (RMA), go through the below web link,
http://www.iwavesystems.com/support/rma.html

Technical Support

iWave Systems technical support team is committed to provide the best possible support for our customers so that our Hardware and Software can be easily migrated and used.
For assistance, contact our Technical Support team at,

Email : support.ip@iwavesystems.com
Website : www.iwavesystems.com
Address : iWave Systems Technologies Pvt. Ltd.
7/B, 29th Main, BTM Layout 2nd Stage,
Bengaluru, Karnataka,
India – 560076

Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Intel Agilex 7 SoC FPGA(R31C/R31B) System on Module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Intel Agilex 7 SoC FPGA System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The Intel Agilex 7 SoC FPGA (R31C/R31B) SOM is an extension of Intel Agilex 7 SoC FPGA(R31C/R31B). Intel Agilex 7 SoC FPGA (R31C/R31B) SOM has a form factor of 90mm x 120mm and provides the functional requirements for an embedded application. Three High-Speed High-Density COM-HPC standard connectors that facilitates the carrier board interfaces to carry all the I/O signals to and from the Intel Agilex 7 SoC FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
NPTH	Non-Plated Through hole
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SGMII	Serial Gigabit Media Independent Interface
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On the Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Agilex 7 Hard Processor Systems Technical Reference Manual
- Intel Agilex 7 Device Data Sheet
- Intel Agilex 7 Device Design Guidelines

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Intel Agilex 7 SoC FPGA (R31C/R31B) SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Intel Agilex 7 SoC FPGA (R31C/R31B) SOM Block Diagram

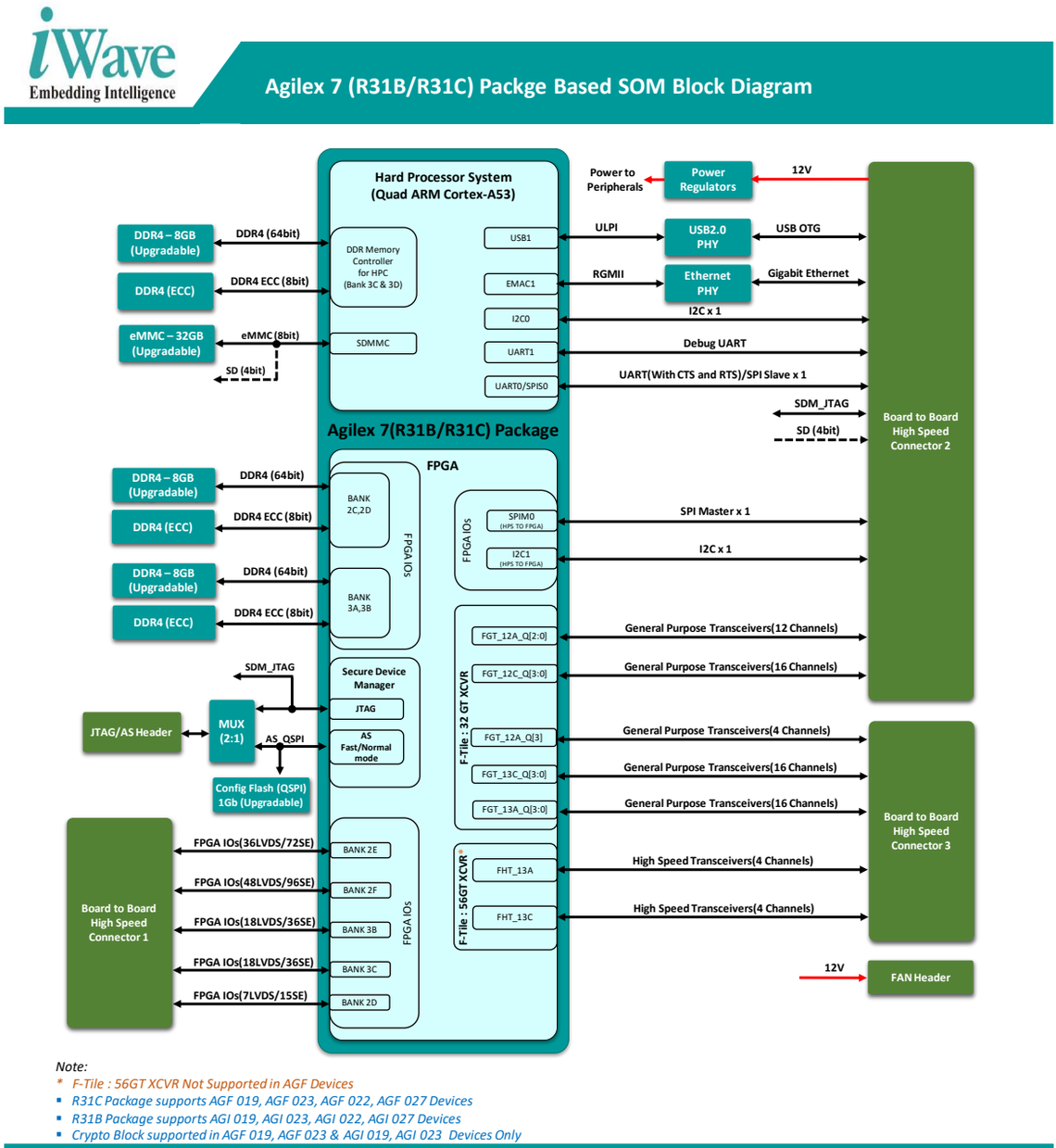

Figure 1: Intel Agilex 7 SoC FPGA SOM Block Diagram

2.2 Intel Agilex 7 SoC FPGA SOM Features

The Intel Agilex 7 SoC FPGA (R31C/R31B) SOM supports the following features.

SoC

- The Intel Agilex 7 SoC FPGA
  - Compatible Agilex 7 (R31B) I-Series – Agilex 7 AGI 019, AGI 023, AGI 022, AGI 023
  - Compatible Agilex 7 (R31C) F-Series – Agilex 7 AGF 019, AGF 023, AGF 022, AGF 023
    - Hard Processing System (HPS)
      - Quad-core 64-bit Arm Cortex-A53 up to 1.50 GHz
    - Field Programmable Gate Array (FPGA)
      - Up to 2,692,760 Logic elements
      - 64 x FGT transceivers up to 32Gbps in NRZ or 58Gbps in PAM4 Format [4]
      - 8 x FHT transceivers up to 58Gbps in NRZ or 116Gbps in PAM4 Format [3]

Power

- Discrete Power Regulators

Memory

- 8GB DDR4 SDRAM (64bit + 8bit) with ECC for HPS (Expandable)[1]
- 2 x 8GB DDR4 SDRAM1 (64bit + 8bit) with ECC for FPGA (Expandable)[1]
- 1Gb QSPI Flash (Expandable)[1]
- 32GB eMMC Flash (Expandable)[1]

Other On-SOM Features

- Gigabit Ethernet PHY Transceiver
- USB2.0 Transceiver
- On SOM PTP & SyncE Network Synchronizers
- JTAG/Active Serial Header
- Fan Header

Board to Board Connector1 Interfaces (400pin)

From FPGA Block

- 7 LVDS/15SE FPGA IOs from Bank 2D
- 36 LVDS/72SE FPGA IOs from Bank 2E
- 48 LVDS/96SE FPGA IOs from Bank 2F
- 18 LVDS/36SE FPGA IOs from Bank 3B

- 18 LVDS/36SE FPGA IOs from Bank 3C

Board to Board Connector2 Interfaces (240pin)

From HPS Block

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- USB2.0 OTG x 1 Port (through On-SOM USB2.0 transceiver)
- SD (4bit) x 1 Port (Optional)
- UART/SPI Slave x 1 Port
- Debug UART x 1 Port
- Data UART x 1 Port
- I2C x 1 Ports
- SDM JTAG (Internally chained with HPS)

From FPGA Block

- FGT transceivers up to 58Gbps x 28 [4]
- SPI Master x 1 Port[2]
- I2C x 1 Port[2]

Board to Board Connector3 Interfaces (400pin)

From FPGA Block

- FHT Transceivers up to 116Gbps x 8 [3]
- FGT transceivers up to 58Gbps x 36oard to Board Connector3 Interfaces (240pin) [4]

General Specification

- Power Supply : 12V (from Board-to-Board Connector2)
- Form Factor : 120mm x 90mm

[1] The Expansion of DDR4, QSPI Flash and eMMC size/capacity are subject to availability of chips in market.

[2] These interfaces are routed from HPS to FPGA.

[3] F-Tile: 58Gbps or 116bps Transceivers are not supported in AGF Devices.

[4] F-Tile: Quad0 transceivers from all FGT banks do not support PAM4 speed; they only support NRZ 32Gbps.

2.3 Intel Agilex 7 SoC FPGA (R31B/R31C)

Intel Agilex 7 FPGAs and SoCs are built using an innovative chiplet architecture, which provides agile and flexible integration of heterogeneous technology elements in a System-in-Package (SiP). The chiplet architecture enables Intel to address a broad array of acceleration and high-bandwidth applications with tailored and flexible solutions. Leveraging advanced 3D packaging technology such as Intel Embedded Multi-Die Interconnect Bridge (EMIB), the chiplet approach allows the combination of traditional FPGA die with purpose-built semiconductor die to create devices that are uniquely optimized for target applications.

The Intel® Agilex 7™ F- and I-Series 10-nm SuperFin technology FPGAs and SoCs deliver on average 50% higher core performance or up to 40% lower power over previous generation high-performance FPGAs. These Intel® Agilex 7™ FPGAs and SoCs accelerate system engineers' delivery of today's and tomorrow's most advanced high-bandwidth applications through ground-breaking features.

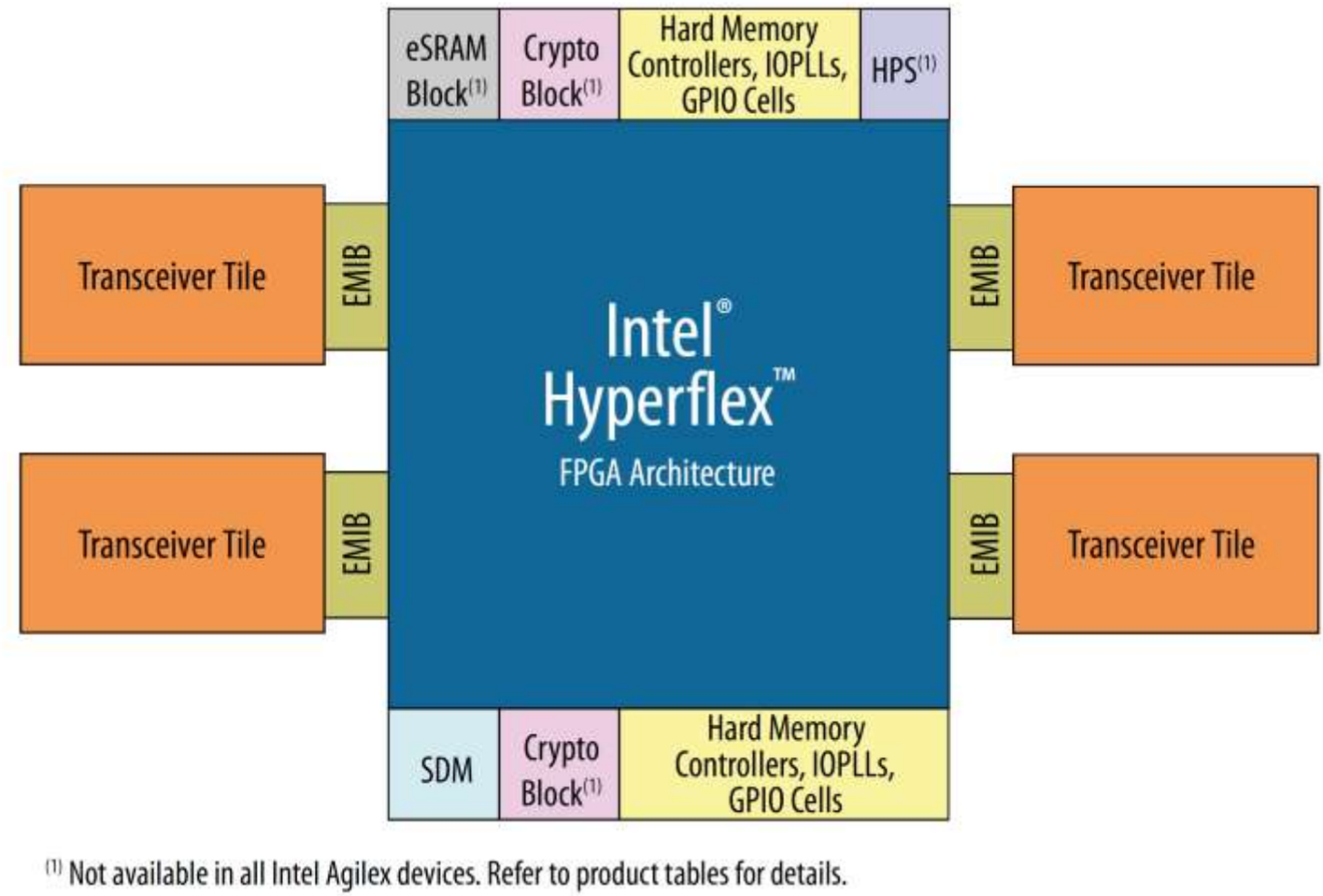

Figure 2: Intel Agilex 7 SoC FPGA CPU Simplified Block Diagram

Note: Please refer the latest Intel Agilex 7 SoC FPGA Datasheet from Intel website for more details which may be revised from time to time.

The Intel Agilex 7 SoC FPGA SOM is compatible to R31C Package AGF 019, AGF 023, AGF 022, AGF 027 devices & R31B Package supports AGI 019, AGI 023, AGI 022, AGI 027 devices

Feature comparison between R31C Package F-series devices is shown below:

Intel® Agilex™ F-Series FPGA and SoC FPGA Product Table

intel.

Version 2022.04.15

	PRODUCT LINE	AGF 019	AGF 023	AGF 022	AGF 027
Resources	Logic elements (LEs)	1,918,975	2,308,080	2,208,075	2,692,760
	Adaptive logic modules (ALMs)	650,500	782,400	748,500	912,800
	ALM registers	2,602,000	3,129,600	2,994,000	3,651,200
	High-performance crypto blocks	2	2	0	0
	eSRAM memory blocks	1	1	0	0
	eSRAM memory size (Mb)	18	18	0	0
	M20K memory blocks	8,500	10,464	10,900	13,272
	M20K memory size (Mb)	166	204	212	259
	MLAB memory count	32,525	39,120	37,425	45,640
	MLAB memory size (Mb)	20	24	23	28
	Fabric PLL	5	5	12	12
	I/O PLL	10	10	16	16
	Variable-precision digital signal processing (DSP) blocks	1,354	1,640	6,250	9,528
	18 x 19 multipliers	2,708	3,280	12,500	17,056
	Single-precision or half-precision tera floating point operations per second (TFLOPS)	2.0 / 4.0	2.5 / 5.0	9.4 / 18.8	12.8 / 25.6
	Maximum EMIF x72[2]	3	3	4	4
Maximum Available Device Resources	Maximum differential (RX or TX) pairs	240	240	384	384
	AIB interfaces	4	4	4	4
	Memory devices supported	DDR4 and QDR IV			
	Secure data manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection			
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4			
Tile Resources	F-Tile	PCI Express(PCIe) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 GbE hard IP block (10/25/50/100/200 Gbps FEC/PCS) IEEE 1588 v2 support PMA direct			
	E-Tile	Transceiver channel count : Up to 24 channels at 28.9 Gbps (NRZ) / 12 channels at 57.8 Gbps (PAM4) - RS & KP FEC[1] Networking support : - 400GbE (4 x 100GbE hard IP blocks (10/25 GbE FEC/PCS/MAC)) IEEE 1588 v2 support PMA direct			
	P-Tile	PCIe hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) SR-IOV 8PF / 2kVF VirtIO support Scalable IOV			

[1] Only 4 instances of KP-FEC are supported when using 100GE MAC
[2] Max EMIF count achieved using AVST x8 mode Compact - Address/Cmd lane (3 lanes) configuration

Figure 3: Intel Agilex 7 SoC FPGA F-Series Devices Comparison

Feature comparison between R31B Package I-series devices is shown below:

Intel® Agilex™ I-Series FPGA and SoC FPGA Product Table

intel.

Version 2022.05.30

	PRODUCT LINE	AGI 019	AGI 023	AGI 022	AGI 027
Resources	Logic elements (LEs)	1,918,975	2,308,080	2,208,075	2,692,760
	Adaptive logic modules (ALMs)	650,500	782,400	748,500	912,800
	ALM registers	2,602,000	3,129,600	2,994,000	3,651,200
	High-performance crypto blocks	2	2	0	0
	eSRAM memory blocks	1	1	0	0
	eSRAM memory size (Mb)	18	18	0	0
	M20K memory blocks	8,500	10,464	10,900	13,272
	M20K memory size (Mb)	166	204	212	259
	MLAB memory count	32,525	39,120	37,425	45,640
	MLAB memory size (Mb)	20	24	23	28
	Fabric PLL	5	5	12	12
	I/O PLL	10	10	16	16
	Variable-precision digital signal processing (DSP) blocks	1,354	1,640	6,250	8,528
	18 x 19 multipliers	2,708	3,280	12,500	17,056
	Single-precision or half-precision tera floating point operations per second (TFLOPS)	2.4 / 4.9	2.4 / 4.9	9.4 / 18.8	12.8 / 25.6
Maximum Available Device Resources	Maximum EMIF x72[1]	3	3	4	4
	Maximum differential (RX or TX) pairs	240	240	360	360
	AIB interfaces	4	4	4	4
	Memory devices supported	DDR4 and QDR IV			
	Secure data manager	AES-256/SHA-256 bitstream encryption or authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection			
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache , NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4			n/a
Tile Resources	F-Tile	PCI Express(PCIe) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : - 4 channels at 116 Gbps (PAM4) / 58 Gbps (NRZ) - 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) IEEE 1588 support PMA direct			
	R-Tile	Compute Express Interface (CXL) - Link width x16 lanes, x8 lanes PCIe hard IP block (Gen5 x16) or Bifurcateable 2x PCIe Gen5 x8 (EP) or 4x Gen5 x4 (RP) Virtualization (SR-IOV) supporting 8 PFs/2k VFs Scalable IOV VirtIO support Precise time management PIPE direct			

[1] Max EMIF count achieved using AVST x8 mode Compact - Address/Cmd lane (3 lanes) configuration

Figure 4: Intel Agilex 7 SoC FPGA I-Series Devices Comparison

2.3.1 Intel Agilex 7 Power

The Intel Agilex 7 SoC FPGA SOM uses discrete power regulators Power Management. In Intel Agilex 7 SoC FPGA SOM, Core power, Periphery circuitry power (VCC and VCCP) is connected to a SmartVID regulator, where the voltage can be varied between 0.70V – 0.90V based on Temperature & Performance. The HPS I/O voltage (VCCIO_HPS) is fixed to 1.8V. The I/O voltage details of each FPGA Bank & High-speed transceiver will be mentioned in the corresponding sections.

2.3.2 Intel Agilex 7 Reset

The Intel Agilex 7 SOM POR is taken care internally by SDM Block in device. Also, it supports warm reset input from Board-to-Board Connector2 pin B14 and connected to pin DF63, HPS_COLD_nRESET pin of the SDM Bank of the device.

2.3.3 Intel Agilex 7 Reference Clock

The Intel Agilex 7 SoC FPGA SOM supports on board clock generator for reference clock to different blocks of Intel Agilex 7 SoC and FPGA and to other On SOM peripherals. These reference clock details are mentioned in the below table.

Table 3: Intel Agilex 7 SoC and FPGA SOM Reference Clocks.

No	Part Number		Clock Type	Frequency		Drive Level		Termination
	Source	Destination		Source	Destination	Source	Destination	
1	Si5341B-D-GM OUT-0	USB TR REFCLK	LVCMOS	100Hz-250MHz	24MHz	-	-	33Ω
	Si5341B-D-GM OUT-1*	FGT_12C_Q2 REFCLK	LVDS	100Hz-1028MHz	125MHz	-	-	100Ω
	Si5341B-D-GM OUT-2	HPS DDR REFCLK	LVDS	100Hz-1028MHz	200MHz	-	-	100Ω
	Si5341B-D-GM OUT-3,4	2x FPGA DDR REFCLK	LVDS	100Hz-1028MHz	200MHz	-	-	100Ω
	Si5341B-D-GM OUT-5*	FPGA REFCLK	LVDS	100Hz-250MHz	100MHz	-	-	100Ω
	Si5341B-D-GM OUT-6	HPS OSC Clock	LVCMOS	100Hz-250MHz	25MHz	-	-	33Ω
	Si5341B-D-GM OUT-7	Ethernet PHY Clock	LVCMOS	100Hz-250MHz	25MHz	-	-	33Ω
	Si5341B-D-GM OUT-8	SDM OSC Clock	LVCMOS	100Hz-250MHz	125MHz	-	-	33Ω
	Si5341B-D-GM OUT-9*	FGT_13A_Q2 REFCLK	LVDS	100Hz-1028MHz	148.5MHz	-	-	100Ω

No	Part Number		Clock Type	Frequency		Drive Level		Termination
	Source	Destination		Source	Destination	Source	Destination	
2	ZL30733(SyncE) OUT-0	FPGA Time of the Day	LVPECL	9.72MHz-400MHz	100MHz	-	-	200Ω
	ZL30733(SyncE) OUT-1p	B2B PSS clock	LVCMOS	9.72MHz-400MHz	1MHz	-	-	200Ω
	ZL30733(SyncE) OUT-1n	FPGA PSS clock	LVCMOS	9.72MHz-400MHz	1MHz	-	-	200Ω
	ZL30733(SyncE) OUT-2p	B2B	LVCMOS	9.72MHz-400MHz	10MHz	-	-	200Ω
	ZL30733(SyncE) OUT-3	FGT_12A_Q2 REFCLK	LVPECL	9.72MHz-400MHz	156.25MHz	-	-	200Ω
	ZL30733(SyncE) OUT-4	FGT_12C_Q2 REFCLK	LVPECL	9.72MHz-400MHz	156.25MHz	-	-	200Ω
	ZL30733(SyncE) OUT-5	FGT_13A_Q2 REFCLK	LVPECL	9.72MHz-400MHz	156.25MHz	-	-	200Ω
	ZL30733(SyncE) OUT-6	FGT_13C_Q2 REFCLK	LVPECL	9.72MHz-400MHz	156.25MHz	-	-	200Ω
	ZL30733(SyncE) OUT-7,8	FHT_13A,13C REFCLK	LVPECL	9.72MHz-400MHz	156.25MHz	-	-	200Ω
	ZL30733(SyncE) OUT-9	B2B SYNC_OUT	LVDS	9.72MHz-400MHz	100MHz	-	-	200Ω
3	VCC1-1537-114M285000	ZL30733 OSC CLK	CMOS	0.5Hz-300MHz	114.285MHz	8 mA (Min)	-	36Ω
4	OX-6011-EAE-1080-20M000	ZL30733 REFIN CLK	HCMOS	0.5Hz-300MHz	20MHz	-	-	36Ω

Note:
[1] Si5341B-GM: Drive strength is register programmable setting and stored in NVM.
[2] ZL30733: Frequency & Drive strength is programmable.
** Optional*

2.3.4 Intel Agilex 7 SoC and FPGA Configuration & Status

The Intel Agilex 7 SoC and FPGA uses multi-stage boot process that supports both a non-secure and a secure boot. It supports different configuration schemes -JTAG-based configuration, AS Fast or Standard POR configuration. These configuration schemes are selected using the MSEL pin setting.

The SDM is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the First stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the HPS first and then configure the FPGA or it can be set to configure the FPGA first, then boot the HPS.

The Intel Agilex 7 SoC and FPGA SOM supports LED for the FPGA Configuration status indication namely CONFIG_DONE. LED interfaced to CONFIG_DONE and it is asserted when the FPGA configuration is complete. It is used to indicate if the FPGA is configured or not.

2.3.5 Intel Agilex 7 Boot Mode Switch

The Intel Agilex 7 SoC and FPGA always boots from SDM first and then boots the HPS or FPGA. Intel Agilex 7 SoC and FPGA supports the SDM QSPI or JTAG as the First Stage Bootloader in Standard or Fast Mode. Upon device reset, Intel Agilex 7 SoC and FPGA MSEL pins are read to determine the primary boot device. The ON SOM Switch also supports to switch between Active serial or JTAG connectivity on the On SOM Header. Also Direct to Factory Image option is made available on the switch.

The Intel Agilex 7 SoC and FPGA SOM supports Switching between Active Serial & JTAG Connectivity on the On SOM Header using the POS3 of the switch. Refer the below table to select between JTAG & Active Serial.

Table 4: JTAG & Active Serial Switch Truth Table

Intel Agilex 7 -AS/JTAG Header selection	SW 1 (4 Position Switch-POS3)	
	POS 3	Switch Position Image
SDM JTAG on AS/JTAG Header	OFF	
SDM Active Serial on AS/JTAG Header	ON	

The Intel Agilex 7 SoC and FPGA SOM supports selection between the different configuration schemes making use of POS1 and POS2 the switch. Refer the below table to select between the different configuration schemes.

Table 5: Configuration Selection Truth Table

Intel Agilex 7 Configuration Scheme Selection	SW (4 Position Switch-POS1 &POS2)		
	POS 1	POS 2	Switch Position Image
	MSEL2	MSEL1	
Active Serial - Fast Mode	OFF	OFF	
Active Serial - Standard Mode	OFF	ON	

2.3.6 Agilex 7 SoC/FPGA High Speed Transceivers

The Agilex 7 SoC/FPGA SOM supports 64 x FGT high speed transceivers and 8 x FHT high speed transceivers on Board-to-Board connectors from Agilex 7 FPGA fabric. The Agilex 7 SoC/FPGA has four high speed transceiver banks (12A, 12C, 13A and 13C) and each transceiver bank has four FGT quad. Special bank 13A and 13C on top of four FGT quad its has one FHT quad as well in R31B Package devices and each quad supports four high speed transmit and receive channels. So, total 72 high speed transmit and receive channels for each bank. Also, each high-speed transceiver quad supports two reference clock input pairs and last two quad supports each one reference clock output pairs. Transceiver data rate performance is based on the transceiver speed grade of the Agilex 7 SoC/FPGA as mentioned in the below table.

Table 6: Agilex 7 R31B/R31C SoC/FPGA Transceiver data rate performance

Description	Condition	Transceiver Speed Grade			Unit
		-1	-2	-3	
FGT					
Supported data rate	NRZ	1–32.45	1–32	1–17.4	Gbps
	PAM4	20–58.125	20–58.125	20–32	Gbps
FHT					
Supported data rate	NRZ	24–29, 48–58	24–29	24–29	Gbps
	PAM4	48–58, 96–116	48–58	48–58	Gbps

Note: FGT Quad0 can only support 20-32 Gbps PAM4. FGT Quad1, Quad2, and Quad3 can ***support 20-58 Gbps PAM4.***

The Agilex 7 SoC/FPGA SOM supports 28 high speed transceiver channels from Bank 12A (Quad0, Quad1 & Quad2) and Bank 12C (Quad0, Quad1, Quad2 & Quad3) along with two reference clock input pairs of each quad on Board to Board connector2 and 36 high speed transceiver channels from Bank 12A (Quad0), 13A (Quad0, Quad1, Quad2 & Quad3) and 13C (Quad0, Quad1, Quad2 & Quad3) along with two reference clock input pairs of each quad on Board-to-Board conenctor3 and 8 supper speed transceiver channels from Bank 13A and 13C along with two reference clock input pairs of quad on Board-to-Board conenctor3. In Agilex 7 SoC/FPGA SOM, on board termination and AC coupling capacitors are not supported on transceiver lines. So it has to be taken care in the carrier board if required.

2.4 Memory

2.4.1 DDR4 SDRAM with ECC for HPS

The Intel Agilex 7 SoC and FPGA SOM supports 64bit, 8GB DDR4 RAM memory for Intel Agilex 7 HPS. Four 16 bit, 2GB DDR4 SDRAM ICs are used to support total on board HPS RAM memory of 8GB. Also, Intel Agilex 7 SoC and FPGA SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 1600MHz in -1 Speed Grade devices and 1334Mhz and 1200MHz speed respectively in -2 and -3 Speed Grade Devices. DDR4 memory is connected to the hard memory controller supported Banks- 3C and 3D. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

The HPS DDR4 reference clock is connected to Bank 3D -T35 & U34 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.4.2 DDR4 SDRAM1 for FPGA

The Intel Agilex 7 SoC and FPGA SOM supports 2 x 64bit, 8GB DDR4 RAM memory for Intel Agilex 7 FPGA. For the first FPGA DDR4 SDRAM, four 16 bit, 2GB DDR4 SDRAM ICs are used to support a total on board FPGA RAM memory of 8GB. Also, Intel Agilex 7 SoC and FPGA SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 1600MHz in -1 Speed Grade devices and 1334Mhz and 1200MHz speed respectively in -2 and -3 Speed Grade Devices. DDR4 memory is connected to the FPGA Banks- 2C and 2D. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

The FPGA1 DDR4 reference clock is connected to Bank 2C -DE36 & DD35 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.4.3 DDR4 SDRAM2 for FPGA

The Intel Agilex 7 SoC and FPGA SOM supports 64bit, 8GB DDR4 RAM memory for Intel Agilex 7 FPGA. For the second FPGA DDR4 SDRAM, four 16 bit, 2GB DDR4 SDRAM ICs are used to support a total on board FPGA RAM memory of 8GB. Also, Intel Agilex 7 SoC and FPGA SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 1600MHz in -1 Speed Grade devices and 1334Mhz and 1200MHz speed respectively in -2 and -3 Speed Grade Devices. DDR4 memory is connected to the FPGA Banks- 2C and 2D. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

The FPGA1 DDR4 reference clock is connected to Bank 3A -F65 & G64 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.4.4 eMMC Flash

The Intel Agilex 7 SoC and FPGA SOM supports 32GB eMMC Flash memory for Second Stage Boot & Storage of Intel Agilex 7 SoC and FPGA. This eMMC Flash memory is directly connected to the SDMMC controller in HPS Block of the Intel Agilex 7 SoC and FPGA and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC5.0 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

*Note: Refer **ORDERING INFORMATION** section for exact eMMC Flash size used on the SOM based on the Product Part Number.*

2.4.5 QSPI Flash

The Intel Agilex 7 SoC and FPGA SOM supports 1Gb QSPI Flash memory for First Stage Boot & Storage of Intel Agilex 7 SoC and FPGA. This QSPI Flash memory is directly connected to the SDM controller of the Intel Agilex 7 SoC and FPGA SDM and operates at 1.8V Voltage level. The QSPI Flash size can be expandable based on the availability of higher density chips.

*Note: Refer **ORDERING INFORMATION** section for exact QSPI Flash size used on the SOM based on the Product Part Number.*

2.5 On SOM Features

2.5.1 JTAG/ Active Serial Header (Optional)

The Intel Agilex 7 SoC and FPGA SOM supports 10Pin JTAG/Active Serial Header for JTAG or Active Serial interface. JTAG Interface Signals and Active Serial Signals from the SDM of Intel Agilex 7 SoC and FPGA is connected to the 10pin Header through a MUX switch. JTAG and Active Serial can be selected by toggling the POS 3 of the DIP Switch. The Intel Agilex 7 SoC and FPGA 's HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Intel Agilex 7 SoC and FPGA. These JTAG interface signals are at 1.8V Voltage level.

The JTAG/Active Serial Header is physically located on topside of the SOM as shown below. USB Blaster Programming Cable can be directly connected to this JTAG Header. JTAG interface signals are also connected to Board-to-Board Connector2 for access from Carrier board. The JTAG/AS Header (J3) is physically located on topside of the SOM as shown below.

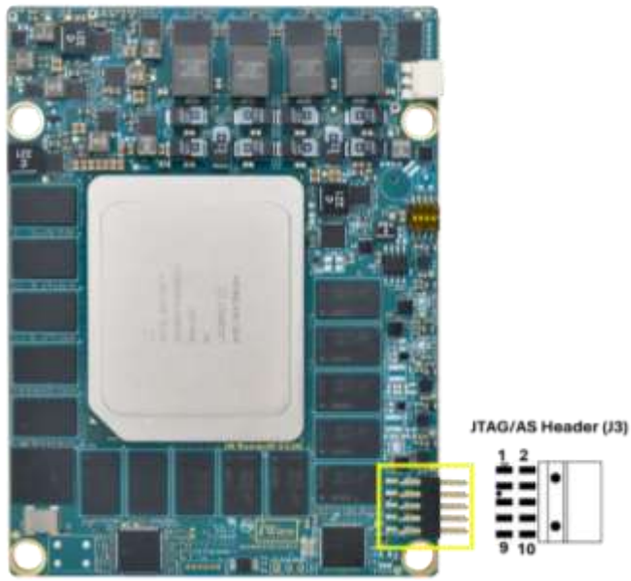

Figure 5: JTAG/AS Header

Number of Pins - 10

Connector Part - 610110249121 from Wurth

Mating Connector - 10pin cable of USB Blaster can be connected to the board directly

Table 7: JTAG/Active Serial Header Pinout- JTAG is selected

Pin No	Signal Name	Signal Type/ Termination	Description
1	JTAG_TCK	I, 1.8V CMOS	JTAG test Clock.
2	GND	Power	Ground.
3	JTAG_TDO	O, 1.8V CMOS	JTAG test data output.
4	VCC(TRGT)	Power	Target Power Supply

Pin No	Signal Name	Signal Type/ Termination	Description
5	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
6	JTAG_RESET	I, 1.8V CMOS /10K PU	JTAG RESET. Not connected to SoC or FPGA
7	NC	-	NC.
8	NC	-	NC.
9	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
10	GND	Power	Ground.

Table 8: JTAG/Active Serial Header Pinout- Active Serial is selected.

Pin No	Signal Name	Signal Type/ Termination	Description
1	AS_CLK	I, 1.8V CMOS/10K PD	Dedicated Serial clock to configure flash.
2	GND	Power	Ground.
3	AS_CONF_DONE	IO, 1.8V OD	Configuration status IO to Intel Agilex 7 SoC and FPGA.
4	VCC(TRGT)	Power	Target Power Supply
5	AS_nCONFIG	I, 1.8V CMOS/10K PU	Configuration input to Intel Agilex 7 SoC and FPGA
6	nCE	I, 1.8V CMOS/10K PU	Chip Enable input to Intel Agilex 7 SoC and FPGA
7	AS_DO	I, 1.8V CMOS	Serial Data input to Configuration flash
8	AS_CS0	I, 1.8V CMOS/10K PU	Chip select input to configuration flash.
9	AS_DI	O, 1.8V CMOS	Serial Data output from configuration flash.
10	GND	Power	Ground.

2.5.2 Fan Header

The Intel Agilex 7 SoC and FPGA SOM supports a Fan Header (J3) to connect cooling Fan if required. The Fan Header (J1) is physically located on topside of the SOM as shown below.

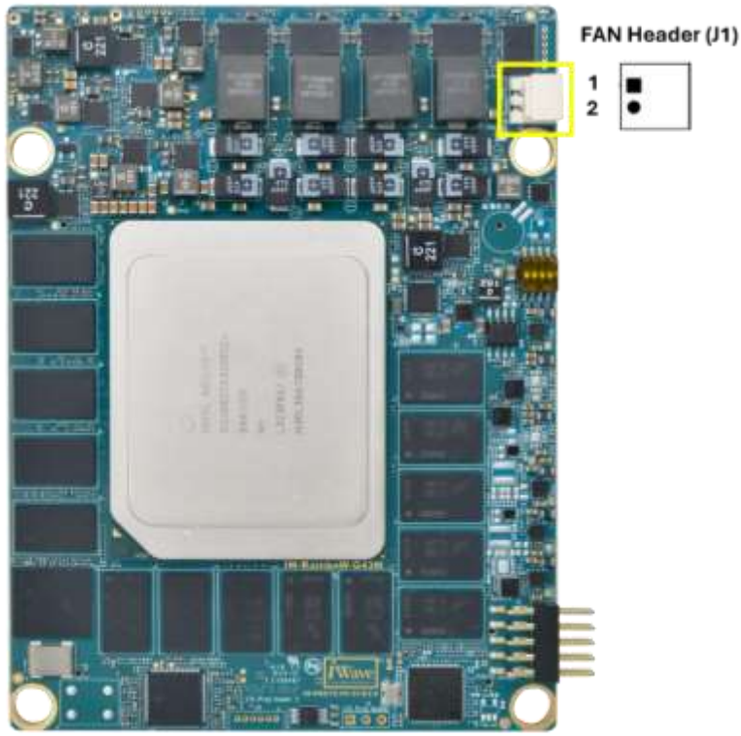

Figure 6: Fan Header

Number of Pins - 2

Connector Part - 52125-02-0200-01 from CNC

Mating Connector - 52225-02 from CNC

Table 9: Fan Header Pinout

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V or VCC_12V	O, 5V Power	Supply Voltage.
2	GND	Power	Ground.

The Intel Agilex 7 SoC and FPGA SOM supports three 400 pin high speed ruggedized terminal strip connectors for interfaces expansion. All the effort is made in Intel Agilex 7 SoC FPGA SOM design to provide the maximum interfaces of Intel Agilex 7 SoC and FPGA to the carrier board through these three Board to Board Connectors.

2.6 Board to Board Connector1

The Intel Agilex 7 SoC and FPGA SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1(J7) is physically located on bottom side of the SOM as shown below.

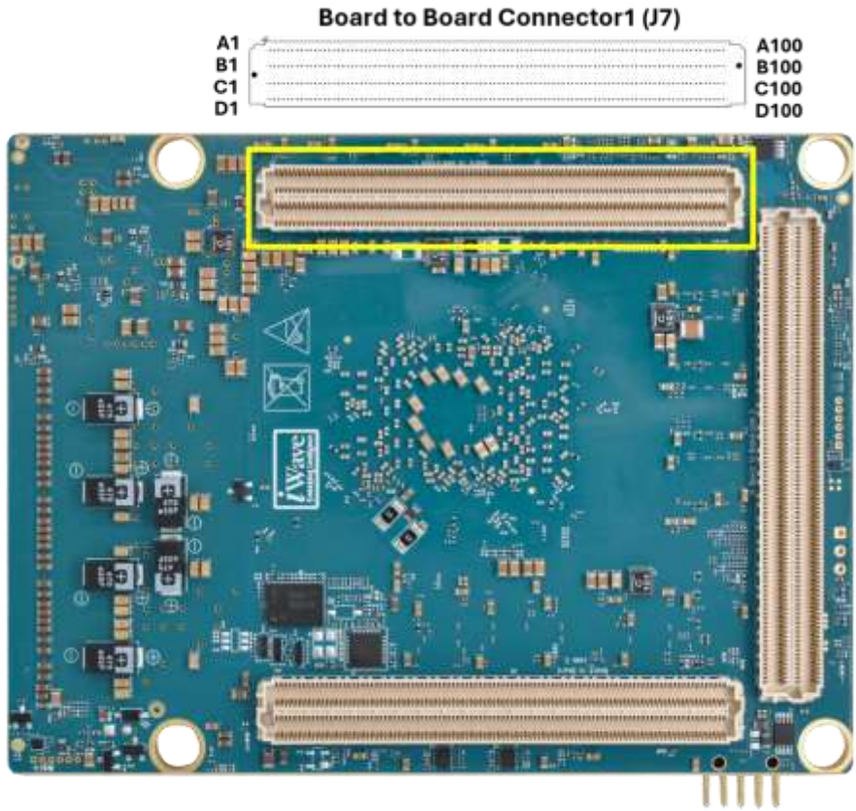

Figure 7: Board-to-Board Connector1

Number of Pins - 400

Connector Part Number - ASP-209946-01 from Samtech

Mating Connector - ASP-214802-01 from Samtech

Staking Height - 5mm

Table 10: Board to Board Connector1 Pinout

B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name
Row-A		Row-B		Row-C		Row-D	
A1	VCC_1V2_IO	B1	VCC_1V2_IO_2E	C1	VCC_1V2_IO_2F	D1	VCC_1V2_IO_2F
A2	FPGA_DK57_LVDS2E_5P_TX_IO76/CLKOUT_1P	B2	FPGA_DP61_LVDS2E_2P_TX_IO88	C2	FPGA_DF59_LVDS2E_4P_RX_IO82	D2	FPGA_DK59_LVDS2E_4P_TX_IO80
A3	FPGA_DJ58_LVDS2E_5N_TX_IO77/CLKOUT_1N	B3	FPGA_DR62_LVDS2E_2N_TX_IO89	C3	FPGA_DG60_LVDS2E_4N_RX_IO83	D3	FPGA_DJ60_LVDS2E_4N_TX_IO81
A4	FPGA_DF57_LVDS2E_5P_RX_IO78	B4	FPGA_DM63_LVDS2E_1P_RX_IO94	C4	FPGA_DM61_LVDS2E_2P_RX_IO90	D4	FPGA_DM59_LVDS2E_3P_RX_IO86
A5	FPGA_DG58_LVDS2E_5N_RX_IO79	B5	FPGA_DL64_LVDS2E_1N_RX_IO95	C5	FPGA_DL62_LVDS2E_2N_RX_IO91	D5	FPGA_DL60_LVDS2E_3N_RX_IO87
A6	FPGA_DK55_LVDS2E_6P_TX_IO72/CLKIN_1P	B6	FPGA_DF55_LVDS2E_6P_RX_IO74	C6	FPGA_DP63_LVDS2E_1P_TX_IO92	D6	FPGA_DP59_LVDS2E_3P_TX_IO84
A7	FPGA_DJ56_LVDS2E_6N_TX_IO73/CLKIN_1N	B7	FPGA_DG56_LVDS2E_6N_RX_IO75	C7	FPGA_DR64_LVDS2E_1N_TX_IO93	D7	FPGA_DR60_LVDS2E_3N_TX_IO85
A8	GND	B8	GND	C8	GND	D8	GND
A9	FPGA_DF51_LVDS2E_11P_RX_IO54	B9	FPGA_DF53_LVDS2E_10P_RX_IO58	C9	FPGA_DP55_LVDS2E_8P_TX_IO64	D9	FPGA_DM57_LVDS2E_7P_RX_IO70/CLKIN_0P
A10	FPGA_DG52_LVDS2E_11N_RX_IO55	B10	FPGA_DG54_LVDS2E_10N_RX_IO59	C10	FPGA_DR56_LVDS2E_8N_TX_IO65	D10	FPGA_DL58_LVDS2E_7N_RX_IO71/CLKIN_0N
A11	FPGA_DF49_LVDS2E_12P_RX_IO50	B11	FPGA_DP53_LVDS2E_9P_TX_IO60	C11	FPGA_DM53_LVDS2E_9P_RX_IO62	D11	FPGA_DP57_LVDS2E_7P_TX_IO68
A12	FPGA_DG50_LVDS2E_12N_RX_IO51	B12	FPGA_DR54_LVDS2E_9N_TX_IO61	C12	FPGA_DL54_LVDS2E_9N_RX_IO63	D12	FPGA_DR58_LVDS2E_7N_TX_IO69
A13	FPGA_DK49_LVDS2E_12P_TX_IO48	B13	FPGA_DK51_LVDS2E_11P_TX_IO52	C13	FPGA_DK53_LVDS2E_10P_TX_IO56	D13	FPGA_DM55_LVDS2E_8P_RX_IO66/CLKOUT_0P
A14	FPGA_DJ50_LVDS2E_12N_TX_IO49	B14	FPGA_DJ52_LVDS2E_11N_TX_IO53	C14	FPGA_DJ54_LVDS2E_10N_TX_IO57	D14	FPGA_DL56_LVDS2E_8N_RX_IO67/CLKOUT_0N
A15	GND	B15	GND	C15	GND	D15	GND
A16	FPGA_DP43_LVDS2F_5P_TX_IO76/CLKOUT_1P	B16	FPGA_DM41_LVDS2F_4P_RX_IO82	C16	FPGA_DK39_LVDS2F_2P_TX_IO88	D16	FPGA_DF37_LVDS2F_1P_RX_IO94
A17	FPGA_BR44_LVDS2F_5N_TX_IO77/CLKOUT_1N	B17	FPGA_DL42_LVDS2F_4N_RX_IO83	C17	FPGA_DJ40_LVDS2F_2N_TX_IO89	D17	FPGA_DG38_LVDS2F_1N_RX_IO95
A18	FPGA_DM45_LVDS2F_6P_RX_IO74	B18	FPGA_DP41_LVDS2F_4P_TX_IO80	C18	FPGA_DF41_LVDS2F_3P_RX_IO86	D18	FPGA_DK37_LVDS2F_1P_TX_IO92
A19	FPGA_DL46_LVDS2F_6N_RX_IO75	B19	FPGA_DR42_LVDS2F_4N_TX_IO81	C19	FPGA_DG42_LVDS2F_3N_RX_IO87	D19	FPGA_DJ38_LVDS2F_1N_TX_IO93
A20	FPGA_DP45_LVDS2F_6P_TX_IO72/CLKIN_1P	B20	FPGA_DM43_LVDS2F_5P_RX_IO78	C20	FPGA_DK41_LVDS2F_3P_TX_IO84	D20	FPGA_DF39_LVDS2F_2P_RX_IO90
A21	FPGA_DR46_LVDS2F_6N_TX_IO73/CLKIN_1N	B21	FPGA_DL44_LVDS2F_5N_RX_IO79	C21	FPGA_DJ42_LVDS2F_3N_TX_IO85	D21	FPGA_DG40_LVDS2F_2N_RX_IO91
A22	GND	B22	GND	C22	GND	D22	GND
A23	FPGA_DM47_LVDS2F_10P_RX_IO58	B23	FPGA_DP51_LVDS2F_12P_TX_IO48	C23	FPGA_DK45_LVDS2F_8P_TX_IO64	D23	FPGA_DF43_LVDS2F_7P_RX_IO70/CLKIN_0P
A24	FPGA_DL48_LVDS2F_10N_RX_IO59	B24	FPGA_DR52_LVDS2F_12N_TX_IO49	C24	FPGA_BJ46_LVDS2F_8N_TX_IO65	D24	FPGA_DG44_LVDS2F_7N_RX_IO71/CLKIN_0N
A25	FPGA_DP47_LVDS2F_10P_TX_IO56	B25	FPGA_DM49_LVDS2F_11P_RX_IO54	C25	FPGA_DM51_LVDS2F_12P_RX_IO50	D25	FPGA_DJ44_LVDS2F_7P_TX_IO68
A26	FPGA_DR48_LVDS2F_10N_TX_IO57	B26	FPGA_DL50_LVDS2F_11N_RX_IO55	C26	FPGA_DL52_LVDS2F_12N_RX_IO51	D26	FPGA_DK43_LVDS2F_7N_TX_IO69
A27	FPGA_DK47_LVDS2F_9P_TX_IO60	B27	FPGA_DF47_LVDS2F_9P_RX_IO62	C27	FPGA_DP49_LVDS2F_11P_TX_IO52	D27	FPGA_DF45_LVDS2F_8P_RX_IO66/CLKOUT_0P
A28	FPGA_BJ48_LVDS2F_9N_TX_IO61	B28	FPGA_DG48_LVDS2F_9N_RX_IO63	C28	FPGA_DR50_LVDS2F_11N_TX_IO53	D28	FPGA_DG46_LVDS2F_8N_RX_IO67/CLKOUT_0N
A29	GND	B29	GND	C29	GND	D29	GND
A30	FPGA_DD45_LVDS2F_17P_TX_IO28/CLKOUT_1P	B30	FPGA_DB43_LVDS2F_16P_RX_IO34	C30	FPGA_CP43_LVDS2F_23P_TX_IO4	D30	FPGA_CR46_LVDS2F_24P_TX_IO0
A31	FPGA_DE46_LVDS2F_17N_TX_IO29/CLKOUT_1N	B31	FPGA_DA44_LVDS2F_16N_RX_IO35	C31	FPGA_CR44_LVDS2F_23N_TX_IO5	D31	FPGA_CP45_LVDS2F_24N_TX_IO1
A32	FPGA_DB47_LVDS2F_18P_RX_IO26	B32	FPGA_DD43_LVDS2F_16P_TX_IO32	C32	FPGA_DB41_LVDS2F_15P_RX_IO38	D32	FPGA_CL46_LVDS2F_24P_RX_IO2
A33	FPGA_DA48_LVDS2F_18N_RX_IO27	B33	FPGA_BE44_LVDS2F_16N_TX_IO33	C33	FPGA_DA42_LVDS2F_15N_RX_IO39	D33	FPGA_CM45_LVDS2F_24N_RX_IO3
A34	FPGA_DD47_LVDS2F_18P_TX_IO24/CLKIN_1P	B34	FPGA_DB45_LVDS2F_17P_RX_IO30	C34	FPGA_DD41_LVDS2F_15P_TX_IO36	D34	FPGA_CM43_LVDS2F_23P_RX_IO6
A35	FPGA_DE48_LVDS2F_18N_TX_IO25/CLKIN_1N	B35	FPGA_DA46_LVDS2F_17N_RX_IO31	C35	FPGA_DE42_LVDS2F_15N_TX_IO37	D35	FPGA_CL44_LVDS2F_23N_RX_IO7
A36	GND	B36	GND	C36	GND	D36	GND
A37	FPGA_DD39_LVDS2F_14P_TX_IO40	B37	FPGA_CL42_LVDS2F_22P_RX_IO10	C37	FPGA_CW42_LVDS2F_19P_TX_IO20	D37	FPGA_CU42_LVDS2F_19P_RX_IO22/CLKIN_0P
A38	FPGA_DE40_LVDS2F_14N_TX_IO41	B38	FPGA_CM41_LVDS2F_22N_RX_IO11	C38	FPGA_CY41_LVDS2F_19N_TX_IO21	D38	FPGA_CT41_LVDS2F_19N_RX_IO23/CLKIN_0N
A39	FPGA_DB39_LVDS2F_14P_RX_IO42	B39	FPGA_CP41_LVDS2F_22P_TX_IO8	C39	FPGA_CT45_LVDS2F_21P_RX_IO14	D39	FPGA_CY43_LVDS2F_20P_TX_IO16

B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name
A40	FPGA_DA40_LVDS2F_14N_RX_IO43	**B40**	FPGA_CR42_LVDS2F_22N_TX_IO9	**C40**	FPGA_CU46_LVDS2F_21N_RX_IO15	**D40**	FPGA_CW44_LVDS2F_20N_TX_IO17
A41	FPGA_DD37_LVDS2F_13P_TX_IO44	**B41**	FPGA_DB37_LVDS2F_13P_RX_IO46	**C41**	FPGA_CW46_LVDS2F_21P_TX_IO12	**D41**	FPGA_CT43_LVDS2F_20P_RX_IO18/CLKOUT_0P
A42	FPGA_DE38_LVDS2F_13N_TX_IO45	**B42**	FPGA_DA38_LVDS2F_13N_RX_IO47	**C42**	FPGA_CY45_LVDS2F_21N_TX_IO13	**D42**	FPGA_CU44_LVDS2F_20N_RX_IO19/CLKOUT_0N
A43	GND	**B43**	GND	**C43**	GND	**D43**	GND
A44	FPGA_G54_LVDS3B_5P_TX_IO76/CLKOUT_1P	**B44**	FPGA_J56_LVDS3B_4P_RX_IO82	**C44**	FPGA_A58_LVDS3B_2P_TX_IO88	**D44**	FPGA_E60_LVDS3B_1P_RX_IO94
A45	FPGA_F55_LVDS3B_5N_TX_IO77/CLKOUT_1N	**B45**	FPGA_K57_LVDS3B_4N_RX_IO83	**C45**	FPGA_B59_LVDS3B_2N_TX_IO89	**D45**	FPGA_D61_LVDS3B_1N_RX_IO95
A46	FPGA_J52_LVDS3B_6P_RX_IO74	**B46**	FPGA_G56_LVDS3B_4P_TX_IO80	**C46**	FPGA_E56_LVDS3B_3P_RX_IO86	**D46**	FPGA_A60_LVDS3B_1P_TX_IO92
A47	FPGA_K53_LVDS3B_6N_RX_IO75	**B47**	FPGA_F57_LVDS3B_4N_TX_IO81	**C47**	FPGA_D57_LVDS3B_3N_RX_IO87	**D47**	FPGA_B61_LVDS3B_1N_TX_IO93
A48	FPGA_G52_LVDS3B_6P_TX_IO72/CLKIN_1P	**B48**	FPGA_J54_LVDS3B_5P_RX_IO78	**C48**	FPGA_A56_LVDS3B_3P_TX_IO84	**D48**	FPGA_E58_LVDS3B_2P_RX_IO90
A49	FPGA_F53_LVDS3B_6N_TX_IO73/CLKIN_1N	**B49**	FPGA_K55_LVDS3B_5N_RX_IO79	**C49**	FPGA_B57_LVDS3B_3N_TX_IO85	**D49**	FPGA_D59_LVDS3B_2N_RX_IO91
A50	GND	**B50**	GND	**C50**	GND	**D50**	GND
A51	FPGA_CY25_LVDS2D_17P_TX_IO28/CLKOUT_1P	**B51**	FPGA_CT23_LVDS2D_16P_RX_IO34	**C51**	FPGA_A52_LVDS3B_8P_TX_IO64	**D51**	FPGA_E54_LVDS3B_7P_RX_IO70/CLKIN_0P
A52	FPGA_CW26_LVDS2D_17N_TX_IO29/CLKOUT_1N	**B52**	FPGA_CU24_LVDS2D_16N_RX_IO35	**C52**	FPGA_B53_LVDS3B_8N_TX_IO65	**D52**	FPGA_D55_LVDS3B_7N_RX_IO71/CLKIN_0N
A53	FPGA_CT25_LVDS2D_17P_RX_IO30	**B53**	FPGA_CY23_LVDS2D_16P_TX_IO32	**C53**	FPGA_E50_LVDS3B_9P_RX_IO62	**D53**	FPGA_A54_LVDS3B_7P_TX_IO68
A54	FPGA_CU26_LVDS2D_17N_RX_IO31	**B54**	FPGA_CW24_LVDS2D_16N_TX_IO33	**C54**	FPGA_D51_LVDS3B_9N_RX_IO63	**D54**	FPGA_B55_LVDS3B_7N_TX_IO69
A55	NC	**B55**	FPGA_CT27_LVDS2D_18P_RX_IO26	**C55**	FPGA_A50_LVDS3B_9P_TX_IO60	**D55**	FPGA_E52_LVDS3B_8P_RX_IO66/CLKOUT_0P
A56	NC	**B56**	FPGA_CU28_LVDS2D_18N_RX_IO27	**C56**	FPGA_B51_LVDS3B_9N_TX_IO61	**D56**	FPGA_D53_LVDS3B_8N_RX_IO67/CLKOUT_0N
A57	GND	**B57**	GND	**C57**	GND	**D57**	GND
A58	GND	**B58**	GND	**C58**	GND	**D58**	GND
A59	FPGA_E42_LVDS3C_6P_RX_IO74	**B59**	FPGA_E44_LVDS3C_7P_RX_IO70/CLKIN_0P	**C59**	FPGA_CY51_LVDS2E_19P_TX_IO20	**D59**	NC
A60	FPGA_D43_LVDS3C_6N_RX_IO75	**B60**	FPGA_D45_LVDS3C_7N_RX_IO71/CLKIN_0N	**C60**	FPGA_CW52_LVDS2E_19N_TX_IO21	**D60**	NC
A61	GND	**B61**	GND	**C61**	GND	**D61**	GND
A62	GND	**B62**	GND	**C62**	GND	**D62**	GND
A63	FPGA_G36_LVDS3C_2P_TX_IO88	**B63**	FPGA_J36_LVDS3C_2P_RX_IO90	**C63**	FPGA_G34_LVDS3C_1P_TX_IO92	**D63**	FPGA_J34_LVDS3C_1P_RX_IO94
A64	FPGA_F37_LVDS3C_2N_TX_IO89	**B64**	FPGA_K37_LVDS3C_2N_RX_IO91	**C64**	FPGA_F35_LVDS3C_1N_TX_IO93	**D64**	FPGA_K35_LVDS3C_1N_RX_IO95
A65	GND	**B65**	GND	**C65**	GND	**D65**	GND
A66	GND	**B66**	GND	**C66**	GND	**D66**	GND
A67	FPGA_A38_LVDS3C_4P_TX_IO80	**B67**	FPGA_E38_LVDS3C_4P_RX_IO82	**C67**	FPGA_G38_LVDS3C_3P_TX_IO84	**D67**	FPGA_J38_LVDS3C_3P_RX_IO86
A68	FPGA_B39_LVDS3C_4N_TX_IO81	**B68**	FPGA_D39_LVDS3C_4N_RX_IO83	**C68**	FPGA_F39_LVDS3C_3N_TX_IO85	**D68**	FPGA_K39_LVDS3C_3N_RX_IO87
A69	GND	**B69**	GND	**C69**	GND	**D69**	GND
A70	GND	**B70**	GND	**C70**	GND	**D70**	GND
A71	NC	**B71**	NC	**C71**	NC	**D71**	NC
A72	NC	**B72**	NC	**C72**	NC	**D72**	NC
A73	GND	**B73**	GND	**C73**	GND	**D73**	GND
A74	GND	**B74**	GND	**C74**	GND	**D74**	GND
A75	FPGA_DB51_LVDS2E_23P_RX_IO6	**B75**	FPGA_DD51_LVDS2E_23P_TX_IO4	**C75**	FPGA_DB49_LVDS2E_24P_RX_IO2	**D75**	FPGA_DD49_LVDS2E_24P_TX_IO0
A76	FPGA_DA52_LVDS2E_23N_RX_IO7	**B76**	FPGA_DE52_LVDS2E_23N_TX_IO5	**C76**	FPGA_DA50_LVDS2E_24N_RX_IO3	**D76**	FPGA_DE50_LVDS2E_24N_TX_IO1
A77	GND	**B77**	GND	**C77**	GND	**D77**	GND
A78	GND	**B78**	GND	**C78**	GND	**D78**	GND

B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name	B2B1 Pin No	Signal Name
A79	FPGA_A46_LVDS3C_8P_TX_IO64	**B79**	FPGA_E46_LVDS3C_8P_RX_IO66/CLKOUT_0P	**C79**	FPGA_A40_LVDS3C_5P_TX_IO76/CLKOUT_1P	**D79**	FPGA_E40_LVDS3C_5P_RX_IO78
A80	FPGA_B47_LVDS3C_8N_TX_IO65	**B80**	FPGA_D47_LVDS3C_8N_RX_IO67/CLKOUT_0N	**C80**	FPGA_B41_LVDS3C_5N_TX_IO77/CLKOUT_1N	**D80**	FPGA_D41_LVDS3C_5N_RX_IO79
A81	GND	**B81**	GND	**C81**	GND	**D81**	GND
A82	GND	**B82**	GND	**C82**	GND	**D82**	GND
A83	FPGA_CP23_LVDS2D_13P_TX_IO44	**B83**	FPGA_CM23_LVDS2D_13P_RX_IO46	**C83**	FPGA_A48_LVDS3C_9P_TX_IO60	**D83**	FPGA_E48_LVDS3C_9P_RX_IO62
A84	FPGA_CR24_LVDS2D_13N_TX_IO45	**B84**	FPGA_CL24_LVDS2D_13N_RX_IO47	**C84**	FPGA_B49_LVDS3C_9N_TX_IO61	**D84**	FPGA_D49_LVDS3C_9N_RX_IO63
A85	GND	**B85**	GND	**C85**	GND	**D85**	GND
A86	GND	**B86**	GND	**C86**	GND	**D86**	GND
A87	FPGA_CT47_LVDS2E_21P_RX_IO14	**B87**	FPGA_CY47_LVDS2E_21P_TX_IO12	**C87**	FPGA_DB53_LVDS2E_22P_RX_IO10	**D87**	FPGA_DD53_LVDS2E_22P_TX_IO8
A88	FPGA_CU48_LVDS2E_21N_RX_IO15	**B88**	FPGA_CW48_LVDS2E_21N_TX_IO13	**C88**	FPGA_DA54_LVDS2E_22N_RX_IO11	**D88**	FPGA_DE54_LVDS2E_22N_TX_IO9
A89	GND	**B89**	GND	**C89**	GND	**D89**	GND
A90	GND	**B90**	GND	**C90**	GND	**D90**	GND
A91	NC	**B91**	NC	**C91**	FPGA_CT49_LVDS2E_20P_RX_IO18/CLKOUT_0P	**D91**	FPGA_CY49_LVDS2E_20P_TX_IO16
A92	NC	**B92**	NC	**C92**	FPGA_CU50_LVDS2E_20N_RX_IO19/CLKOUT_0N	**D92**	FPGA_CW50_LVDS2E_20N_TX_IO17
A93	GND	**B93**	GND	**C93**	GND	**D93**	GND
A94	GND	**B94**	GND	**C94**	GND	**D94**	GND
A95	FPGA_A42_LVDS3C_6P_TX_IO72/CLKIN_1P	**B95**	FPGA_A44_LVDS3C_7P_TX_IO68	**C95**	FPGA_CT51_LVDS2E_19P_RX_IO22/CLKIN_0P	**D95**	NC
A96	FPGA_B43_LVDS3C_6N_TX_IO73/CLKIN_1N	**B96**	FPGA_B45_LVDS3C_7N_TX_IO69	**C96**	FPGA_CU52_LVDS2E_19N_RX_IO23/CLKIN_0N	**D96**	NC
A97	GND	**B97**	GND	**C97**	GND	**D97**	GND
A98	GND	**B98**	GND	**C98**	GND	**D98**	GND
A99	TEMPDIODE_13C_GXF_DP	**B99**	VCC_1V2_IO_2E	**C99**	TEMPDIODE_12A_GXF_DP	**D99**	TEMPDIODE_12C_GXF_DP
A100	TEMPDIODE_13C_GXF_DN	**B100**	VCC_1V2_IO	**C100**	TEMPDIODE_12A_GXF_DN	**D100**	TEMPDIODE_12C_GXF_DN

2.6.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Intel Agilex 7 SoC and FPGA is explained in the following section.

2.6.2 FPGA IOs & General-Purpose Clocks – Bank2D

The Intel Agilex 7 SoC and FPGA SOM supports up to 7 LVDS or 15 Single Ended IOs and from Intel Agilex 7 FPGA Bank2D on Board-to-Board connector1. In Intel Agilex 7 SoC and FPGA SOM, Bank2D signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank2D signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

In Intel Agilex 7 SoC and FPGA SOM, upon these 7 LVDS or 15 Single Ended IOs from Intel Agilex 7 FPGA Bank2D, one General Purpose Clock input LVDS pair and oneGeneral Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Intel Agilex 7 SoC and FPGA SOM, Bank2D I/O voltage is set to **1.2V** as the remaining bank IOs are used for FPGA1 DDR4 support.

For more details on Intel Agilex 7 SoC and FPGA Bank2D pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B84	FPGA_CL24_LVDS2D_13N_RX_IO47	IO47, CDR, DIFF_RX_2D13N/ CL24	IO, 1.2V LVDS	Bank2D 13n Rx differential Negative. Same pin can be configured as Single ended I/O.
B83	FPGA_CM23_LVDS2D_13P_RX_IO46	IO46, CDR, DIFF_RX_2D13P/ CM23	IO, 1.2V LVDS	Bank2D 13p Rx differential Positive. Same pin can be configured as Single ended I/O.
A84	FPGA_CR24_LVDS2D_13N_TX_IO45	IO45, CDR, DIFF_RX_2D13N/ CR24	IO, 1.2V LVDS	Bank2D 13n Rx differential Negative. Same pin can be configured as Single ended I/O.
A83	FPGA_CP23_LVDS2D_13P_TX_IO44	IO44, DIFF_TX_2D13P/ CP23	IO, 1.2V LVCMOS	Bank2D 13p Rx differential Positive. Same pin can be configured as Single ended I/O.
B52	FPGA_CU24_LVDS2D_16N_RX_IO35	IO35, CDR, DIFF_RX_2D16N/ CU24	IO, 1.2V LVDS	Bank2D 16n Rx differential Negative. Same pin can be configured as Single ended I/O.
B51	FPGA_CT23_LVDS2D_16P_RX_IO34	IO34, CDR, DIFF_RX_2D16P/ CT23	IO, 1.2V LVDS	Bank2D 16p Rx differential Positive. Same pin can be configured as Single ended I/O.
B54	FPGA_CW24_LVDS2D_16N_TX_IO33	IO33, DIFF_TX_2D16N/ CW24	IO, 1.2V LVDS	Bank2D 16n Tx differential Negative. Same pin can be configured as Single ended I/O.
B53	FPGA_CY23_LVDS2D_16P_TX_IO32	IO32, DIFF_TX_2D16P/ CY23	IO, 1.2V LVDS	Bank2D 16p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B56	FPGA_CU28_LVDS2D_18N_RX_IO27	IO27, CDR, DIFF_RX_2D18N/ CU28	IO, 1.2V LVDS	Bank2D 18n Rx differential Negative. Same pin can be configured as Single ended I/O.
B55	FPGA_CT27_LVDS2D_18P_RX_IO26	IO26, RZQ_B_2D, CDR, DIFF_RX_2D18P/ CT27	IO, 1.2V LVDS	Bank2D 18p Rx differential Positive. Same pin can be configured as Single ended I/O.
A52	FPGA_CW26_LVDS2D_17N_TX_IO29/CLKOUT_1N	IO29, PLL_2D_B_CLKOUT1N, DIFF_TX_2D17N/ CW26	IO, 1.2V LVDS	Bank2D 17n Tx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
A51	FPGA_CY25_LVDS2D_17P_TX_IO28/CLKOUT_1P	IO28, PLL_2D_B_CLKOUT1P, PLL_2D_B_CLKOUT1, PLL_2D_B_FB1, DIFF_TX_2D17P/ CY25	IO, 1.2V LVDS	Bank2D 17p Tx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
A54	FPGA_CU26_LVDS2D_17N_RX_IO31	IO31, DIFF_RX_2D17N/ CU26	IO, 1.2V LVDS	Bank2D 17n Rx differential Negative. Same pin can be configured as Single ended I/O.
A53	FPGA_CT25_LVDS2D_17P_RX_IO30	IO30, DIFF_RX_2D17P/ CT25	IO, 1.2V LVDS	Bank2D 17p Rx differential Positive. Same pin can be configured as Single ended I/O.

2.6.3 FPGA IOs & General-Purpose Clocks – Bank2E

The Intel Agilex 7 SoC and FPGA SOM supports up to 36 LVDS or 72 Single Ended IOs and from Intel Agilex 7 FPGA Bank2E on Board-to-Board connector1. In Intel Agilex 7 SoC and FPGA SOM, Bank2E signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank2E signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

In Intel Agilex 7 SoC and FPGA SOM, upon these 36 LVDS or 72 Single Ended IOs from Intel Agilex 7 FPGA Bank2D, three General Purpose Clock input LVDS pair and three General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Intel Agilex 7 SoC and FPGA SOM, Bank2E I/O voltage is set to **1.2V**. Contact iWave if **1.5V** voltage support is required.

For more details on Intel Agilex 7 SoC and FPGA Bank2E pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D92	FPGA_CW50_LVDS2E_20N_TX_IO17	IO17, DIFF_TX_2E20N/ CW50	IO, 1.2V/1.5V LVDS	Bank2E 20n Tx differential Negative. Same pin can be configured as Single ended I/O.
D91	FPGA_CY49_LVDS2E_20P_TX_IO16	IO16, DIFF_TX_2E20P/ CY49	IO, 1.2V/1.5V LVDS	Bank2E 20p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C92	FPGA_CU50_LVDS2E_20N_RX_IO19/CLKOUT_0N	IO19, PLL_2E_B_CLKOUT0N, DIFF_RX_2E20N/ CU50	IO, 1.2V LVDS	Bank2E 20n Rx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
C91	FPGA_CT49_LVDS2E_20P_RX_IO18/CLKOUT_0P	IO18, PLL_2E_B_CLKOUT0P, PLL_2E_B_CLKOUT0, PLL_2E_B_FB0, DIFF_RX_2E20P/ CT49	IO, 1.2V LVDS	Bank2E 20p Rx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
D88	FPGA_DE54_LVDS2E_22N_TX_IO9	IO9, DIFF_TX_2E22N/ DE54	IO, 1.2V LVDS	Bank2E 22n Tx differential Negative. Same pin can be configured as Single ended I/O.
D87	FPGA_DD53_LVDS2E_22P_TX_IO8	IO8, DIFF_TX_2E22P/ DD53	IO, 1.2V LVDS	Bank2E 22p Tx differential Positive. Same pin can be configured as Single ended I/O.
C88	FPGA_DA54_LVDS2E_22N_RX_IO11	IO11, CDR, DIFF_RX_2E22N/ DA54	IO, 1.2V LVDS	Bank2E 22n Rx differential Negative. Same pin can be configured as Single ended I/O.
C87	FPGA_DB53_LVDS2E_22P_RX_IO10	IO10, CDR, DIFF_RX_2E22P/ DB53	IO, 1.2V LVDS	Bank2E 22p Rx differential Positive. Same pin can be configured as Single ended I/O.
B88	FPGA_CW48_LVDS2E_21N_TX_IO13	IO13, DIFF_TX_2E21N/ CW48	IO, 1.2V LVDS	Bank2E 21n Tx differential Negative. Same pin can be configured as Single ended I/O.
B87	FPGA_CY47_LVDS2E_21P_TX_IO12	IO12, DIFF_TX_2E21P/ CY47	IO, 1.2V LVDS	Bank2E 21p Tx differential Positive. Same pin can be configured as Single ended I/O.
A88	FPGA_CU48_LVDS2E_21N_RX_IO15	IO15, CDR, DIFF_RX_2E21N/ CU48	IO, 1.2V LVDS	Bank2E 21n Rx differential Negative. Same pin can be configured as Single ended I/O.
A87	FPGA_CT47_LVDS2E_21P_RX_IO14	IO14, CDR, DIFF_RX_2E21P/ CT47	IO, 1.2V LVDS	Bank2E 21p Rx differential Positive. Same pin can be configured as Single ended I/O.
C96	FPGA_CU52_LVDS2E_19N_RX_IO23/CLKIN_0N	IO23, CLK_B_2E_0N, CDR, DIFF_RX_2E19N/ CU52	IO, 1.2V LVDS	Bank2E 19n Rx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
C95	FPGA_CT51_LVDS2E_19P_RX_IO22/CLKIN_0P	IO22, CLK_B_2E_0P, CDR, DIFF_RX_2E19P/ CT51	IO, 1.2V LVDS	Bank2E 19p Rx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D3	FPGA_DJ60_LVDS2E_4N_TX_IO81	IO81, DIFF_TX_2E4N/ DJ60	IO, 1.2V LVDS	Bank2E 4n Tx differential Negative. Same pin can be configured as Single ended I/O.
D2	FPGA_DK59_LVDS2E_4P_TX_IO80	IO80, DIFF_TX_2E4P/ DK59	IO, 1.2V LVDS	Bank2E 4p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D5	FPGA_DL60_LVDS2E_3N_RX_IO87	IO87, CDR, DIFF_RX_2E3N/ DL60	IO, 1.2V/1.5V LVDS	Bank2E 3n Rx differential Negative. Same pin can be configured as Single ended I/O.
D4	FPGA_DM59_LVDS2E_3P_RX_IO86	IO86, CDR, DIFF_RX_2E3P/ DM59	IO, 1.2V/1.5V LVDS	Bank2E 3p Rx differential Positive. Same pin can be configured as Single ended I/O.
D7	FPGA_DR60_LVDS2E_3N_TX_IO85	IO85, DIFF_TX_2E3N/ DR60	IO, 1.2V/1.5V LVDS	Bank2E 3n Tx differential Negative. Same pin can be configured as Single ended I/O.
D6	FPGA_DP59_LVDS2E_3P_TX_IO84	IO84, DIFF_TX_2E3P/ DP59	IO, 1.2V/1.5V LVDS	Bank2E 3p Tx differential Positive. Same pin can be configured as Single ended I/O.
C3	FPGA_DG60_LVDS2E_4N_RX_IO83	IO83, DIFF_RX_2E4N/ DG60	IO, 1.2V/1.5V LVDS	Bank2E 4n Rx differential Negative. Same pin can be configured as Single ended I/O.
C2	FPGA_DF59_LVDS2E_4P_RX_IO82	IO82, DIFF_RX_2E4P/ DF59	IO, 1.2V/1.5V LVDS	Bank2E 4p Rx differential Positive. Same pin can be configured as Single ended I/O.
C5	FPGA_DL62_LVDS2E_2N_RX_IO91	IO91, DIFF_RX_2E2N/ DL62	IO, 1.2V/1.5V LVDS	Bank2E 2n Rx differential Negative. Same pin can be configured as Single ended I/O.
C4	FPGA_DM61_LVDS2E_2P_RX_IO90	IO90, DIFF_RX_2E2P/ DM61	IO, 1.2V/1.5V LVDS	Bank2E 2p Rx differential Positive. Same pin can be configured as Single ended I/O.
C7	FPGA_DR64_LVDS2E_1N_TX_IO93	IO93, DIFF_TX_2E1N/ DR64	IO, 1.2V/1.5V LVDS	Bank2E 1n Tx differential Negative. Same pin can be configured as Single ended I/O.
C6	FPGA_DP63_LVDS2E_1P_TX_IO92	IO92, DIFF_TX_2E1P/ DP63	IO, 1.2V/1.5V LVDS	Bank2E 1p Tx differential Positive. Same pin can be configured as Single ended I/O.
B3	FPGA_DR62_LVDS2E_2N_TX_IO89	IO89, DIFF_TX_2E2N/ DR62	IO, 1.2V/1.5V LVDS	Bank2E 2n Tx differential Negative. Same pin can be configured as Single ended I/O.
B2	FPGA_DP61_LVDS2E_2P_TX_IO88	IO88, DIFF_TX_2E2P/ DP61	IO, 1.2V/1.5V LVDS	Bank2E 2p Tx differential Positive. Same pin can be configured as Single ended I/O.
B5	FPGA_DL64_LVDS2E_1N_RX_IO95	IO95, DIFF_RX_2E1N/ DL64	IO, 1.2V LVDS	Bank2E 1n Rx differential Negative. Same pin can be configured as Single ended I/O.
B4	FPGA_DM63_LVDS2E_1P_RX_IO94	IO94, DIFF_RX_2E1P/ DM63	IO, 1.2V/1.5V LVDS	Bank2E 1p Rx differential Positive. Same pin can be configured as Single ended I/O.
B7	FPGA_DG56_LVDS2E_6N_RX_IO75	IO75, CDR, DIFF_RX_2E6N/ DG56	IO, 1.2V/1.5V LVDS	Bank2E 6n Rx differential Negative. Same pin can be configured as Single ended I/O.
B6	FPGA_DF55_LVDS2E_6P_RX_IO74	IO74, RZQ_T_2E, CDR, DIFF_RX_2E6P/ DF55	IO, 1.2V/1.5V LVDS	Bank2E 6p Rx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A3	FPGA_DJ58_LVDS2E_5N_TX_IO77/CLKOUT_1N	IO77, PLL_2E_T_CLKOUT1N, DIFF_TX_2E5N/ DJ58	IO, 1.2V/1.5V LVDS	Bank2E 5n Tx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
A2	FPGA_DK57_LVDS2E_5P_TX_IO76/CLKOUT_1P	IO76, PLL_2E_T_CLKOUT1P, PLL_2E_T_CLKOUT1, PLL_2E_T_FB1, DIFF_TX_2E5P/ DK57	IO, 1.2V/1.5V LVDS	Bank2E 5p Tx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
A5	FPGA_DG58_LVDS2E_5N_RX_IO79	IO79, DIFF_RX_2E5N/ DG58	IO, 1.2V/1.5V LVDS	Bank2E 5n Rx differential Negative. Same pin can be configured as Single ended I/O.
A4	FPGA_DF57_LVDS2E_5P_RX_IO78	IO78, DIFF_RX_2E5P/ DF57	IO, 1.2V/1.5V LVDS	Bank2E 5p Rx differential Positive. Same pin can be configured as Single ended I/O.
A7	FPGA_DJ56_LVDS2E_6N_TX_IO73/CLKIN_1N	IO73, CLK_T_2E_1N, DIFF_TX_2E6N/ DJ56	IO, 1.2V/1.5V LVDS	Bank2E 6n Tx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
A6	FPGA_DK55_LVDS2E_6P_TX_IO72/CLKIN_1P	IO72, CLK_T_2E_1P, DIFF_TX_2E6P/ DK55	IO, 1.2V/1.5V LVDS	Bank2E 6p Tx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D10	FPGA_DL58_LVDS2E_7N_RX_IO71/CLKIN_0N	IO71, CLK_T_2E_0N, DIFF_RX_2E7N/ DL58	IO, 1.2V/1.5V LVDS	Bank2E 7n Rx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
D9	FPGA_DM57_LVDS2E_7P_RX_IO70/CLKIN_0P	IO70, CLK_T_2E_0P, DIFF_RX_2E7P/ DM57	IO, 1.2V/1.5V LVDS	Bank2E 7p Rx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D12	FPGA_DR58_LVDS2E_7N_TX_IO69	IO69, DIFF_TX_2E7N/ DR58	IO, 1.2V/1.5V LVDS	Bank2E 7n Tx differential Negative. Same pin can be configured as Single ended I/O.
D11	FPGA_DP57_LVDS2E_7P_TX_IO68	IO68, DIFF_TX_2E7P/ DP57	IO, 1.2V/1.5V LVDS	Bank2E 7p Tx differential Positive. Same pin can be configured as Single ended I/O.
D14	FPGA_DL56_LVDS2E_8N_RX_IO67/CLKOUT_0N	IO67, PLL_2E_T_CLKOUT0N, DIFF_RX_2E8N/ DL56	IO, 1.2V/1.5V LVDS	Bank2E 8n Rx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
D13	FPGA_DM55_LVDS2E_8P_RX_IO66/CLKOUT_0P	IO66, PLL_2E_T_CLKOUT0P, PLL_2E_T_CLKOUT0, PLL_2E_T_FB0, DIFF_RX_2E8P/ DM55	IO, 1.2V/1.5V LVDS	Bank2E 8p Rx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
C10	FPGA_DR56_LVDS2E_8N_TX_IO65	IO65, DIFF_TX_2E8N/ DR56	IO, 1.2V/1.5V LVDS	Bank2E 8n Tx differential Negative. Same pin can be configured as Single ended I/O.
C9	FPGA_DP55_LVDS2E_8P_TX_IO64	IO64, DIFF_TX_2E8P/ DP55	IO, 1.2V/1.5V LVDS	Bank2E 8p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C12	FPGA_DL54_LVDS2E_9N_RX_IO63	IO63, CDR, DIFF_RX_2E9N/ DL54	IO, 1.2V/1.5V LVDS	Bank2E 9n Rx differential Negative. Same pin can be configured as Single ended I/O.
C11	FPGA_DM53_LVDS2E_9P_RX_IO62	IO62, CDR, DIFF_RX_2E9P/ DM53	IO, 1.2V/1.5V LVDS	Bank2E 9p Rx differential Positive. Same pin can be configured as Single ended I/O.
C14	FPGA_DJ54_LVDS2E_10N_TX_IO57	IO57, DIFF_TX_2E10N/ DJ54	IO, 1.2V/1.5V LVDS	Bank2E 10n Tx differential Negative. Same pin can be configured as Single ended I/O.
C13	FPGA_DK53_LVDS2E_10P_TX_IO56	IO56, DIFF_TX_2E10P/ DK53	IO, 1.2V/1.5V LVDS	Bank2E 10p Tx differential Positive. Same pin can be configured as Single ended I/O.
B10	FPGA_DG54_LVDS2E_10N_RX_IO59	IO59, DIFF_RX_2E10N/ DG54	IO, 1.2V/1.5V LVDS	Bank2E 10n Rx differential Negative. Same pin can be configured as Single ended I/O.
B9	FPGA_DF53_LVDS2E_10P_RX_IO58	IO58, DIFF_RX_2E10P/ DF53	IO, 1.2V/1.5V LVDS	Bank2E 10p Rx differential Positive. Same pin can be configured as Single ended I/O.
B12	FPGA_DR54_LVDS2E_9N_TX_IO61	IO61, DIFF_TX_2E9N/ DR54	IO, 1.2V/1.5V LVDS	Bank2E 9n Tx differential Negative. Same pin can be configured as Single ended I/O.
B11	FPGA_DP53_LVDS2E_9P_TX_IO60	IO60, DIFF_TX_2E9P/ DP53	IO, 1.2V/1.5V LVDS	Bank2E 9p Tx differential Positive. Same pin can be configured as Single ended I/O.
B14	FPGA_DJ52_LVDS2E_11N_TX_IO53	IO53, DIFF_TX_2E11N/ DJ52	IO, 1.2V/1.5V LVDS	Bank2E 11n Tx differential Negative. Same pin can be configured as Single ended I/O.
B13	FPGA_DK51_LVDS2E_11P_TX_IO52	IO52, DIFF_TX_2E11P/ DK51	IO, 1.2V/1.5V LVDS	Bank2E 11p Tx differential Positive. Same pin can be configured as Single ended I/O.
A10	FPGA_DG52_LVDS2E_11N_RX_IO55	IO55, DIFF_RX_2E11N/ DG52	IO, 1.2V/1.5V LVDS	Bank2E 11n Rx differential Negative. Same pin can be configured as Single ended I/O.
A9	FPGA_DF51_LVDS2E_11P_RX_IO54	IO54, DIFF_RX_2E11P/ DF51	IO, 1.2V/1.5V LVDS	Bank2E 11p Rx differential Positive. Same pin can be configured as Single ended I/O.
A12	FPGA_DG50_LVDS2E_12N_RX_IO51	IO51, CDR, DIFF_RX_2E12N/ DG50	IO, 1.2V/1.5V LVDS	Bank2E 12n Rx differential Negative. Same pin can be configured as Single ended I/O.
A11	FPGA_DF49_LVDS2E_12P_RX_IO50	IO50, CDR, DIFF_RX_2E12P/ DF49	IO, 1.2V/1.5V LVDS	Bank2E 12p Rx differential Positive. Same pin can be configured as Single ended I/O.
A14	FPGA_DJ50_LVDS2E_12N_TX_IO49	IO49, DIFF_TX_2E12N/ DJ50	IO, 1.2V/1.5V LVDS	Bank2E 12n Tx differential Negative. Same pin can be configured as Single ended I/O.
A13	FPGA_DK49_LVDS2E_12P_TX_IO48	IO48, DIFF_TX_2E12P/ DK49	IO, 1.2V/1.5V LVDS	Bank2E 12p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D76	FPGA_DE50_LVDS2E_24N_TX_IO1	IO1, DIFF_TX_2E24N/ DE50	IO, 1.2V/1.5V LVDS	Bank2E 24n Tx differential Negative. Same pin can be configured as Single ended I/O.
D75	FPGA_DD49_LVDS2E_24P_TX_IO0	IO0, DIFF_TX_2E24P/ DD49	IO, 1.2V/1.5V LVDS	Bank2E 24p Tx differential Positive. Same pin can be configured as Single ended I/O.
C76	FPGA_DA50_LVDS2E_24N_RX_IO3	IO3, CDR, DIFF_RX_2E24N/ DA50	IO, 1.2V/1.5V LVDS	Bank2E 24n Rx differential Negative. Same pin can be configured as Single ended I/O.
C75	FPGA_DB49_LVDS2E_24P_RX_IO2	IO2, CDR, DIFF_RX_2E24P/ DB49	IO, 1.2V/1.5V LVDS	Bank2E 24p Rx differential Positive. Same pin can be configured as Single ended I/O.
B76	FPGA_DE52_LVDS2E_23N_TX_IO5	IO5, DIFF_TX_2E23N/ DE52	IO, 1.2V/1.5V LVDS	Bank2E 23n Tx differential Negative. Same pin can be configured as Single ended I/O.
B75	FPGA_DD51_LVDS2E_23P_TX_IO4	IO4, DIFF_TX_2E23P/ DD51	IO, 1.2V/1.5V LVDS	Bank2E 23p Tx differential Positive. Same pin can be configured as Single ended I/O.
A76	FPGA_DA52_LVDS2E_23N_RX_IO7	IO7, DIFF_RX_2E23N/ DA52	IO, 1.2V/1.5V LVDS	Bank2E 23n Rx differential Negative. Same pin can be configured as Single ended I/O.
A75	FPGA_DB51_LVDS2E_23P_RX_IO6	IO6, DIFF_RX_2E23P/ DB51	IO, 1.2V/1.5V LVDS	Bank2E 23p Rx differential Positive. Same pin can be configured as Single ended I/O.
C60	FPGA_CW52_LVDS2E_19N_TX_IO21	IO21, DIFF_TX_2E19N/ CW52	IO, 1.2V/1.5V LVDS	Bank2E 19n Tx differential Negative. Same pin can be configured as Single ended I/O.
C59	FPGA_CY51_LVDS2E_19P_TX_IO20	IO20, DIFF_TX_2E19P/ CY51	IO, 1.2V/1.5V LVDS	Bank2E 19p Tx differential Positive. Same pin can be configured as Single ended I/O.

2.6.4 FPGA IOs & General-Purpose Clocks – Bank2F

The Intel Agilex 7 SoC and FPGA SOM supports up to 48 LVDS or 96 Single Ended IOs and from Intel Agilex 7 FPGA Bank2F on Board-to-Board connector1. In Intel Agilex 7 SoC and FPGA SOM, Bank2F signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank2F signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

In Intel Agilex 7 SoC and FPGA SOM, upon these 48 LVDS or 96 Single Ended IOs from Intel Agilex 7 FPGA Bank2D, four General Purpose Clock input LVDS pair and four General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Intel Agilex 7 SoC and FPGA SOM, Bank2F I/O voltage is set to **1.2V**. Contact iWave if **1.5V** voltage support is required.

For more details on Intel Agilex 7 SoC and FPGA Bank2F pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D17	FPGA_DG38_LVDS2F_1N_RX_IO95	IO95, DIFF_RX_2F1N/ DG38	IO, 1.2V/1.5V LVDS	Bank2F 1n Rx differential Negative. Same pin can be configured as Single ended I/O.
D16	FPGA_DF37_LVDS2F_1P_RX_IO94	IO94, DIFF_RX_2F1P/ DF37	IO, 1.2V/1.5V LVDS	Bank2F 1p Rx differential Positive. Same pin can be configured as Single ended I/O.
D19	FPGA_DJ38_LVDS2F_1N_TX_IO93	IO93, DIFF_TX_2F1N/ DJ38	IO, 1.2V/1.5V LVDS	Bank2F 1n Tx differential Negative. Same pin can be configured as Single ended I/O.
D18	FPGA_DK37_LVDS2F_1P_TX_IO92	IO92, DIFF_TX_2F1P/ DK37	IO, 1.2V/1.5V LVDS	Bank2F 1p Tx differential Positive. Same pin can be configured as Single ended I/O.
D21	FPGA_DG40_LVDS2F_2N_RX_IO91	IO91, DIFF_RX_2F2N/ DG40	IO, 1.2V/1.5V LVDS	Bank2F 2n Rx differential Negative. Same pin can be configured as Single ended I/O.
D20	FPGA_DF39_LVDS2F_2P_RX_IO90	IO90, DIFF_RX_2F2P/ DF39	IO, 1.2V/1.5V LVDS	Bank2F 2p Rx differential Positive. Same pin can be configured as Single ended I/O.
C17	FPGA_DJ40_LVDS2F_2N_TX_IO89	IO89, DIFF_TX_2F2N/ DJ40	IO, 1.2V/1.5V LVDS	Bank2F 2n Tx differential Negative. Same pin can be configured as Single ended I/O.
C16	FPGA_DK39_LVDS2F_2P_TX_IO88	IO88, DIFF_TX_2F2P/ DK39	IO, 1.2V/1.5V LVDS	Bank2F 2p Tx differential Positive. Same pin can be configured as Single ended I/O.
C19	FPGA_DG42_LVDS2F_3N_RX_IO87	IO87, CDR, DIFF_RX_2F3N/ DG42	IO, 1.2V/1.5V LVDS	Bank2F 3n Rx differential Negative. Same pin can be configured as Single ended I/O.
C18	FPGA_DF41_LVDS2F_3P_RX_IO86	IO86, CDR, DIFF_RX_2F3P/ DF41	IO, 1.2V/1.5V LVDS	Bank2F 3p Rx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C21	FPGA_DJ42_LVDS2F_3N_TX_IO85	IO85, DIFF_TX_2F3N/ DJ42	IO, 1.2V/1.5V LVDS	Bank2F 3n Tx differential Negative. Same pin can be configured as Single ended I/O.
C20	FPGA_DK41_LVDS2F_3P_TX_IO84	IO84, DIFF_TX_2F3P/ DK41	IO, 1.2V/1.5V LVDS	Bank2F 3p Tx differential Positive. Same pin can be configured as Single ended I/O.
B17	FPGA_DL42_LVDS2F_4N_RX_IO83	IO83, DIFF_RX_2F4N/ DL42	IO, 1.2V/1.5V LVDS	Bank2F 4n Rx differential Negative. Same pin can be configured as Single ended I/O.
B16	FPGA_DM41_LVDS2F_4P_RX_IO82	IO82, DIFF_RX_2F4P/ DM41	IO, 1.2V/1.5V LVDS	Bank2F 4p Rx differential Positive. Same pin can be configured as Single ended I/O.
B19	FPGA_DR42_LVDS2F_4N_TX_IO81	IO81, DIFF_TX_2F4N/ DR42	IO, 1.2V/1.5V LVDS	Bank2F 4n Tx differential Negative. Same pin can be configured as Single ended I/O.
B18	FPGA_DP41_LVDS2F_4P_TX_IO80	IO80, DIFF_TX_2F4P/ DP41	IO, 1.2V/1.5V LVDS	Bank2F 4p Tx differential Positive. Same pin can be configured as Single ended I/O.
B21	FPGA_DL44_LVDS2F_5N_RX_IO79	IO79, DIFF_RX_2F5N/ DL44	IO, 1.2V/1.5V LVDS	Bank2F 5n Rx differential Negative. Same pin can be configured as Single ended I/O.
B20	FPGA_DM43_LVDS2F_5P_RX_IO78	IO78, DIFF_RX_2F5P/ DM43	IO, 1.2V/1.5V LVDS	Bank2F 5p Rx differential Positive. Same pin can be configured as Single ended I/O.
A17	FPGA_BR44_LVDS2F_5N_TX_IO77/CLKOUT_1N	IO77, PLL_2F_T_CLKOUT1N, DIFF_TX_2F5N/ DR44	IO, 1.2V/1.5V LVDS	Bank2F 5n Tx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
A16	FPGA_DP43_LVDS2F_5P_TX_IO76/CLKOUT_1P	IO76, PLL_2F_T_CLKOUT1P, PLL_2F_T_CLKOUT1, PLL_2F_T_FB1, DIFF_TX_2F5P/ DP43	IO, 1.2V/1.5V LVDS	Bank2F 5p Tx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
A19	FPGA_DL46_LVDS2F_6N_RX_IO75	IO75, CDR, DIFF_RX_2F6N/ DL46	IO, 1.2V/1.5V LVDS	Bank2F 6n Rx differential Negative. Same pin can be configured as Single ended I/O.
A18	FPGA_DM45_LVDS2F_6P_RX_IO74	IO74, RZQ_T_2F, CDR, DIFF_RX_2F6P/ DM45	IO, 1.2V/1.5V LVDS	Bank2F 6p Rx differential Positive. Same pin can be configured as Single ended I/O.
A21	FPGA_DR46_LVDS2F_6N_TX_IO73/CLKIN_1N	IO73, CLK_T_2F_1N, DIFF_TX_2F6N/ DR46	IO, 1.2V/1.5V LVDS	Bank2F 6n Tx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
A20	FPGA_DP45_LVDS2F_6P_TX_IO72/CLKIN_1P	IO72, CLK_T_2F_1P, DIFF_TX_2F6P/ DP45	IO, 1.2V/1.5V LVDS	Bank2F 6p Tx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D24	FPGA_DG44_LVDS2F_7N_RX_IO71/CLKIN_0N	IO71, CLK_T_2F_0N, DIFF_RX_2F7N/ DG44	IO, 1.2V/1.5V LVDS	Bank2F 7n Rx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
D23	FPGA_DF43_LVDS2F_7P_RX_IO70/CLKIN_0P	IO70, CLK_T_2F_0P, DIFF_RX_2F7P/ DF43	IO, 1.2V/1.5V LVDS	Bank2F 7p Rx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D26	FPGA_DK43_LVDS2F_7N_TX_IO69	IO69, DIFF_TX_2F7N/ DK43	IO, 1.2V/1.5V LVDS	Bank2F 7n Tx differential Negative. Same pin can be configured as Single ended I/O.
D25	FPGA_DJ44_LVDS2F_7P_TX_IO68	IO68, DIFF_TX_2F7P/ DJ44	IO, 1.2V/1.5V LVDS	Bank2F 7p Tx differential Positive. Same pin can be configured as Single ended I/O.
D28	FPGA_DG46_LVDS2F_8N_RX_IO67/CLKOUT_0N	IO67, PLL_2F_T_CLKOUT0N, DIFF_RX_2F8N/ DG46	IO, 1.2V/1.5V LVDS	Bank2F 8n Rx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
D27	FPGA_DF45_LVDS2F_8P_RX_IO66/CLKOUT_0P	IO66, PLL_2F_T_CLKOUT0P, PLL_2F_T_CLKOUT0, PLL_2F_T_FB0, DIFF_RX_2F8P/ DF45	IO, 1.2V/1.5V LVDS	Bank2F 8p Rx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
C24	FPGA_BJ46_LVDS2F_8N_TX_IO65	IO65, DIFF_TX_2F8N/ DJ46	IO, 1.2V/1.5V LVDS	Bank2F 8n Tx differential Negative. Same pin can be configured as Single ended I/O.
C23	FPGA_DK45_LVDS2F_8P_TX_IO64	IO64, DIFF_TX_2F8P/ DK45	IO, 1.2V/1.5V LVDS	Bank2F 8p Tx differential Positive. Same pin can be configured as Single ended I/O.
C26	FPGA_DL52_LVDS2F_12N_RX_IO51	IO51, CDR, DIFF_RX_2F12N/ DL52	IO, 1.2V/1.5V LVDS	Bank2F 12n Rx differential Negative. Same pin can be configured as Single ended I/O.
C25	FPGA_DM51_LVDS2F_12P_RX_IO50	IO50, CDR, DIFF_RX_2F12P/ DM51	IO, 1.2V/1.5V LVDS	Bank2F 12p Rx differential Positive. Same pin can be configured as Single ended I/O.
C28	FPGA_DR50_LVDS2F_11N_TX_IO53	IO53, DIFF_TX_2F11N/ DR50	IO, 1.2V/1.5V LVDS	Bank2F 11n Tx differential Negative. Same pin can be configured as Single ended I/O.
C27	FPGA_DP49_LVDS2F_11P_TX_IO52	IO52, DIFF_TX_2F11P/ DP49	IO, 1.2V/1.5V LVDS	Bank2F 11p Tx differential Positive. Same pin can be configured as Single ended I/O.
B24	FPGA_DR52_LVDS2F_12N_TX_IO49	IO49, DIFF_TX_2F12N/ DR52	IO, 1.2V/1.5V LVDS	Bank2F 12n Tx differential Negative. Same pin can be configured as Single ended I/O.
B23	FPGA_DP51_LVDS2F_12P_TX_IO48	IO48, DIFF_TX_2F12P/ DP51	IO, 1.2V/1.5V LVDS	Bank2F 12p Tx differential Positive. Same pin can be configured as Single ended I/O.
B26	FPGA_DL50_LVDS2F_11N_RX_IO55	IO55, DIFF_RX_2F11N/ DL50	IO, 1.2V/1.5V LVDS	Bank2F 11n Rx differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B25	FPGA_DM49_LVDS2F_11P_RX_IO54	IO54, DIFF_RX_2F11P/ DM49	IO, 1.2V/1.5V LVDS	Bank2F 11p Rx differential Positive. Same pin can be configured as Single ended I/O.
B28	FPGA_DG48_LVDS2F_9N_RX_IO63	IO63, CDR, DIFF_RX_2F9N/ DG48	IO, 1.2V/1.5V LVDS	Bank2F 9n Rx differential Negative. Same pin can be configured as Single ended I/O.
B27	FPGA_DF47_LVDS2F_9P_RX_IO62	IO62, CDR, DIFF_RX_2F9P/ DF47	IO, 1.2V/1.5V LVDS	Bank2F 9p Rx differential Positive. Same pin can be configured as Single ended I/O.
A24	FPGA_DL48_LVDS2F_10N_RX_IO59	IO59, DIFF_RX_2F10N/ DL48	IO, 1.2V/1.5V LVDS	Bank2F 10n Rx differential Negative. Same pin can be configured as Single ended I/O.
A23	FPGA_DM47_LVDS2F_10P_RX_IO58	IO58, DIFF_RX_2F10P/ DM47	IO, 1.2V/1.5V LVDS	Bank2F 10p Rx differential Positive. Same pin can be configured as Single ended I/O.
A26	FPGA_DR48_LVDS2F_10N_TX_IO57	IO57, DIFF_TX_2F10N/ DR48	IO, 1.2V/1.5V LVDS	Bank2F 10n Tx differential Negative. Same pin can be configured as Single ended I/O.
A25	FPGA_DP47_LVDS2F_10P_TX_IO56	IO56, DIFF_TX_2F10P/ DP47	IO, 1.2V/1.5V LVDS	Bank2F 10p Tx differential Positive. Same pin can be configured as Single ended I/O.
A28	FPGA_BJ48_LVDS2F_9N_TX_IO61	IO61, DIFF_TX_2F9N/ DJ48	IO, 1.2V/1.5V LVDS	Bank2F 9n Tx differential Negative. Same pin can be configured as Single ended I/O.
A27	FPGA_DK47_LVDS2F_9P_TX_IO60	I IO60, DIFF_TX_2F9P/ DK47	IO, 1.2V/1.5V LVDS	Bank2F 9p Tx differential Positive. Same pin can be configured as Single ended I/O.
D31	FPGA_CP45_LVDS2F_24N_TX_IO1	IO1, DIFF_TX_2F24N/ CP45	IO, 1.2V/1.5V LVDS	Bank2F 24n Tx differential Negative. Same pin can be configured as Single ended I/O.
D30	FPGA_CR46_LVDS2F_24P_TX_IO0	IO0, DIFF_TX_2F24P/ CR46	IO, 1.2V/1.5V LVDS	Bank2F 24p Tx differential Positive. Same pin can be configured as Single ended I/O.
D33	FPGA_CM45_LVDS2F_24N_RX_IO3	IO3, CDR, DIFF_RX_2F24N/ CM45	IO, 1.2V/1.5V LVDS	Bank2F 24n Rx differential Negative. Same pin can be configured as Single ended I/O.
D32	FPGA_CL46_LVDS2F_24P_RX_IO2	IO2, CDR, DIFF_RX_2F24P/ CL46	IO, 1.2V/1.5V LVDS	Bank2F 24p Rx differential Positive. Same pin can be configured as Single ended I/O.
D35	FPGA_CL44_LVDS2F_23N_RX_IO7	IO7, DIFF_RX_2F23N/ CL44	IO, 1.2V/1.5V LVDS	Bank2F 23n Rx differential Negative. Same pin can be configured as Single ended I/O.
D34	FPGA_CM43_LVDS2F_23P_RX_IO6	IO6, DIFF_RX_2F23P/ CM43	IO, 1.2V/1.5V LVDS	Bank2F 23p Rx differential Positive. Same pin can be configured as Single ended I/O.
C31	FPGA_CR44_LVDS2F_23N_TX_IO5	IO5, DIFF_TX_2F23N/ CR44	IO, 1.2V/1.5V LVDS	Bank2F 23n Tx differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C30	FPGA_CP43_LVDS2F_23P_TX_IO4	IO4, DIFF_TX_2F23P/ CP43	IO, 1.2V/1.5V LVDS	Bank2F 23p Tx differential Positive. Same pin can be configured as Single ended I/O.
C33	FPGA_DA42_LVDS2F_15N_RX_IO39	IO39, CDR, DIFF_RX_2F15N/ DA42	IO, 1.2V/1.5V LVDS	Bank2F 15n Rx differential Negative. Same pin can be configured as Single ended I/O.
C32	FPGA_DB41_LVDS2F_15P_RX_IO38	IO38, CDR, DIFF_RX_2F15P/ DB41	IO, 1.2V/1.5V LVDS	Bank2F 15p Rx differential Positive. Same pin can be configured as Single ended I/O.
C35	FPGA_DE42_LVDS2F_15N_TX_IO37	IO37, DIFF_TX_2F15N/ DE42	IO, 1.2V/1.5V LVDS	Bank2F 15n Tx differential Negative. Same pin can be configured as Single ended I/O.
C34	FPGA_DD41_LVDS2F_15P_TX_IO36	IO36, DIFF_TX_2F15P/ DD41	IO, 1.2V/1.5V LVDS	Bank2F 15p Tx differential Positive. Same pin can be configured as Single ended I/O.
B31	FPGA_DA44_LVDS2F_16N_RX_IO35	IO35, CDR, DIFF_RX_2F16N/ DA44	IO, 1.2V/1.5V LVDS	Bank2F 16n Rx differential Negative. Same pin can be configured as Single ended I/O.
B30	FPGA_DB43_LVDS2F_16P_RX_IO34	IO34, CDR, DIFF_RX_2F16P/ DB43	IO, 1.2V/1.5V LVDS	Bank2F 16p Rx differential Positive. Same pin can be configured as Single ended I/O.
B33	FPGA_BE44_LVDS2F_16N_TX_IO33	IO33, DIFF_TX_2F16N/ DE44	IO, 1.2V/1.5V LVDS	Bank2F 16n Tx differential Negative. Same pin can be configured as Single ended I/O.
B32	FPGA_DD43_LVDS2F_16P_TX_IO32	IO32, DIFF_TX_2F16P/ DD43	IO, 1.2V/1.5V LVDS	Bank2F 16p Tx differential Positive. Same pin can be configured as Single ended I/O.
B35	FPGA_DA46_LVDS2F_17N_RX_IO31	IO31, DIFF_RX_2F17N/ DA46	IO, 1.2V/1.5V LVDS	Bank2F 17n Rx differential Negative. Same pin can be configured as Single ended I/O.
B34	FPGA_DB45_LVDS2F_17P_RX_IO30	IO30, DIFF_RX_2F17P/ DB45	IO, 1.2V/1.5V LVDS	Bank2F 17p Rx differential Positive. Same pin can be configured as Single ended I/O.
A31	FPGA_DE46_LVDS2F_17N_TX_IO29/CLKOUT_1N	IO29, PLL_2F_B_CLKOUT1N, DIFF_TX_2F17N/ DE46	IO, 1.2V/1.5V LVDS	Bank2F 17n Tx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
A30	FPGA_DD45_LVDS2F_17P_TX_IO28/CLKOUT_1P	IO28, PLL_2F_B_CLKOUT1P, PLL_2F_B_CLKOUT1, PLL_2F_B_FB1, DIFF_TX_2F17P/ DD45	IO, 1.2V/1.5V LVDS	Bank2F 17p Tx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
A33	FPGA_DA48_LVDS2F_18N_RX_IO27	IO27, CDR, DIFF_RX_2F18N/ DA48	IO, 1.2V/1.5V LVDS	Bank2F 18n Rx differential Negative. Same pin can be configured as Single ended I/O.
A32	FPGA_DB47_LVDS2F_18P_RX_IO26	IO26, RZQ_B_2F, CDR, DIFF_RX_2F18P/ DB47	IO, 1.2V/1.5V LVDS	Bank2F 18p Rx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A35	FPGA_DE48_LVDS2F_18N_TX_IO25/CLKIN_1N	IO25, CLK_B_2F_1N, DIFF_TX_2F18N/ DE48	IO, 1.2V/1.5V LVDS	Bank2F 18n Tx differential Negative. Same pin can be configured as Clock input or Single ended I/O.
A34	FPGA_DD47_LVDS2F_18P_TX_IO24/CLKIN_1P	IO24, CLK_B_2F_1P, DIFF_TX_2F18P/ DD47	IO, 1.2V/1.5V LVDS	Bank2F 18p Tx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D38	FPGA_CT41_LVDS2F_19N_RX_IO23/CLKIN_0N	IO23, CLK_B_2F_0N, CDR, DIFF_RX_2F19N/ CT41	IO, 1.2V/1.5V LVDS	Bank2F 19n Rx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
D37	FPGA_CU42_LVDS2F_19P_RX_IO22/CLKIN_0P	IO22, CLK_B_2F_0P, CDR, DIFF_RX_2F19P/ CU42	IO, 1.2V/1.5V LVDS	Bank2F 19p Rx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D40	FPGA_CW44_LVDS2F_20N_TX_IO17	IO17, DIFF_TX_2F20N/ CW44	IO, 1.2V/1.5V LVDS	Bank2F 20n Tx differential Negative. Same pin can be configured as Single ended I/O.
D39	FPGA_CY43_LVDS2F_20P_TX_IO16	IO16, DIFF_TX_2F20P/ CY43	IO, 1.2V/1.5V LVDS	Bank2F 20p Tx differential Positive. Same pin can be configured as Single ended I/O.
D42	FPGA_CU44_LVDS2F_20N_RX_IO19/CLKOUT_0N	IO19, PLL_2F_B_CLKOUT0N, DIFF_RX_2F20N/ CU44	IO, 1.2V/1.5V LVDS	Bank2F 20n Rx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
D41	FPGA_CT43_LVDS2F_20P_RX_IO18/CLKOUT_0P	IO18, PLL_2F_B_CLKOUT0P, PLL_2F_B_CLKOUT0, PLL_2F_B_FB0, DIFF_RX_2F20P/ CT43	IO, 1.2V/1.5V LVDS	Bank2F 20p Rx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
C38	FPGA_CY41_LVDS2F_19N_TX_IO21	IO21, DIFF_TX_2F19N/ CY41	IO, 1.2V/1.5V LVDS	Bank2F 19n Tx differential Negative. Same pin can be configured as Single ended I/O.
C37	FPGA_CW42_LVDS2F_19P_TX_IO20	IO20, DIFF_TX_2F19P/ CW42	IO, 1.2V/1.5V LVDS	Bank2F 19p Tx differential Positive. Same pin can be configured as Single ended I/O.
C40	FPGA_CU46_LVDS2F_21N_RX_IO15	IO15, CDR, DIFF_RX_2F21N/ CU46	IO, 1.2V/1.5V LVDS	Bank2F 21n Rx differential Negative. Same pin can be configured as Single ended I/O.
C39	FPGA_CT45_LVDS2F_21P_RX_IO14	IO14, CDR, DIFF_RX_2F21P/ CT45	IO, 1.2V/1.5V LVDS	Bank2F 21p Rx differential Positive. Same pin can be configured as Single ended I/O.
C42	FPGA_CY45_LVDS2F_21N_TX_IO13	IO13, DIFF_TX_2F21N/ CY45	IO, 1.2V/1.5V LVDS	Bank2F 21n Tx differential Negative. Same pin can be configured as Single ended I/O.
C41	FPGA_CW46_LVDS2F_21P_TX_IO12	IO12, DIFF_TX_2F21P/ CW46	IO, 1.2V/1.5V LVDS	Bank2F 21p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B38	FPGA_CM41_LVDS2F_22N_RX_IO11	IO11, CDR, DIFF_RX_2F22N/ CM41	IO, 1.2V/1.5V LVDS	Bank2F 22n Rx differential Negative. Same pin can be configured as Single ended I/O.
B37	FPGA_CL42_LVDS2F_22P_RX_IO10	IO10, CDR, DIFF_RX_2F22P/ CL42	IO, 1.2V/1.5V LVDS	Bank2F 22p Rx differential Positive. Same pin can be configured as Single ended I/O.
B40	FPGA_CR42_LVDS2F_22N_TX_IO9	IO9, DIFF_TX_2F22N/ CR42	IO, 1.2V/1.5V LVDS	Bank2F 22n Tx differential Negative. Same pin can be configured as Single ended I/O.
B39	FPGA_CP41_LVDS2F_22P_TX_IO8	IO8, DIFF_TX_2F22P/ CP41	IO, 1.2V/1.5V LVDS	Bank2F 22p Tx differential Positive. Same pin can be configured as Single ended I/O.
B42	FPGA_DA38_LVDS2F_13N_RX_IO47	IO47, CDR, DIFF_RX_2F13N/ DA38	IO, 1.2V/1.5V LVDS	Bank2F 13n Rx differential Negative. Same pin can be configured as Single ended I/O.
B41	FPGA_DB37_LVDS2F_13P_RX_IO46	IO46, CDR, DIFF_RX_2F13P/ DB37	IO, 1.2V/1.5V LVDS	Bank2F 13p Rx differential Positive. Same pin can be configured as Single ended I/O.
A38	FPGA_DE40_LVDS2F_14N_TX_IO41	IO41, DIFF_TX_2F14N/ DE40	IO, 1.2V/1.5V LVDS	Bank2F 14n Tx differential Negative. Same pin can be configured as Single ended I/O.
A37	FPGA_DD39_LVDS2F_14P_TX_IO40	IO40, DIFF_TX_2F14P/ DD39	IO, 1.2V/1.5V LVDS	Bank2F 14p Tx differential Positive. Same pin can be configured as Single ended I/O.
A40	FPGA_DA40_LVDS2F_14N_RX_IO43	IO43, DIFF_RX_2F14N/ DA40	IO, 1.2V/1.5V LVDS	Bank2F 14n Rx differential Negative. Same pin can be configured as Single ended I/O.
A39	FPGA_DB39_LVDS2F_14P_RX_IO42	IO42, DIFF_RX_2F14P/ DB39	IO, 1.2V/1.5V LVDS	Bank2F 14p Rx differential Positive. Same pin can be configured as Single ended I/O.
A42	FPGA_DE38_LVDS2F_13N_TX_IO45	IO45, DIFF_TX_2F13N/ DE38	IO, 1.2V/1.5V LVDS	Bank2F 13n Tx differential Negative. Same pin can be configured as Single ended I/O.
A41	FPGA_DD37_LVDS2F_13P_TX_IO44	IO44, DIFF_TX_2F13P/ DD37	IO, 1.2V/1.5V LVDS	Bank2F 13p Tx differential Positive. Same pin can be configured as Single ended I/O.

2.6.5 FPGA IOs & General-Purpose Clocks – Bank3B

The Intel Agilex 7 SoC and FPGA SOM supports up to 18 LVDS or 36 Single Ended IOs and from Intel Agilex 7 FPGA Bank3B on Board-to-Board connector1. In Intel Agilex 7 SoC and FPGA SOM, Bank3B signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank3B signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

In Intel Agilex 7 SoC and FPGA SOM, upon these 18 LVDS or 36 Single Ended IOs from Intel Agilex 7 FPGA Bank3B, two General Purpose Clock input LVDS pair and two General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended

clock. In Intel Agilex 7 SoC and FPGA SOM, Bank3B I/O voltage is set to **1.2V** as the remaining bank IOs are used for FPGA2 DDR4 support.

For more details on Intel Agilex 7 SoC and FPGA Bank3B pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D45	FPGA_D61_LVDS3B_1N_RX_IO95	IO95, DIFF_RX_3B1N/ D61	IO, 1.2V LVDS	Bank3B 1n Rx differential Negative. Same pin can be configured as Single ended I/O.
D44	FPGA_E60_LVDS3B_1P_RX_IO94	IO94, DIFF_RX_3B1P/ E60	IO, 1.2V LVDS	Bank3B 1p Rx differential Positive. Same pin can be configured as Single ended I/O.
D47	FPGA_B61_LVDS3B_1N_TX_IO93	IO93, DIFF_TX_3B1N/ B61	IO, 1.2V LVDS	Bank3B 1n Tx differential Negative. Same pin can be configured as Single ended I/O.
D46	FPGA_A60_LVDS3B_1P_TX_IO92	IO92, DIFF_TX_3B1P/ A60	IO, 1.2V LVDS	Bank3B 1p Tx differential Positive. Same pin can be configured as Single ended I/O.
D49	FPGA_D59_LVDS3B_2N_RX_IO91	IO91, DIFF_RX_3B2N/ D59	IO, 1.2V LVDS	Bank3B 2n Rx differential Negative. Same pin can be configured as Single ended I/O.
D48	FPGA_E58_LVDS3B_2P_RX_IO90	IO90, DIFF_RX_3B2P/ E58	IO, 1.2V LVDS	Bank3B 2p Rx differential Positive. Same pin can be configured as Single ended I/O.
C45	FPGA_B59_LVDS3B_2N_TX_IO89	IO89, DIFF_TX_3B2N/ B59	IO, 1.2V LVDS	Bank3B 2n Tx differential Negative. Same pin can be configured as Single ended I/O.
C44	FPGA_A58_LVDS3B_2P_TX_IO88	IO88, DIFF_TX_3B2P/ A58	IO, 1.2V LVDS	Bank3B 2p Tx differential Positive. Same pin can be configured as Single ended I/O.
C47	FPGA_D57_LVDS3B_3N_RX_IO87	IO87, CDR, DIFF_RX_3B3N/ D57	IO, 1.2V LVDS	Bank3B 3n Rx differential Negative. Same pin can be configured as Single ended I/O.
C46	FPGA_E56_LVDS3B_3P_RX_IO86	IO86, CDR, DIFF_RX_3B3P/ E56	IO, 1.2V LVDS	Bank3B 3p Rx differential Positive. Same pin can be configured as Single ended I/O.
C49	FPGA_B57_LVDS3B_3N_TX_IO85	IO85, DIFF_TX_3B3N/ B57	IO, 1.2V LVDS	Bank3B 3n Tx differential Negative. Same pin can be configured as Single ended I/O.
C48	FPGA_A56_LVDS3B_3P_TX_IO84	IO84, DIFF_TX_3B3P/ A56	IO, 1.2V LVDS	Bank3B 3p Tx differential Positive. Same pin can be configured as Single ended I/O.
B45	FPGA_K57_LVDS3B_4N_RX_IO83	IO83, DIFF_RX_3B4N/ K57	IO, 1.2V LVDS	Bank3B 4n Rx differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B44	FPGA_J56_LVDS3B_4P_RX_IO82	IO82, DIFF_RX_3B4P/ J56	IO, 1.2V LVDS	Bank3B 4p Rx differential Positive. Same pin can be configured as Single ended I/O.
B47	FPGA_F57_LVDS3B_4N_TX_IO81	IO81, DIFF_TX_3B4N/ F57	IO, 1.2V LVDS	Bank3B 4n Tx differential Negative. Same pin can be configured as Single ended I/O.
B46	FPGA_G56_LVDS3B_4P_TX_IO80	IO80, DIFF_TX_3B4P/ G56	IO, 1.2V LVDS	Bank3B 4p Tx differential Positive. Same pin can be configured as Single ended I/O.
B49	FPGA_K55_LVDS3B_5N_RX_IO79	IO79, DIFF_RX_3B5N/ K55	IO, 1.2V LVDS	Bank3B 5n Rx differential Negative. Same pin can be configured as Single ended I/O.
B48	FPGA_J54_LVDS3B_5P_RX_IO78	IO78, DIFF_RX_3B5P/ J54	IO, 1.2V LVDS	Bank3B 5p Rx differential Positive. Same pin can be configured as Single ended I/O.
A45	FPGA_F55_LVDS3B_5N_TX_IO77/CLKOUT_1N	IO77, PLL_3B_T_CLKOUT1N, DIFF_TX_3B5N/ F55	IO, 1.2V LVDS	Bank3B 5n Tx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
A44	FPGA_G54_LVDS3B_5P_TX_IO76/CLKOUT_1P	IO76, PLL_3B_T_CLKOUT1P, PLL_3B_T_CLKOUT1, PLL_3B_T_FB1, DIFF_TX_3B5P/ G54	IO, 1.2V LVDS	Bank3B 5p Tx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
A47	FPGA_K53_LVDS3B_6N_RX_IO75	IO75, CDR, DIFF_RX_3B6N/ K53	IO, 1.2V LVDS	Bank3B 6n Rx differential Negative. Same pin can be configured as Single ended I/O.
A46	FPGA_J52_LVDS3B_6P_RX_IO74	IO74, RZQ_T_3B, CDR, DIFF_RX_3B6P/ J52	IO, 1.2V LVDS	Bank3B 6p Rx differential Positive. Same pin can be configured as Single ended I/O.
A49	FPGA_F53_LVDS3B_6N_TX_IO73/CLKIN_1N	IO73, CLK_T_3B_1N, DIFF_TX_3B6N/ F53	IO, 1.2V LVDS	Bank3B 6n Tx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
A48	FPGA_G52_LVDS3B_6P_TX_IO72/CLKIN_1P	IO72, CLK_T_3B_1P, DIFF_TX_3B6P/ G52	IO, 1.2V LVDS	Bank3B 6p Tx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D52	FPGA_D55_LVDS3B_7N_RX_IO71/CLKIN_0N	IO71, CLK_T_3B_0N, DIFF_RX_3B7N/ D55	IO, 1.2V LVDS	Bank3B 7n Rx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
D51	FPGA_E54_LVDS3B_7P_RX_IO70/CLKIN_0P	IO70, CLK_T_3B_0P, DIFF_RX_3B7P/ E54	IO, 1.2V LVDS	Bank3B 7p Rx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D54	FPGA_B55_LVDS3B_7N_TX_IO69	IO69, DIFF_TX_3B7N/ B55	IO, 1.2V LVDS	Bank3B 7n Tx differential Negative. Same pin can be configured as Single ended I/O.
D53	FPGA_A54_LVDS3B_7P_TX_IO68	IO68, DIFF_TX_3B7P/ A54	IO, 1.2V LVDS	Bank3B 7p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D56	FPGA_D53_LVDS3B_8N_RX_IO67/CLKOUT_0N	IO67, PLL_3B_T_CLKOUT0N, DIFF_RX_3B8N/ D53	IO, 1.2V LVDS	Bank3B 8n Rx differential Negative. Same pin can be configured as Clock Output or Single ended I/O.
D55	FPGA_E52_LVDS3B_8P_RX_IO66/CLKOUT_0P	IO66, PLL_3B_T_CLKOUT0P, PLL_3B_T_CLKOUT0, PLL_3B_T_FB0, DIFF_RX_3B8P/ E52	IO, 1.2V LVDS	Bank3B 8p Rx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
C52	FPGA_B53_LVDS3B_8N_TX_IO65	IO65, DIFF_TX_3B8N/ B53	IO, 1.2V LVDS	Bank3B 8n Tx differential Negative. Same pin can be configured as Single ended I/O.
C51	FPGA_A52_LVDS3B_8P_TX_IO64	IO64, DIFF_TX_3B8P/ A52	IO, 1.2V LVDS	Bank3B 8p Tx differential Positive. Same pin can be configured as Single ended I/O.
C54	FPGA_D51_LVDS3B_9N_RX_IO63	IO63, CDR, DIFF_RX_3B9N/ D51	IO, 1.2V LVDS	Bank3B 9n Rx differential Negative. Same pin can be configured as Single ended I/O.
C53	FPGA_E50_LVDS3B_9P_RX_IO62	IO62, CDR, DIFF_RX_3B9P/ E50	IO, 1.2V LVDS	Bank3B 9p Rx differential Positive. Same pin can be configured as Single ended I/O.
C56	FPGA_B51_LVDS3B_9N_TX_IO61	IO61, DIFF_TX_3B9N/ B51	IO, 1.2V LVDS	Bank3B 9n Tx differential Negative. Same pin can be configured as Single ended I/O.
C55	FPGA_A50_LVDS3B_9P_TX_IO60	IO60, DIFF_TX_3B9P/ A50	IO, 1.2V LVDS	Bank3B 9p Tx differential Positive. Same pin can be configured as Single ended I/O.

2.6.6 FPGA IOs & General-Purpose Clocks – Bank3C

The Intel Agilex 7 SoC and FPGA SOM supports up to 18 LVDS IOs/36 Single Ended IOs and from Intel Agilex 7 FPGA Bank3C on Board-to-Board connector1. In Intel Agilex 7 SoC and FPGA SOM, Bank3C signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank3C signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

In Intel Agilex 7 SoC and FPGA SOM, upon these 18 LVDS IOs/36 Single Ended IOs from Intel Agilex 7 FPGA Bank3C, two General Purpose Clock input LVDS pair and two General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Intel Agilex 7 SoC and FPGA SOM, Bank3C I/O voltage is set to **1.2V** as the remaining bank IOs are used for HPS DDR4 support.

For more details on Intel Agilex 7 SoC and FPGA Bank3C pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D84	FPGA_D49_LVDS3C_9N_RX_IO63	IO63, CDR, DIFF_RX_3C9N/ D49	IO, 1.2V LVDS	Bank3C 9n Rx differential Negative. Same pin can be configured as Single ended I/O.
D83	FPGA_E48_LVDS3C_9P_RX_IO62	IO62, CDR, DIFF_RX_3C9P/ E48	IO, 1.2V LVDS	Bank3C 9p Rx differential Positive. Same pin can be configured as Single ended I/O.
C84	FPGA_B49_LVDS3C_9N_TX_IO61	IO61, DIFF_TX_3C9N/ B49	IO, 1.2V LVDS	Bank3C 9n Tx differential Negative. Same pin can be configured as Single ended I/O.
C83	FPGA_A48_LVDS3C_9P_TX_IO60	IO60, DIFF_TX_3C9P/ A48	IO, 1.2V LVDS	Bank3C 9p Tx differential Positive. Same pin can be configured as Single ended I/O.
B96	FPGA_B45_LVDS3C_7N_TX_IO69	IO69, DIFF_TX_3C7N/ B45	IO, 1.2V LVDS	Bank3C 7n Tx differential Negative. Same pin can be configured as Single ended I/O.
B95	FPGA_A44_LVDS3C_7P_TX_IO68	IO68, DIFF_TX_3C7P/ A44	IO, 1.2V LVDS	Bank3C 7p Tx differential Positive. Same pin can be configured as Single ended I/O.
D80	FPGA_D41_LVDS3C_5N_RX_IO79	IO79, DIFF_RX_3C5N/ D41	IO, 1.2V LVDS	Bank3C 5n Rx differential Negative. Same pin can be configured as Single ended I/O.
D79	FPGA_E40_LVDS3C_5P_RX_IO78	IO78, DIFF_RX_3C5P/ E40	IO, 1.2V LVDS	Bank3C 5p Rx differential Positive. Same pin can be configured as Single ended I/O.
C80	FPGA_B41_LVDS3C_5N_TX_IO77/CLKOUT_1N	IO77, PLL_3C_T_CLKOUT1N, DIFF_TX_3C5N/ B41	IO, 1.2V LVDS	Bank3C 5n Tx differential Negative. Same pin can be configured as Clock output or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C79	FPGA_A40_LVDS3C_5P_TX_IO76/CLKOUT_1P	IO76, PLL_3C_T_CLKOUT1P, PLL_3C_T_CLKOUT1, PLL_3C_T_FB1, DIFF_TX_3C5P/ A40	IO, 1.2V LVDS	Bank3C 5p Tx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
B80	FPGA_D47_LVDS3C_8N_RX_IO67/CLKOUT_0N	IO67, PLL_3C_T_CLKOUT0N, DIFF_RX_3C8N/ D47	IO, 1.2V LVDS	Bank3C 8n Rx differential Negative. Same pin can be configured as Clock output or Single ended I/O.
B79	FPGA_E46_LVDS3C_8P_RX_IO66/CLKOUT_0P	IO66, PLL_3C_T_CLKOUT0P, PLL_3C_T_CLKOUT0, PLL_3C_T_FB0, DIFF_RX_3C8P/ E46	IO, 1.2V LVDS	Bank3C 8p Rx differential Positive. Same pin can be configured as Clock Output or Single ended I/O.
A80	FPGA_B47_LVDS3C_8N_TX_IO65	IO65, DIFF_TX_3C8N/ B47	IO, 1.2V LVDS	Bank3C 8n Tx differential Negative. Same pin can be configured as Single ended I/O.
A79	FPGA_A46_LVDS3C_8P_TX_IO64	IO64, DIFF_TX_3C8P/ A46	IO, 1.2V LVDS	Bank3C 8p Tx differential Positive. Same pin can be configured as Single ended I/O.
A96	FPGA_B43_LVDS3C_6N_TX_IO73/CLKIN_1N	IO73, CLK_T_3C_1N, DIFF_TX_3C6N/ B43	IO, 1.2V LVDS	Bank3C 6n Tx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
A95	FPGA_A42_LVDS3C_6P_TX_IO72/CLKIN_1P	IO72, CLK_T_3C_1P, DIFF_TX_3C6P/ A42	IO, 1.2V LVDS	Bank3C 6p Tx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D68	FPGA_K39_LVDS3C_3N_RX_IO87	IO87, CDR, DIFF_RX_3C3N/ K39	IO, 1.2V LVDS	Bank3C 3n Rx differential Negative. Same pin can be configured as Single ended I/O.
D67	FPGA_J38_LVDS3C_3P_RX_IO86	IO86, CDR, DIFF_RX_3C3P/ J38	IO, 1.2V LVDS	Bank3C 3p Rx differential Positive. Same pin can be configured as Single ended I/O.
C68	FPGA_F39_LVDS3C_3N_TX_IO85	IO85, DIFF_TX_3C3N/ F39	IO, 1.2V LVDS	Bank3C 3n Tx differential Negative. Same pin can be configured as Single ended I/O.
C67	FPGA_G38_LVDS3C_3P_TX_IO84	IO84, DIFF_TX_3C3P/ G38	IO, 1.2V LVDS	Bank3C 3p Tx differential Positive. Same pin can be configured as Single ended I/O.
B68	FPGA_D39_LVDS3C_4N_RX_IO83	IO83, DIFF_RX_3C4N/ D39	IO, 1.2V LVDS	Bank3C 4n Rx differential Negative. Same pin can be configured as Single ended I/O.
B67	FPGA_E38_LVDS3C_4P_RX_IO82	IO82, DIFF_RX_3C4P/ E38	IO, 1.2V LVDS	Bank3C 4p Rx differential Positive. Same pin can be configured as Single ended I/O.
A68	FPGA_B39_LVDS3C_4N_TX_IO81	IO81, DIFF_TX_3C4N/ B39	IO, 1.2V LVDS	Bank3C 4n Tx differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A67	FPGA_A38_LVDS3C_4P_TX_IO80	IO80, DIFF_TX_3C4P/ A38	IO, 1.2V LVDS	Bank3C 4p Tx differential Positive. Same pin can be configured as Single ended I/O.
B60	FPGA_D45_LVDS3C_7N_RX_IO71/CLKIN_0N	IO71, CLK_T_3C_0N, DIFF_RX_3C7N/ D45	IO, 1.2V LVDS	Bank3C 7n Rx differential Negative. Same pin can be configured as Clock Input or Single ended I/O.
B59	FPGA_E44_LVDS3C_7P_RX_IO70/CLKIN_0P	IO70, CLK_T_3C_0P, DIFF_RX_3C7P/ E44	IO, 1.2V LVDS	Bank3C 7p Rx differential Positive. Same pin can be configured as Clock Input or Single ended I/O.
D64	FPGA_K35_LVDS3C_1N_RX_IO95	IO95, DIFF_RX_3C1N/ K35	IO, 1.2V LVDS	Bank3C 1n Rx differential Negative. Same pin can be configured as Single ended I/O.
D63	FPGA_J34_LVDS3C_1P_RX_IO94	IO94, DIFF_RX_3C1P/ J34	IO, 1.2V LVDS	Bank3C 1p Rx differential Positive. Same pin can be configured as Single ended I/O.
C64	FPGA_F35_LVDS3C_1N_TX_IO93	IO93, DIFF_TX_3C1N/ F35	IO, 1.2V LVDS	Bank3C 1n Tx differential Negative. Same pin can be configured as Single ended I/O.
C63	FPGA_G34_LVDS3C_1P_TX_IO92	IO92, DIFF_TX_3C1P/ G34	IO, 1.2V LVDS	Bank3C 1p Tx differential Positive. Same pin can be configured as Single ended I/O.
B64	FPGA_K37_LVDS3C_2N_RX_IO91	IO91, DIFF_RX_3C2N/ K37	IO, 1.2V LVDS	Bank3C 2n Rx differential Negative. Same pin can be configured as Single ended I/O.
B63	FPGA_J36_LVDS3C_2P_RX_IO90	IO90, DIFF_RX_3C2P/ J36	IO, 1.2V LVDS	Bank3C 2p Rx differential Positive. Same pin can be configured as Single ended I/O.
A64	FPGA_F37_LVDS3C_2N_TX_IO89	IO89, DIFF_TX_3C2N/ F37	IO, 1.2V LVDS	Bank3C 2n Tx differential Negative. Same pin can be configured as Single ended I/O.
A63	FPGA_G36_LVDS3C_2P_TX_IO88	IO88, DIFF_TX_3C2P/ G36	IO, 1.2V LVDS	Bank3C 2p Tx differential Positive. Same pin can be configured as Single ended I/O.
A60	FPGA_D43_LVDS3C_6N_RX_IO75	IO75, CDR, DIFF_RX_3C6N/ D43	IO, 1.2V LVDS	Bank3C 6n Rx differential Negative. Same pin can be configured as Single ended I/O.
A59	FPGA_E42_LVDS3C_6P_RX_IO74	IO74, RZQ_T_3C, CDR, DIFF_RX_3C6P/ E42	IO, 1.2V LVDS	Bank3C 6p Rx differential Positive. Same pin can be configured as Single ended I/O.

2.6.7 Power Control Input

The Intel Agilex 7 SoC and FPGA SOM works with 12V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. In Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance.

For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	Pin Name	Signal Type/ Termination	Description
C73, C74, B58, B57, C77, C78, B65, B77, C81, C82, B78, B81, C85, C86, B82, A8, C89, C90, C22, B50, B85, C94, B43, B36, C97, C98, D89, B29, B22, B15, C70, B8, D93, C61, A97, D8, C50, A94, A93, A90, A89, C65, D15, A85, A82, A81, A78, A77, B73, D22, C58, A74, A73, C57, B61, A70, D29, A69, C43, C29, A66, A65, C69, D36, C62, A62, A61, B66, C66, A58, D43, A57, B86, A15, B89, B90, B94, D50, C15, A36, B97, B98, D97, D90, D57, D58, C36, B69, D61, D62, A86, A43, D65, D66, B74, A98, D69, D70, B62, A29, D73, D74, B70, C93, D77, D78, C8, A50, D81, D82, A22, B93, D85, D86, D98, D94	GND	NA	Power	Ground.

2.7 Board to Board Connector2

The Intel Agilex 7 SoC and FPGA SOM Board to Board Connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2(J6) is physically located on bottom side of the SOM as shown below.

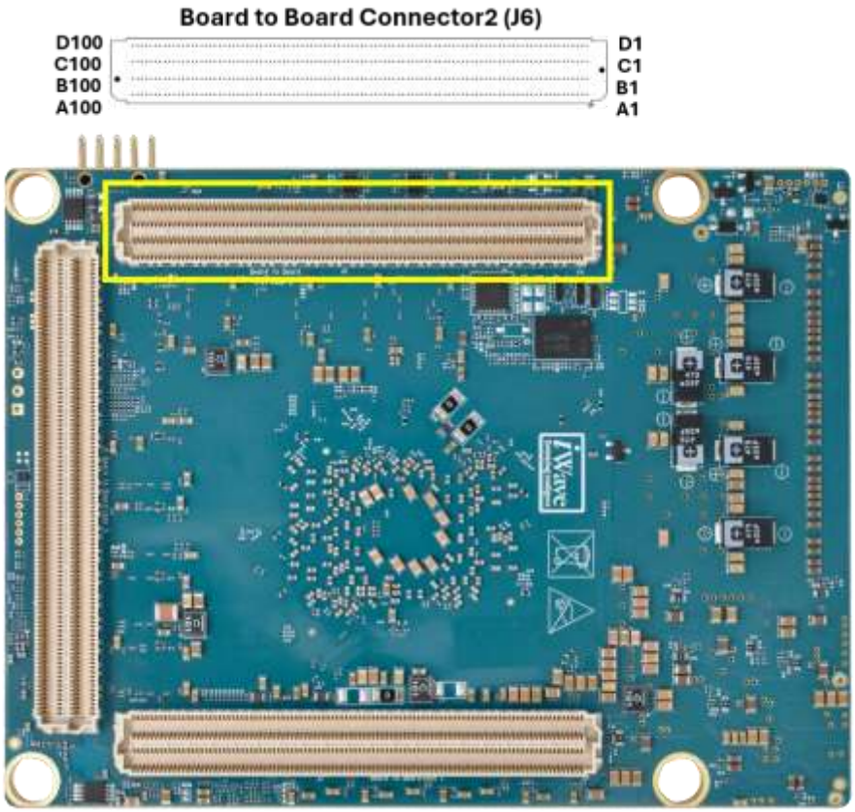

Figure 8: Board-to-Board Connector2

Number of Pins - 400

Connector Part Number - ASP-209946-01 from Samtech

Mating Connector - ASP-214802-01 from Samtech

Staking Height - 5mm

Table 11: Board to Board Connector2 Pinout

B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name
Row-A		Row-B		Row-C		Row-D	
A1	VCC_12V	B1	VCC_12V	C1	VCC_12V	D1	VCC_12V
A2	VCC_12V	B2	VCC_12V	C2	VCC_12V	D2	VCC_12V
A3	VCC_12V	B3	VCC_12V	C3	VCC_12V	D3	VCC_12V
A4	VCC_12V	B4	VCC_12V	C4	VCC_12V	D4	VCC_12V
A5	VCC_12V	B5	VCC_12V	C5	VCC_12V	D5	VCC_12V
A6	VCC_12V	B6	VCC_12V	C6	VCC_12V	D6	VCC_12V
A7	VCC_12V	B7	VCC_12V	C7	VCC_12V	D7	VCC_12V
A8	VCC_12V	B8	VCC_12V	C8	VCC_12V	D8	VCC_12V
A9	GND	B9	GND	C9	GND	D9	GND
A10	GND	B10	GND	C10	GND	D10	GND
A11	NC	B11	SOMPWR_EN	C11	NC	D11	10MHZ_B2B_OUT
A12	SDM_TCK_B2B	B12	SOM_PWR_OK	C12	VRTC_3V0	D12	1PPS_B2B_OUT
A13	SDM_TMS_B2B	B13	HPS_RESET_OUT(GPIO1_22)	C13	SDM_AS_nCSO0/MSEL0*	D13	PCIE_PERST_N_12A_GXF
A14	SDM_TDO_B2B	B14	SDM_HPS_NRESET_1V8	C14	SDM_MSEL1	D14	PCIE_PERST_N_13C_GXF
A15	SDM_TDI_B2B	B15	SDM_AS_CONFIG_DONE	C15	SDM_MSEL2	D15	nCATTRIP_1V8/ FACTORY_IMAGE
A16	GND	B16	GND	C16	GND	D16	GND
A17	SD_CLK	B17	H2F_SPI_SCK/QSPI_CLK	C17	NC	D17	NC
A18	SD_CMD	B18	H2F_SPI_MOSI/QSPI_IO0	C18	NC	D18	NC
A19	SD_DATA0	B19	H2F_SPI_MISO/QSPI_IO1	C19	NC	D19	NC
A20	SD_DATA1	B20	QSPI_IO2	C20	NC	D20	NC
A21	SD_DATA2	B21	H2F_SPI_CS1/QSPI_IO3	C21	NC	D21	NC
A22	SD_DATA3	B22	H2F_SPI_CS0/QSPI_CS	C22	NC	D22	NC
A23	GND	B23	GND	C23	GND	D23	GND
A24	SD_CD(GPIO1_18)	B24	SD_WP(GPIO1_19)	C24	NC	D24	NC
A25	SD_PWR_EN(GPIO1_20)	B25	10MHZ_B2B_IN	C25	NC	D25	NC
A26	HPS_I2C0_SCL_1V8	B26	1PPS_B2B_IN_3V3	C26	PCIE_PERST_N_12C_GXF	D26	NC
A27	HPS_I2C0_SDA_1V8	B27	HPS_UART0_TX	C27	PCIE_PERST_N_13A_GXF	D27	NC
A28	H2F_I2C1_SCL_1V8	B28	HPS_UART0_RX	C28	GND	D28	GND
A29	H2F_I2C1_SDA_1V8	B29	HPS_UART0_CTS	C29	NC	D29	NC
A30	HPS_UART1_TX	B30	HPS_UART0_RTS	C30	NC	D30	NC
A31	HPS_UART1_RX	B31	HPS_VBUS_USB	C31	GND	D31	GND
A32	B_GPHY_ACTIVITY_LED1	B32	HPS_USB_PWR_EN	C32	NC	D32	NC
A33	B_GPHY_LINK_LED2	B33	HPS_USB_OTG_ID	C33	NC	D33	NC
A34	GND	B34	GND	C34	GND	D34	GND
A35	GPHY_DTXRXM	B35	HPS_USB_OTG_DM	C35	NC	D35	NC
A36	GPHY_DTXRXP	B36	HPS_USB_OTG_DP	C36	NC	D36	NC
A37	GND	B37	GND	C37	GND	D37	GND
A38	GPHY_CTXRXM	B38	TEMP_CORE_AP	C38	NC	D38	NC
A39	GPHY_CTXRXP	B39	TEMP_CORE_AN	C39	NC	D39	NC

B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name
A40	GND	**B40**	GND	**C40**	GND	**D40**	GND
A41	GPHY_BTXRXM	**B41**	B2B_SYNC_CLK_OUTP	**C41**	NC	**D41**	NC
A42	GPHY_BTXRXP	**B42**	B2B_SYNC_CLK_OUTN	**C42**	NC	**D42**	NC
A43	GND	**B43**	GND	**C43**	GND	**D43**	GND
A44	GPHY_ATXRXM	**B44**	B2B_SYNC_CLK_INP	**C44**	NC	**D44**	NC
A45	GPHY_ATXRXP	**B45**	B2B_SYNC_CLK_INN	**C45**	NC	**D45**	NC
A46	GND	**B46**	GND	**C46**	GND	**D46**	GND
A47	FGTL12A_TX_Q0_CH0P	**B47**	FGTL12A_RX_Q0_CH0P	**C47**	FGTL12A_TX_Q1_CH0P	**D47**	FGTL12A_RX_Q1_CH0P
A48	FGTL12A_TX_Q0_CH0N	**B48**	FGTL12A_RX_Q0_CH0N	**C48**	FGTL12A_TX_Q1_CH0N	**D48**	FGTL12A_RX_Q1_CH0N
A49	GND	**B49**	GND	**C49**	GND	**D49**	GND
A50	FGTL12A_TX_Q0_CH1P	**B50**	FGTL12A_RX_Q0_CH1P	**C50**	FGTL12A_TX_Q1_CH1P	**D50**	FGTL12A_RX_Q1_CH1P
A51	FGTL12A_TX_Q0_CH1N	**B51**	FGTL12A_RX_Q0_CH1N	**C51**	FGTL12A_TX_Q1_CH1N	**D51**	FGTL12A_RX_Q1_CH1N
A52	GND	**B52**	GND	**C52**	GND	**D52**	GND
A53	FGTL12A_TX_Q0_CH2P	**B53**	FGTL12A_RX_Q0_CH2P	**C53**	FGTL12A_TX_Q1_CH2P	**D53**	FGTL12A_RX_Q1_CH2P
A54	FGTL12A_TX_Q0_CH2N	**B54**	FGTL12A_RX_Q0_CH2N	**C54**	FGTL12A_TX_Q1_CH2N	**D54**	FGTL12A_RX_Q1_CH2N
A55	GND	**B55**	GND	**C55**	GND	**D55**	GND
A56	FGTL12A_TX_Q0_CH3P	**B56**	FGTL12A_RX_Q0_CH3P	**C56**	FGTL12A_TX_Q1_CH3P	**D56**	FGTL12A_RX_Q1_CH3P
A57	FGTL12A_TX_Q0_CH3N	**B57**	FGTL12A_RX_Q0_CH3N	**C57**	FGTL12A_TX_Q1_CH3N	**D57**	FGTL12A_RX_Q1_CH3N
A58	GND	**B58**	GND	**C58**	GND	**D58**	GND
A59	REFCLK_FGTL12A_Q0_RX_CH0P	**B59**	REFCLK_FGTL12A_Q0_RX_CH1P	**C59**	REFCLK_FGTL12A_Q1_RX_CH2P	**D59**	REFCLK_FGTL12A_Q1_RX_CH3P
A60	REFCLK_FGTL12A_Q0_RX_CH0N	**B60**	REFCLK_FGTL12A_Q0_RX_CH1N	**C60**	REFCLK_FGTL12A_Q1_RX_CH2N	**D60**	REFCLK_FGTL12A_Q1_RX_CH3N
A61	GND	**B61**	GND	**C61**	GND	**D61**	GND
A62	FGTL12C_TX_Q0_CH0P	**B62**	FGTL12C_RX_Q0_CH0P	**C62**	FGTL12C_TX_Q1_CH0P	**D62**	FGTL12C_RX_Q1_CH0P
A63	FGTL12C_TX_Q0_CH0N	**B63**	FGTL12C_RX_Q0_CH0N	**C63**	FGTL12C_TX_Q1_CH0N	**D63**	FGTL12C_RX_Q1_CH0N
A64	GND	**B64**	GND	**C64**	GND	**D64**	GND
A65	FGTL12C_TX_Q0_CH1P	**B65**	FGTL12C_RX_Q0_CH1P	**C65**	FGTL12C_TX_Q1_CH1P	**D65**	FGTL12C_RX_Q1_CH1P
A66	FGTL12C_TX_Q0_CH1N	**B66**	FGTL12C_RX_Q0_CH1N	**C66**	FGTL12C_TX_Q1_CH1N	**D66**	FGTL12C_RX_Q1_CH1N
A67	GND	**B67**	GND	**C67**	GND	**D67**	GND
A68	FGTL12C_TX_Q0_CH2P	**B68**	FGTL12C_RX_Q0_CH2P	**C68**	FGTL12C_TX_Q1_CH2P	**D68**	FGTL12C_RX_Q1_CH2P
A69	FGTL12C_TX_Q0_CH2N	**B69**	FGTL12C_RX_Q0_CH2N	**C69**	FGTL12C_TX_Q1_CH2N	**D69**	FGTL12C_RX_Q1_CH2N
A70	GND	**B70**	GND	**C70**	GND	**D70**	GND
A71	FGTL12C_TX_Q0_CH3P	**B71**	FGTL12C_RX_Q0_CH3P	**C71**	FGTL12C_TX_Q1_CH3P	**D71**	FGTL12C_RX_Q1_CH3P
A72	FGTL12C_TX_Q0_CH3N	**B72**	FGTL12C_RX_Q0_CH3N	**C72**	FGTL12C_TX_Q1_CH3N	**D72**	FGTL12C_RX_Q1_CH3N
A73	GND	**B73**	GND	**C73**	GND	**D73**	GND
A74	REFCLK_FGTL12C_Q1_RX_CH2p	**B74**	REFCLK_FGTL12C_Q0_RX_CH1P	**C74**	REFCLK_FGTL12C_Q0_RX_CH0p	**D74**	REFCLK_FGTL12C_Q1_RX_CH3P
A75	REFCLK_FGTL12C_Q1_RX_CH2n	**B75**	REFCLK_FGTL12C_Q0_RX_CH1N	**C75**	REFCLK_FGTL12C_Q0_RX_CH0n	**D75**	REFCLK_FGTL12C_Q1_RX_CH3N
A76	GND	**B76**	GND	**C76**	GND	**D76**	GND
A77	FGTL12C_TX_Q2_CH0P	**B77**	FGTL12C_RX_Q2_CH0P	**C77**	FGTL12C_TX_Q3_CH0P	**D77**	FGTL12C_RX_Q3_CH0P
A78	FGTL12C_TX_Q2_CH0N	**B78**	FGTL12C_RX_Q2_CH0N	**C78**	FGTL12C_TX_Q3_CH0N	**D78**	FGTL12C_RX_Q3_CH0N
A79	GND	**B79**	GND	**C79**	GND	**D79**	GND
A80	FGTL12C_TX_Q2_CH1P	**B80**	FGTL12C_RX_Q2_CH1P	**C80**	FGTL12C_TX_Q3_CH1P	**D80**	FGTL12C_RX_Q3_CH1P

B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name	B2B2 Pin No	Signal Name
A81	FGTL12C_TX_Q2_CH1N	**B81**	FGTL12C_RX_Q2_CH1N	**C81**	FGTL12C_TX_Q3_CH1N	**D81**	FGTL12C_RX_Q3_CH1N
A82	GND	**B82**	GND	**C82**	GND	**D82**	GND
A83	FGTL12C_TX_Q2_CH2P	**B83**	FGTL12C_RX_Q2_CH2P	**C83**	FGTL12C_TX_Q3_CH2P	**D83**	FGTL12C_RX_Q3_CH2P
A84	FGTL12C_TX_Q2_CH2N	**B84**	FGTL12C_RX_Q2_CH2N	**C84**	FGTL12C_TX_Q3_CH2N	**D84**	FGTL12C_RX_Q3_CH2N
A85	GND	**B85**	GND	**C85**	GND	**D85**	GND
A86	FGTL12C_TX_Q2_CH3P	**B86**	FGTL12C_RX_Q2_CH3P	**C86**	FGTL12C_TX_Q3_CH3P	**D86**	FGTL12C_RX_Q3_CH3P
A87	FGTL12C_TX_Q2_CH3N	**B87**	FGTL12C_RX_Q2_CH3N	**C87**	FGTL12C_TX_Q3_CH3N	**D87**	FGTL12C_RX_Q3_CH3N
A88	GND	**B88**	GND	**C88**	GND	**D88**	GND
A89	REFCLK_FGTL12C_Q2_RX_CH5P	**B89**	REFCLK_FGTL12C_Q2_CH8P	**C89**	REFCLK_FGTL12C_Q3_RX_CH6P	**D89**	REFCLK_FGTL12C_Q3_RX_CH7P
A90	REFCLK_FGTL12C_Q2_RX_CH5N	**B90**	REFCLK_FGTL12C_Q2_CH8N	**C90**	REFCLK_FGTL12C_Q3_RX_CH6N	**D90**	REFCLK_FGTL12C_Q3_RX_CH7N
A91	GND	**B91**	GND	**C91**	GND	**D91**	GND
A92	FGTL12A_TX_Q2_CH0P	**B92**	FGTL12A_RX_Q2_CH0p	**C92**	FGTL12A_TX_Q2_CH2p	**D92**	FGTL12A_RX_Q2_CH2P
A93	FGTL12A_TX_Q2_CH0N	**B93**	FGTL12A_RX_Q2_CH0n	**C93**	FGTL12A_TX_Q2_CH2n	**D93**	FGTL12A_RX_Q2_CH2N
A94	GND	**B94**	GND	**C94**	GND	**D94**	GND
A95	FGTL12A_TX_Q2_CH1P	**B95**	FGTL12A_RX_Q2_CH1p	**C95**	FGTL12A_TX_Q2_CH3p	**D95**	FGTL12A_RX_Q2_CH3P
A96	FGTL12A_TX_Q2_CH1N	**B96**	FGTL12A_RX_Q2_CH1n	**C96**	FGTL12A_TX_Q2_CH3n	**D96**	FGTL12A_RX_Q2_CH3N
A97	GND	**B97**	GND	**C97**	GND	**D97**	GND
A98	REFCLK_FGTL12A_Q2_RX_CH5P	**B98**	REFCLK_FGTL12A_Q2_CH8P	**C98**	SDM_ADC_VSIGP_0	**D98**	SDM_ADC_VSIGP_1
A99	REFCLK_FGTL12A_Q2_RX_CH5N	**B99**	REFCLK_FGTL12A_Q2_CH8N	**C99**	SDM_ADC_VSIGN_0	**D99**	SDM_ADC_VSIGN_1
A100	GND	**B100**	GND	**C100**	GND	**D100**	GND

2.7.1 HPS & SDM Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Intel Agilex 7 SoC and FPGA device HPS & SDM banks are explained in the following section.

2.7.1.1 Gigabit Ethernet Interface

The Intel Agilex 7 SoC and FPGA SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2. The MAC is integrated in the Intel Agilex 7 SoC and FPGA HPS and connected to the external Gigabit Ethernet PHY "RTL8211FI-VD-CG" on SOM. This Gigabit Ethernet PHY is interfaced with EMAC1 interface of Intel Agilex 7 HPS and works at 1.8V IO voltage level.

In Intel Agilex 7 SoC and FPGA SOM, HPS GPIO "HPS_GPIO0_IO10" is used for Ethernet PHY reset. Also, SOM supports Ethernet PHY interrupt through HPS GPIO "HPS_GPIO0_IO12". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the Carrier board.

In Intel Agilex 7 SoC and FPGA SOM, EMAC1 Ethernet PHY Address is set to 100 using on SOM Strapping option.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A35	GPHY_DTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
A36	GPHY_DTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
A38	GPHY_CTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
A39	GPHY_CTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
A41	GPHY_BTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
A42	GPHY_BTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
A44	GPHY_ATXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
A45	GPHY_ATXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
A33	B_GPHY_LINK_LED	NA	O, 1.8V CMOS	Gigabit Ethernet 1000Mbps Link status LED (Active High).
A32	B_GPHY_ACTIVITY_LED	NA	O, 1.8V CMOS	Gigabit Ethernet Activity LED (Active High).

2.7.1.2 USB2.0 OTG Interface

The Intel Agilex 7 SoC and FPGA SOM supports one USB2.0 OTG interface on Board-to-Board Connector2. USB1 OTG controller of Intel Agilex 7 SoC and FPGA device HPS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the HPS pins. The Intel Agilex 7 SoC and FPGA SOM supports “USB3320” ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Intel Agilex 7 SoC and FPGA SOM, HPS GPIO “HPS_GPIO0_IO10” can be optionally used for USB ULPI PHY reset. It supports active high power enable signal on Board-to-Board Connector2 from USB PHY for external VBUS power control.

Also, Intel Agilex 7 SoC and FPGA SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
B35	HPS_USB_OTG_DM	NA	IO, USB	USB OTG data negative.
B36	HPS_USB_OTG_DP	NA	IO, USB	USB OTG data positive.
B32	HPS_USB_PWR_EN	NA	O, 3.3V CMOS	USB active high power enable output to control external USB VBUS.
B33	HPS_USB_OTG_ID	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
B31	HPS_VBUS_USB	NA	I, 5V Power	USB VBUS for VBUS monitoring.

2.7.1.3 SD/SDIO Interface (Optional)

The Intel Agilex 7 SoC and FPGA SOM optionally supports SD/SDIO interface on Board-to-Board Connector2. The SDMMC controller of Intel Agilex 7 SoC and FPGA HPS can be used for SD/SDIO interface on the Board-to-Board Connector. By default, these lines are connected to the On SOM eMMC. This SD/SDIO/MMC controller supports versions 4.3 to 4.5. It supports up to 50MHz operating frequency. Also in SD mode, data transfers in 1-bit and 4-bit modes.

The Intel Agilex 7 SoC and FPGA SOM supports Card Detect, Write Protect & Power Enable/Voltage Select pins through HPS pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
B24	SD_WP(GPIO1_19)	HPS_IOB_20/ L16	O, 1.8V LVCMOS	SD Write Protect.
A24	SD_CD(GPIO1_18)	HPS_IOB_19/ T21	I, 1.8V LVCMOS	SD Card Detect.
A25	SD_PWR_EN(GPIO1_20)	HPS_IOB_21/ M21	O, 1.8V LVCMOS	SD Power Enable/Voltage select through HPS GPIO.
A22	SD_DATA3	HPS_IOB_18/ L20	IO, 1.8V LVCMOS	SD DATA3.
A21	SD_DATA2	HPS_IOB_17/ U22	IO, 1.8V LVCMOS	SD DATA2.
A20	SD_DATA1	HPS_IOB_16/ N18	IO, 1.8V LVCMOS	SD DATA1.
A19	SD_DATA0	HPS_IOB_13/ Y27	IO, 1.8V LVCMOS	SD DATA0.
A18	SD_CMD	HPS_IOB_14/ P19	IO, 1.8V LVCMOS	SD Command.
A17	SD_CLK	HPS_IOB_15/ W26	O, 1.8V LVCMOS	SD Clock.

2.7.1.4 QSPI Interface – From SDM Bank (Optional)

The Intel Agilex 7 SoC and FPGA SOM the SPI lines connected to the On-SOM QSPI Flash is optionally connected to Board-to-Board Connector2 from the SDM Bank. The SPI controller of Intel Agilex 7 SoC and FPGA SDM is used for QSPI interface through SDM pins. By default, the On-SOM QSPI Flash will be supported and, on these pins, QSPI lines will be connected that are routed from HPS to FPGA internally.

For more details on QSPI Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
B17	H2F_SPI_SCK/QSPI_CLK	SDM_IO2/ DL66	O, 1.8V LVCMOS	QSPI clock.
B18	H2F_SPI_MOSI/QSPI_IO 0	SDM_IO4/ DD65	IO, 1.8V LVCMOS	QSPI IO0.
B19	H2F_SPI_MISO/QSPI_IO 1	SDM_IO1/ DC58	IO, 1.8V LVCMOS	QSPI IO1.
B20	QSPI_IO2	SDM_IO3/ DK65	IO, 1.8V LVCMOS	QSPI IO2.
B21	H2F_SPI_CS1/QSPI_IO3	SDM_IO6/ DD57	IO, 1.8V LVCMOS	QSPI IO3.
B22	H2F_SPI_CS0/QSPI_CS	SDM_IO5 / DE62	O, 1.8V LVCMOS	QSPI Chip Select.

2.7.1.5 Debug UART Interface

The Intel Agilex 7 SoC and FPGA SOM supports one Debug UART interface on Board-to-Board Connector2. The UART1 controller of Intel Agilex 7 SoC and FPGA HPS is used for Debug UART interface through HPS pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A30	HPS_UART1_TX	HPS_IOB_7/ W28	O, 1.8V LVCMOS	UART1 Transmit data line for Debug.
A31	HPS_UART1_RX	HPS_IOB_8/ A22	I, 1.8V LVCMOS	UART1 Receive data line for Debug.

2.7.1.6 Data UART Interface

The Intel Agilex 7 SoC and FPGA SOM supports one DATA UART interface on Board-to-Board Connector2. The UART0 controller of Intel Agilex 7 SoC and FPGA device HPS is used for Data UART interface through HPS pins. This controller supports full-duplex asynchronous receiver and transmitter path with programmable baud rates.

For more details on Data UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
B27	HPS_UART0_TX	HPS_IOA_3/ Y23	O, 1.8V LVCMOS	UART0 Transmit data line
B28	HPS_UART0_RX	HPS_IOA_4/ M17	I, 1.8V LVCMOS	UART0 Receive data line
B29	HPS_UART0_CTS	HPS_IOA_1/ AA24	O, 1.8V LVCMOS	UART0 Clear to Send data line
B30	HPS_UART0_RTS	HPS_IOA_2/ M19	I, 1.8V LVCMOS	UART0 Request to Send data line

2.7.1.7 I2C Interface

The Intel Agilex 7 SoC and FPGA SOM supports one I2C interface from HPS on Board-to-Board Connector2. The I2C0 module of Intel Agilex 7 SoC and FPGA device's HPS is used for I2C interface through HPS pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C0 interface is also connected to On-SOM On SOM Regulators & Clock Generators in the Intel Agilex 7 SoC and FPGA SOM.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A27	HPS_I2C0_SDA_1V8	HPS_IOA_5/ AA28	IO, 1.8V OD/ 4.7K PU	I2C0 data.
A26	HPS_I2C0_SCL_1V8	HPS_IOA_6/ A20	O, 1.8V OD/ 4.7K PU	I2C0 clock.

2.7.1.8 JTAG Interface

The Intel Agilex 7 SoC and FPGA SOM supports JTAG interface on Board-to-Board Connector2. The Intel Agilex 7 SoC and FPGA device's HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Intel Agilex 7 SoC and FPGA device. These JTAG interface signals are also connected to on-board JTAG connector. The JTAG connection can be selected to either Board-to-Board Connector2 or On Board JTAG Header using the On-Board Switch.

For more details on JTAG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A15	SDM_TDI_B2B	TDI/DL68	I, 1.8V LVCMOS	JTAG Test Data Input.
A13	SDM_TMS_B2B	TMS/DK69	I, 1.8V LVCMOS	JTAG Test Mode Select.
A12	SDM_TCK_B2B	TCK/DF65	I, 1.8V LVCMOS	JTAG Test Clock.
A14	SDM_TDO_B2B	TDO/DK67	O, 1.8V LVCMOS	JTAG Test Data Output.

2.7.2 HPS to FPGA routed Interfaces

The Intel Agilex 7 SoC FPGA supports routing of interfaces from HPS to FPGA. The interfaces which are supported in Board-to-Board Connector2 from Intel Agilex 7 SoC and FPGA device that are routed from HPS to FPGA are explained in the following section.

2.7.2.1 SPI Interface

The Intel Agilex 7 SoC and FPGA SOM the SPI lines are routed internally from HPS to FPGA and connected to Board-to-Board Connector2 from the FPGA Bank. The SPI controller of Intel Agilex 7 SoC and FPGA SDM is used for SPI interface through FPGA pins. By default, the On-SOM QSPI Flash will be supported and, on these pins, QSPI lines will be connected that are routed from HPS to FPGA internally.

For more details on SPI Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B17	H2F_SPI_SCK/QSPI_CLK	IO19, PLL_2D_B_CLKOUT0N, DIFF_RX_2D20N / CL32	O, 1.8V LVCMOS	SPI clock.
B18	H2F_SPI_MOSI/QSPI_IO0	IO18, PLL_2D_B_CLKOUT0P, PLL_2D_B_CLKOUT0, PLL_2D_B_FB0, DIFF_RX_2D20P/ CM31	O, 1.8V LVCMOS	SPI MOSI.
B19	H2F_SPI_MISO/QSPI_IO1	IO17, DIFF_TX_2D20N / CR32	I, 1.8V LVCMOS	SPI MISO.
B21	H2F_SPI_CS1/QSPI_IO3	IO15, CDR, DIFF_RX_2D21N / CL34	O, 1.8V LVCMOS	SPI Chip Select1.
B22	H2F_SPI_CS0/QSPI_CS	IO16, DIFF_TX_2D20P /CP31	O, 1.8V LVCMOS	SPI Chip Select0.

2.7.2.2 I2C Interface

In the Intel Agilex 7 SoC and FPGA SOM the I2C lines are routed internally from HPS to FPGA and connected to Board-to-Board Connector2 from the FPGA Bank. The I2C controller of Intel Agilex 7 SoC and FPGA SDM is used for I2C interface through FPGA pins. This will help in supporting an additional I2C on the Board-to-Board Connector that can be used in standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A29	H2F_I2C1_SDA_1V8	IO21, DIFF_TX_2D19N/ CR30	IO, 1.8V OD/ 4.7K PU	I2C1 data.
A28	H2F_I2C1_SCL_1V8	IO20, DIFF_TX_2D19P/ CP29	O, 1.8V OD/ 4.7K PU	I2C1 clock.

2.7.3 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Intel Agilex 7 SoC and FPGA device's FPGA is explained in the following section.

2.7.3.1 High Speed Transceivers

The Intel Agilex 7 SoC and FPGA SOM supports 28 high speed transceiver channels (12 Channels from FGT 12A Bank Quad [2:0] and 16 Channels from FGT 12C Bank Quad [3:0], Each quad supports 4 Transceiver channels) on Board-to-Board connector2. In Intel Agilex 7 SoC and FPGA SOM, the Transceivers connected to Board-to-Board Connector2 is capable of running up to a maximum speed of 32Gbps in NRZ Format or 58Gbps in PAM4 Format. These transceivers can be used to interface to multiple high-speed interface protocols. Each 4 Channel Transceiver Bank supports two reference clock input pairs.

For more details on FGTL 12A transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT_12A Quad0 Channels				
B48	FGTL12A_RX_Q0_CH0N	FGTL12A_RX_Q0_CH0N /CY65	I, DIFF	Bank FGT12A-Q0 channel0 High speed differential receiver negative.
B47	FGTL12A_RX_Q0_CH0P	FGTL12A_RX_Q0_CH0P /DA66	I, DIFF	Bank FGT12A-Q0 channel0 High speed differential receiver positive.
B51	FGTL12A_RX_Q0_CH1N	FGTL12A_RX_Q0_CH1N /CW68	I, DIFF	Bank FGT12A-Q0 channel1 High speed differential receiver negative.
B50	FGTL12A_RX_Q0_CH1P	FGTL12A_RX_Q0_CH1P /CV69	I, DIFF	Bank FGT12A-Q0 channel1 High speed differential receiver positive.
B54	FGTL12A_RX_Q0_CH2N	FGTL12A_RX_Q0_CH2N /CT65	I, DIFF	Bank FGT12A-Q0 channel2 High speed differential receiver negative.
B53	FGTL12A_RX_Q0_CH2P	FGTL12A_RX_Q0_CH2P /CU66	I, DIFF	Bank FGT12A-Q0 channel2 High speed differential receiver positive.
B57	FGTL12A_RX_Q0_CH3N	FGTL12A_RX_Q0_CH3N /CR68	I, DIFF	Bank FGT12A-Q0 channel3 High speed differential receiver negative.
B56	FGTL12A_RX_Q0_CH3P	FGTL12A_RX_Q0_CH3P /CP69	I, DIFF	Bank FGT12A-Q0 channel3 High speed differential receiver positive.
A48	FGTL12A_TX_Q0_CH0N	FGTL12A_TX_Q0_CH0N /CY59	O, DIFF	Bank FGT12A-Q0 channel0 High speed differential transmitter negative.
A47	FGTL12A_TX_Q0_CH0P	FGTL12A_TX_Q0_CH0P /DA60	O, DIFF	Bank FGT12A-Q0 channel0 High speed differential transmitter positive.
A51	FGTL12A_TX_Q0_CH1N	FGTL12A_TX_Q0_CH1N /CW62	O, DIFF	Bank FGT12A-Q0 channel1 High speed differential transmitter negative.
A50	FGTL12A_TX_Q0_CH1P	FGTL12A_TX_Q0_CH1P /CV63	O, DIFF	Bank FGT12A-Q0 channel1 High speed differential transmitter positive.
A54	FGTL12A_TX_Q0_CH2N	FGTL12A_TX_Q0_CH2N /CT59	O, DIFF	Bank FGT12A-Q0 channel2 High speed differential transmitter negative.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A53	FGTL12A_TX_Q0_CH2P	FGTL12A_TX_Q0_CH2P /CU60	O, DIFF	Bank FGT12A-Q0 channel2 High speed differential transmitter positive.
A57	FGTL12A_TX_Q0_CH3N	FGTL12A_TX_Q0_CH3N /CR62	O, DIFF	Bank FGT12A-Q0 channel3 High speed differential transmitter negative.
A56	FGTL12A_TX_Q0_CH3P	FGTL12A_TX_Q0_CH3P /CP63	O, DIFF	Bank FGT12A-Q0 channel3 High speed differential transmitter positive.
A60	REFCLK_FGTL12A_Q0_ RX_CH0N	REFCLK_FGTL12A_Q0_RX _CH0N /CW56	I, DIFF	Bank FGT12A-Q0 High speed differential Clock0 negative. Regional reference clock, this clock can be used for 12A Bank Q0 Transceivers.
A59	REFCLK_FGTL12A_Q0_ RX_CH0P	REFCLK_FGTL12A_Q0_RX _CH0P /CV57	I, DIFF	Bank FGT12A-Q0 High speed differential Clock0 positive. Regional reference clock, this clock can be used for 12A Bank Q0 Transceivers.
B60	REFCLK_FGTL12A_Q0_ RX_CH1N	REFCLK_FGTL12A_Q0_RX _CH1N /CR56	I, DIFF	Bank FGT12A-Q0 High speed differential Clock1 negative. Regional reference clock, this clock can be used for 12A Bank Q0 Transceivers.
B59	REFCLK_FGTL12A_Q0_ RX_CH1P	REFCLK_FGTL12A_Q0_RX _CH1P /CU56	I, DIFF	Bank FGT12A-Q0 High speed differential Clock1 positive. Regional reference clock, this clock can be used for 12A Bank Q0 Transceivers.
BANK-FGT_12A Quad1 Channels				
D48	FGTL12A_RX_Q1_CH0N	FGTL12A_RX_Q1_CH0N /CM65	I, DIFF	Bank FGT12A-Q1 channel0 High speed differential receiver negative.
D47	FGTL12A_RX_Q1_CH0P	FGTL12A_RX_Q1_CH0P /CN66	I, DIFF	Bank FGT12A-Q1 channel0 High speed differential receiver positive.
D51	FGTL12A_RX_Q1_CH1N	FGTL12A_RX_Q1_CH1N /CL68	I, DIFF	Bank FGT12A-Q1 channel1 High speed differential receiver negative.
D50	FGTL12A_RX_Q1_CH1P	FGTL12A_RX_Q1_CH1P /CK69	I, DIFF	Bank FGT12A-Q1 channel1 High speed differential receiver positive.
D54	FGTL12A_RX_Q1_CH2N	FGTL12A_RX_Q1_CH2N /CH65	I, DIFF	Bank FGT12A-Q1 channel2 High speed differential receiver negative.
D53	FGTL12A_RX_Q1_CH2P	FGTL12A_RX_Q1_CH2P /CJ66	I, DIFF	Bank FGT12A-Q1 channel2 High speed differential receiver positive.
D57	FGTL12A_RX_Q1_CH3N	FGTL12A_RX_Q1_CH3N /CG68	I, DIFF	Bank FGT12A-Q1 channel3 High speed differential receiver negative.
D56	FGTL12A_RX_Q1_CH3P	FGTL12A_RX_Q1_CH3P /CF69	I, DIFF	Bank FGT12A-Q1 channel3 High speed differential receiver positive.
C48	FGTL12A_TX_Q1_CH0N	FGTL12A_TX_Q1_CH0N /CM59	O, DIFF	Bank FGT12A-Q1 channel0 High speed differential transmitter negative.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C47	FGTL12A_TX_Q1_CH0P	FGTL12A_TX_Q1_CH0P /CN60	O, DIFF	Bank FGT12A-Q1 channel0 High speed differential transmitter positive.
C51	FGTL12A_TX_Q1_CH1N	FGTL12A_TX_Q1_CH1N /CL62	O, DIFF	Bank FGT12A-Q1 channel1 High speed differential transmitter negative.
C50	FGTL12A_TX_Q1_CH1P	FGTL12A_TX_Q1_CH1P /CK63	O, DIFF	Bank FGT12A-Q1 channel1 High speed differential transmitter positive.
C54	FGTL12A_TX_Q1_CH2N	FGTL12A_TX_Q1_CH2N /CH59	O, DIFF	Bank FGT12A-Q1 channel2 High speed differential transmitter negative.
C53	FGTL12A_TX_Q1_CH2P	FGTL12A_TX_Q1_CH2P /CJ60	O, DIFF	Bank FGT12A-Q1 channel2 High speed differential transmitter positive.
C57	FGTL12A_TX_Q1_CH3N	FGTL12A_TX_Q1_CH3N /CG62	O, DIFF	Bank FGT12A-Q1 channel3 High speed differential transmitter negative.
C56	FGTL12A_TX_Q1_CH3P	FGTL12A_TX_Q1_CH3P /CF63	O, DIFF	Bank FGT12A-Q1 channel3 High speed differential transmitter positive.
C60	REFCLK_FGTL12A_Q1_ RX_CH2N	REFCLK_FGTL12A_Q1_RX _CH2N /CP57	I, DIFF	Bank FGT12A-Q1 High speed differential Clock0 negative. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2, Q3 Transceivers.
C59	REFCLK_FGTL12A_Q1_ RX_CH2P	REFCLK_FGTL12A_Q1_RX _CH2P /CN56	I, DIFF	Bank FGT12A-Q1 High speed differential Clock0 positive. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2, Q3 Transceivers.
D60	REFCLK_FGTL12A_Q1_ RX_CH3N	REFCLK_FGTL12A_Q1_RX _CH3N /CG56	I, DIFF	Bank FGT12A-Q1 High speed differential Clock1 negative. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2, Q3 Transceivers.
D59	REFCLK_FGTL12A_Q1_ RX_CH3P	REFCLK_FGTL12A_Q1_RX _CH3P /CE56	I, DIFF	Bank FGT12A-Q1 High speed differential Clock1 positive. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2, Q3 Transceivers.
BANK-FGT_12A Quad2 Channels				
B93	FGTL12A_RX_Q2_CH0N	FGTL12A_RX_Q2_CH0N /CD65	I, DIFF	Bank FGT12A-Q2 channel0 High speed differential receiver negative.
B92	FGTL12A_RX_Q2_CH0P	FGTL12A_RX_Q2_CH0P /CE66	I, DIFF	Bank FGT12A-Q2 channel0 High speed differential receiver positive.
B96	FGTL12A_RX_Q2_CH1N	FGTL12A_RX_Q2_CH1N /CC68	I, DIFF	Bank FGT12A-Q2 channel1 High speed differential receiver negative.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B95	FGTL12A_RX_Q2_CH1P	FGTL12A_RX_Q2_CH1P /CB69	I, DIFF	Bank FGT12A-Q2 channel1 High speed differential receiver positive.
D93	FGTL12A_RX_Q2_CH2N	FGTL12A_RX_Q2_CH2N /BY65	I, DIFF	Bank FGT12A-Q2 channel2 High speed differential receiver negative.
D92	FGTL12A_RX_Q2_CH2P	FGTL12A_RX_Q2_CH2P /CA66	I, DIFF	Bank FGT12A-Q2 channel2 High speed differential receiver positive.
D96	FGTL12A_RX_Q2_CH3N	FGTL12A_RX_Q2_CH3N /BW68	I, DIFF	Bank FGT12A-Q2 channel3 High speed differential receiver negative.
D95	FGTL12A_RX_Q2_CH3P	FGTL12A_RX_Q2_CH3P /BV69	I, DIFF	Bank FGT12A-Q2 channel3 High speed differential receiver positive.
A93	FGTL12A_TX_Q2_CH0N	FGTL12A_TX_Q2_CH0N /CD59	O, DIFF	Bank FGT12A-Q2 channel0 High speed differential transmitter negative.
A92	FGTL12A_TX_Q2_CH0P	FGTL12A_TX_Q2_CH0P /CE60	O, DIFF	Bank FGT12A-Q2 channel0 High speed differential transmitter positive.
A96	FGTL12A_TX_Q2_CH1N	FGTL12A_TX_Q2_CH1N /CC62	O, DIFF	Bank FGT12A-Q2 channel1 High speed differential transmitter negative.
A95	FGTL12A_TX_Q2_CH1P	FGTL12A_TX_Q2_CH1P /CB63	O, DIFF	Bank FGT12A-Q2 channel1 High speed differential transmitter positive.
C93	FGTL12A_TX_Q2_CH2N	FGTL12A_TX_Q2_CH2N /BY59	O, DIFF	Bank FGT12A-Q2 channel2 High speed differential transmitter negative.
C92	FGTL12A_TX_Q2_CH2P	FGTL12A_TX_Q2_CH2P /CA60	O, DIFF	Bank FGT12A-Q2 channel2 High speed differential transmitter positive.
C96	FGTL12A_TX_Q2_CH3N	FGTL12A_TX_Q2_CH3N /BW62	O, DIFF	Bank FGT12A-Q2 channel3 High speed differential transmitter negative.
C95	FGTL12A_TX_Q2_CH3P	FGTL12A_TX_Q2_CH3P /BV63	O, DIFF	Bank FGT12A-Q2 channel3 High speed differential transmitter positive.
B99	REFCLK_FGTL12A_Q2_ CH8N	REFCLK_FGTL12A_Q2_CH 8N /CD57	IO, DIFF	Bank FGT12A-Q2 High speed differential Clock0 negative. Bidirectional Local reference clock, this clock can be used for 12A Bank Q2
B98	REFCLK_FGTL12A_Q2_ CH8P	REFCLK_FGTL12A_Q2_CH 8P /CC56	IO, DIFF	Bank FGT12A-Q2 High speed differential Clock0 positive. Bidirectional Local reference clock, this clock can be used for 12A Bank Q2
A99	REFCLK_FGTL12A_Q2_ RX_CH5N	REFCLK_FGTL12A_Q2_RX _CH5N /CB57	I, DIFF	Bank FGT12A-Q2 High speed differential Clock1 negative. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2, Q3 Transceivers.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A98	REFCLK_FGTL12A_Q2_ RX_CH5P	REFCLK_FGTL12A_Q2_RX _CH5P /BY57	I, DIFF	Bank FGT12A-Q2 High speed differential Clock1 positive. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2, Q3 Transceivers.

For more details on FGTL 12C Bank transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT_12C Quad0 Channels				
B63	FGTL12C_RX_Q0_CH0N	FGTL12C_RX_Q0_CH0N /BH65	I, DIFF	Bank FGT12C-Q0 channel0 High speed differential receiver negative.
B62	FGTL12C_RX_Q0_CH0P	FGTL12C_RX_Q0_CH0P /BJ66	I, DIFF	Bank FGT12C-Q0 channel0 High speed differential receiver positive.
B66	FGTL12C_RX_Q0_CH1N	FGTL12C_RX_Q0_CH1N /BG68	I, DIFF	Bank FGT12C-Q0 channel1 High speed differential receiver negative.
B65	FGTL12C_RX_Q0_CH1P	FGTL12C_RX_Q0_CH1P /BF69	I, DIFF	Bank FGT12C-Q0 channel1 High speed differential receiver positive.
B69	FGTL12C_RX_Q0_CH2N	FGTL12C_RX_Q0_CH2N /BD65	I, DIFF	Bank FGT12C-Q0 channel2 High speed differential receiver negative.
B68	FGTL12C_RX_Q0_CH2P	FGTL12C_RX_Q0_CH2P /BE66	I, DIFF	Bank FGT12C-Q0 channel2 High speed differential receiver positive.
B72	FGTL12C_RX_Q0_CH3N	FGTL12C_RX_Q0_CH3N /BC68	I, DIFF	Bank FGT12C-Q0 channel3 High speed differential receiver negative.
B71	FGTL12C_RX_Q0_CH3P	FGTL12C_RX_Q0_CH3P /BB69	I, DIFF	Bank FGT12C-Q0 channel3 High speed differential receiver positive.
A63	FGTL12C_TX_Q0_CH0N	FGTL12C_TX_Q0_CH0N /BH59	O, DIFF	Bank FGT12C-Q0 channel0 High speed differential transmitter negative.
A62	FGTL12C_TX_Q0_CH0P	FGTL12C_TX_Q0_CH0P /BJ60	O, DIFF	Bank FGT12C-Q0 channel0 High speed differential transmitter positive.
A66	FGTL12C_TX_Q0_CH1N	FGTL12C_TX_Q0_CH1N /BG62	O, DIFF	Bank FGT12C-Q0 channel1 High speed differential transmitter negative.
A65	FGTL12C_TX_Q0_CH1P	FGTL12C_TX_Q0_CH1P /BF63	O, DIFF	Bank FGT12C-Q0 channel1 High speed differential transmitter positive.
A69	FGTL12C_TX_Q0_CH2N	FGTL12C_TX_Q0_CH2N /BD59	O, DIFF	Bank FGT12C-Q0 channel2 High speed differential transmitter negative.
A68	FGTL12C_TX_Q0_CH2P	FGTL12C_TX_Q0_CH2P /BE60	O, DIFF	Bank FGT12C-Q0 channel2 High speed differential transmitter positive.
A72	FGTL12C_TX_Q0_CH3N	FGTL12C_TX_Q0_CH3N /BC62	O, DIFF	Bank FGT12C-Q0 channel3 High speed differential transmitter negative.
A71	FGTL12C_TX_Q0_CH3P	FGTL12C_TX_Q0_CH3P /BB63	O, DIFF	Bank FGT12C-Q0 channel3 High speed differential transmitter positive.
C75	REFCLK_FGTL12C_Q0_ RX_CH0N	REFCLK_FGTL12C_Q0_RX _CH0N /BE56	I, DIFF	Bank FGT12C-Q0 High speed differential Clock0 negative. Regional reference clock, this clock can be used for 12C Bank Q0 Transceivers.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C74	REFCLK_FGTL12C_Q0_RX_CH0P	REFCLK_FGTL12C_Q0_RX_CH0P /BF57	I, DIFF	Bank FGT12C-Q0 High speed differential Clock0 positive. Regional reference clock, this clock can be used for 12C Bank Q0 Transceivers.
B75	REFCLK_FGTL12C_Q0_RX_CH1N	REFCLK_FGTL12C_Q0_RX_CH1N /BA56	I, DIFF	Bank FGT12C-Q0 High speed differential Clock1 negative. Regional reference clock, this clock can be used for 12C Bank Q0 Transceivers.
B74	REFCLK_FGTL12C_Q0_RX_CH1P	REFCLK_FGTL12C_Q0_RX_CH1P /AY57	I, DIFF	Bank FGT12C-Q0 High speed differential Clock1 positive. Regional reference clock, this clock can be used for 12C Bank Q0 Transceivers.
BANK-FGT_12C Quad1 Channels				
D63	FGTL12C_RX_Q1_CH0N	FGTL12C_RX_Q1_CH0N /AY65	I, DIFF	Bank FGT12C-Q1 channel0 High speed differential receiver negative.
D62	FGTL12C_RX_Q1_CH0P	FGTL12C_RX_Q1_CH0P /BA66	I, DIFF	Bank FGT12C-Q1 channel0 High speed differential receiver positive.
D66	FGTL12C_RX_Q1_CH1N	FGTL12C_RX_Q1_CH1N /AW68	I, DIFF	Bank FGT12C-Q1 channel1 High speed differential receiver negative.
D65	FGTL12C_RX_Q1_CH1P	FGTL12C_RX_Q1_CH1P /AV69	I, DIFF	Bank FGT12C-Q1 channel1 High speed differential receiver positive.
D69	FGTL12C_RX_Q1_CH2N	FGTL12C_RX_Q1_CH2N /AT65	I, DIFF	Bank FGT12C-Q1 channel2 High speed differential receiver negative.
D68	FGTL12C_RX_Q1_CH2P	FGTL12C_RX_Q1_CH2P /AU66	I, DIFF	Bank FGT12C-Q1 channel2 High speed differential receiver positive.
D72	FGTL12C_RX_Q1_CH3N	FGTL12C_RX_Q1_CH3N /AR68	I, DIFF	Bank FGT12C-Q1 channel3 High speed differential receiver negative.
D71	FGTL12C_RX_Q1_CH3P	FGTL12C_RX_Q1_CH3P /AP69	I, DIFF	Bank FGT12C-Q1 channel3 High speed differential receiver positive.
C63	FGTL12C_TX_Q1_CH0N	FGTL12C_TX_Q1_CH0N /AY59	O, DIFF	Bank FGT12C-Q1 channel0 High speed differential transmitter negative.
C62	FGTL12C_TX_Q1_CH0P	FGTL12C_TX_Q1_CH0P /BA60	O, DIFF	Bank FGT12C-Q1 channel0 High speed differential transmitter positive.
C66	FGTL12C_TX_Q1_CH1N	FGTL12C_TX_Q1_CH1N /AW62	O, DIFF	Bank FGT12C-Q1 channel1 High speed differential transmitter negative.
C65	FGTL12C_TX_Q1_CH1P	FGTL12C_TX_Q1_CH1P /AV63	O, DIFF	Bank FGT12C-Q1 channel1 High speed differential transmitter positive.
C69	FGTL12C_TX_Q1_CH2N	FGTL12C_TX_Q1_CH2N /AT59	O, DIFF	Bank FGT12C-Q1 channel2 High speed differential transmitter negative.
C68	FGTL12C_TX_Q1_CH2P	FGTL12C_TX_Q1_CH2P /AU60	O, DIFF	Bank FGT12C-Q1 channel2 High speed differential transmitter positive.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C72	FGTL12C_TX_Q1_CH3N	FGTL12C_TX_Q1_CH3N /AR62	O, DIFF	Bank FGT12C-Q1 channel3 High speed differential transmitter negative.
C71	FGTL12C_TX_Q1_CH3P	FGTL12C_TX_Q1_CH3P /AP63	O, DIFF	Bank FGT12C-Q1 channel3 High speed differential transmitter positive.
A75	REFCLK_FGTL12C_Q1_ RX_CH2N	REFCLK_FGTL12C_Q1_RX _CH2N /BD57	I, DIFF	Bank FGT12C-Q1 High speed differential Clock0 negative. Global reference clock, this clock can be used for 12C Bank Q0, Q1, Q2, Q3 Transceivers.
A74	REFCLK_FGTL12C_Q1_ RX_CH2P	REFCLK_FGTL12C_Q1_RX _CH2P /BB57	I, DIFF	Bank FGT12C-Q1 High speed differential Clock0 positive. Global reference clock, this clock can be used for 12C Bank Q0, Q1, Q2, Q3 Transceivers.
D75	REFCLK_FGTL12C_Q1_ RX_CH3N	REFCLK_FGTL12C_Q1_RX _CH3N /AT57	I, DIFF	Bank FGT12C-Q1 High speed differential Clock1 negative. Global reference clock, this clock can be used for 12C Bank Q0, Q1, Q2, Q3 Transceivers.
D74	REFCLK_FGTL12C_Q1_ RX_CH3P	REFCLK_FGTL12C_Q1_RX _CH3P /AR56	I, DIFF	Bank FGT12C-Q1 High speed differential Clock1 positive. Global reference clock, this clock can be used for 12C Bank Q0, Q1, Q2, Q3 Transceivers.
BANK-FGT_12C Quad2 Channels				
B78	FGTL12C_RX_Q2_CH0N	FGTL12C_RX_Q2_CH0N /AM65	I, DIFF	Bank FGT12C-Q2 channel0 High speed differential receiver negative.
B77	FGTL12C_RX_Q2_CH0P	FGTL12C_RX_Q2_CH0P /AN66	I, DIFF	Bank FGT12C-Q2 channel0 High speed differential receiver positive.
B81	FGTL12C_RX_Q2_CH1N	FGTL12C_RX_Q2_CH1N /AL68	I, DIFF	Bank FGT12C-Q2 channel1 High speed differential receiver negative.
B80	FGTL12C_RX_Q2_CH1P	FGTL12C_RX_Q2_CH1P /AK69	I, DIFF	Bank FGT12C-Q2 channel1 High speed differential receiver positive.
B84	FGTL12C_RX_Q2_CH2N	FGTL12C_RX_Q2_CH2N /AH65	I, DIFF	Bank FGT12C-Q2 channel2 High speed differential receiver negative.
B83	FGTL12C_RX_Q2_CH2P	FGTL12C_RX_Q2_CH2P /AJ66	I, DIFF	Bank FGT12C-Q2 channel2 High speed differential receiver positive.
B87	FGTL12C_RX_Q2_CH3N	FGTL12C_RX_Q2_CH3N /AG68	I, DIFF	Bank FGT12C-Q2 channel3 High speed differential receiver negative.
B86	FGTL12C_RX_Q2_CH3P	FGTL12C_RX_Q2_CH3P /AF69	I, DIFF	Bank FGT12C-Q2 channel3 High speed differential receiver positive.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A78	FGTL12C_TX_Q2_CH0N	FGTL12C_TX_Q2_CH0N /AM59	O, DIFF	Bank FGT12C-Q2 channel0 High speed differential transmitter negative.
A77	FGTL12C_TX_Q2_CH0P	FGTL12C_TX_Q2_CH0P /AN60	O, DIFF	Bank FGT12C-Q2 channel0 High speed differential transmitter positive.
A81	FGTL12C_TX_Q2_CH1N	FGTL12C_TX_Q2_CH1N /AL62	O, DIFF	Bank FGT12C-Q2 channel1 High speed differential transmitter negative.
A80	FGTL12C_TX_Q2_CH1P	FGTL12C_TX_Q2_CH1P /AK63	O, DIFF	Bank FGT12C-Q2 channel1 High speed differential transmitter positive.
A84	FGTL12C_TX_Q2_CH2N	FGTL12C_TX_Q2_CH2N /AH59	O, DIFF	Bank FGT12C-Q2 channel2 High speed differential transmitter negative.
A83	FGTL12C_TX_Q2_CH2P	FGTL12C_TX_Q2_CH2P /AJ60	O, DIFF	Bank FGT12C-Q2 channel2 High speed differential transmitter positive.
A87	FGTL12C_TX_Q2_CH3N	FGTL12C_TX_Q2_CH3N /AG62	O, DIFF	Bank FGT12C-Q2 channel3 High speed differential transmitter negative.
A86	FGTL12C_TX_Q2_CH3P	FGTL12C_TX_Q2_CH3P /AF63	O, DIFF	Bank FGT12C-Q2 channel3 High speed differential transmitter positive.
B90	REFCLK_FGTL12C_Q2_ CH8N	REFCLK_FGTL12C_Q2_CH 8N /AB57	IO, DIFF	Bank FGT12C-Q2 High speed differential Clock0 negative. Bidirectional Local reference clock, this clock can be used for 12C Bank Q2
B89	REFCLK_FGTL12C_Q2_ CH8P	REFCLK_FGTL12C_Q2_CH 8P /AD57	IO, DIFF	Bank FGT12C-Q2 High speed differential Clock0 positive. Bidirectional Local reference clock, this clock can be used for 12C Bank Q2
A90	REFCLK_FGTL12C_Q2_ RX_CH5N	REFCLK_FGTL12C_Q2_RX _CH5N /AA56	I, DIFF	Bank FGT12C-Q2 High speed differential Clock1 negative. Global reference clock, this clock can be used for 12C Bank Q0, Q1, Q2, Q3 Transceivers.
A89	REFCLK_FGTL12C_Q2_ RX_CH5P	REFCLK_FGTL12C_Q2_RX _CH5P /Y57	I, DIFF	Bank FGT12C-Q2 High speed differential Clock1 positive. Global reference clock, this clock can be used for 12C Bank Q0, Q1, Q2, Q3 Transceivers.
BANK-FGT12C Q3 Channels				
D78	FGTL12C_RX_Q3_CH0N	FGTL12C_RX_Q3_CH0N /AD65	I, DIFF	Bank FGT12C-Q3 channel0 High speed differential receiver negative.
D77	FGTL12C_RX_Q3_CH0P	FGTL12C_RX_Q3_CH0P /AE66	I, DIFF	Bank FGT12C-Q3 channel0 High speed differential receiver positive.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D81	FGTL12C_RX_Q3_CH1N	FGTL12C_RX_Q3_CH1N /AC68	I, DIFF	Bank FGT12C-Q3 channel1 High speed differential receiver negative.
D80	FGTL12C_RX_Q3_CH1P	FGTL12C_RX_Q3_CH1P /AB69	I, DIFF	Bank FGT12C-Q3 channel1 High speed differential receiver positive.
D84	FGTL12C_RX_Q3_CH2N	FGTL12C_RX_Q3_CH2N /Y65	I, DIFF	Bank FGT12C-Q3 channel2 High speed differential receiver negative.
D83	FGTL12C_RX_Q3_CH2P	FGTL12C_RX_Q3_CH2P /AA66	I, DIFF	Bank FGT12C-Q3 channel2 High speed differential receiver positive.
D87	FGTL12C_RX_Q3_CH3N	FGTL12C_RX_Q3_CH3N /W68	I, DIFF	Bank FGT12C-Q3 channel3 High speed differential receiver negative.
D86	FGTL12C_RX_Q3_CH3P	FGTL12C_RX_Q3_CH3P /V69	I, DIFF	Bank FGT12C-Q3 channel3 High speed differential receiver positive.
C78	FGTL12C_TX_Q3_CH0N	FGTL12C_TX_Q3_CH0N /AD59	O, DIFF	Bank FGT12C-Q3 channel0 High speed differential transmitter negative.
C77	FGTL12C_TX_Q3_CH0P	FGTL12C_TX_Q3_CH0P /AE60	O, DIFF	Bank FGT12C-Q3 channel0 High speed differential transmitter positive.
C81	FGTL12C_TX_Q3_CH1N	FGTL12C_TX_Q3_CH1N /AC62	O, DIFF	Bank FGT12C-Q3 channel1 High speed differential transmitter negative.
C80	FGTL12C_TX_Q3_CH1P	FGTL12C_TX_Q3_CH1P /AB63	O, DIFF	Bank FGT12C-Q3 channel1 High speed differential transmitter positive.
C84	FGTL12C_TX_Q3_CH2N	FGTL12C_TX_Q3_CH2N /Y59	O, DIFF	Bank FGT12C-Q3 channel2 High speed differential transmitter negative.
C83	FGTL12C_TX_Q3_CH2P	FGTL12C_TX_Q3_CH2P /AA60	O, DIFF	Bank FGT12C-Q3 channel2 High speed differential transmitter positive.
C87	FGTL12C_TX_Q3_CH3N	FGTL12C_TX_Q3_CH3N /W62	O, DIFF	Bank FGT12C-Q3 channel3 High speed differential transmitter negative.
C86	FGTL12C_TX_Q3_CH3P	FGTL12C_TX_Q3_CH3P /V63	O, DIFF	Bank FGT12C-Q3 channel3 High speed differential transmitter positive.
C90	REFCLK_FGTL12C_Q3_ RX_CH6N	REFCLK_FGTL12C_Q3_RX _CH6N /AF57	I, DIFF	Bank FGT12C-Q3 High speed differential Clock0 negative. Regional reference clock, this clock can be used for 12C Bank Q3 Transceivers.
C89	REFCLK_FGTL12C_Q3_ RX_CH6P	REFCLK_FGTL12C_Q3_RX _CH6P /AE56	I, DIFF	Bank FGT12C-Q3 High speed differential Clock0 positive. Regional reference clock, this clock can be used for 12C Bank Q3 Transceivers.
D90	REFCLK_FGTL12C_Q3_ RX_CH7N	REFCLK_FGTL12C_Q3_RX _CH7N /W56	I, DIFF	Bank FGT12C-Q3 High speed differential Clock1 negative. Regional reference clock, this clock can be used for 12C Bank Q3 Transceivers.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D89	REFCLK_FGTL12C_Q3_ RX_CH7P	REFCLK_FGTL12C_Q3_RX _CH7P /V55	I, DIFF	Bank FGT12C-Q3 High speed differential Clock1 positive. Regional reference clock, this clock can be used for 12C Bank Q3 Transceivers.

2.7.4 Power, Control & Reset Input

The Intel Agilex 7 SoC and FPGA SOM works with 12V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. In Board-to-Board Connector1, Ground pins are also distributed throughout the connector for better performance. In Board-to-Board Connector2, there are also Hardware Reset signal for resetting the CPU from Carrier Board and SOM Power Enable Signal for turning ON/OFF the SOM Power from the Carrier Board. Also, 3V RTC Power & 5V standby powers are connected to Board-to-Board Connector2.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	Pin Name	Signal Type/ Termination	Description
D8, C5, C8, D7, C7, C4, D6, B2, B3, A8, B1, D5, A7, D4, D3, A6, D2, D1, A5, C2, C6, A4, C1, B4, A3, B5, B6, A2, B7, B8, C3, A1	VCC_12V	NA	Power	12V SOM Input Power.
C11	VSTBY_5V	NA	Power	5V Standby Power.
C12	VRTC_3V0	NA	Power	3V RTC Power.
B11	SOMPWR_EN	NA	OD/ Input	Control signal for controlling SOM Power.
B13	HPS_RESET_OUT(GPIO1_22)	HPS_IOB_23/ P21	1.8V Input/ 10K PU	Control Signal to reset the CPU.
A91, A70, A9, A82, A67, A23, A73, A76, A40, A64, A16, A43, A85, A61, A46, A79, A94, A49, A37, A100, A52, A88, A97, A55, A34, A10, A58, B91, B88, B85, B82, B79, B9, B10, B76, B73, B97, B67, B94, B16, B64, B61, B37, B40, B58, B55, B23, B52, B70, B100, B43, B49, B46, B34, C73, C88, C76, C94, C16, C10, C9, C79, C82, C91, C85, C23, C97, C100, C70, C67, C28, C64, C61, C31, C43, C49, C34, C58, C55, C37, C52, C40, C46, D76, D73, D70, D10, D64, D16, D88, D9, D79, D85, D82, D100, D23, D91, D94, D97, D67, D28, D61, D46, D31, D40, D58, D34, D55, D52, D37, D49, D43,	GND	NA	Power	Ground.

2.8 Board to Board Connector3

The Intel Agilex 7 SoC and FPGA SOM Board to Board Connector3 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector3 are explained in the following sections. The Board-to-Board Connector3 (J8) is physically located on bottom side of the SOM as shown below.

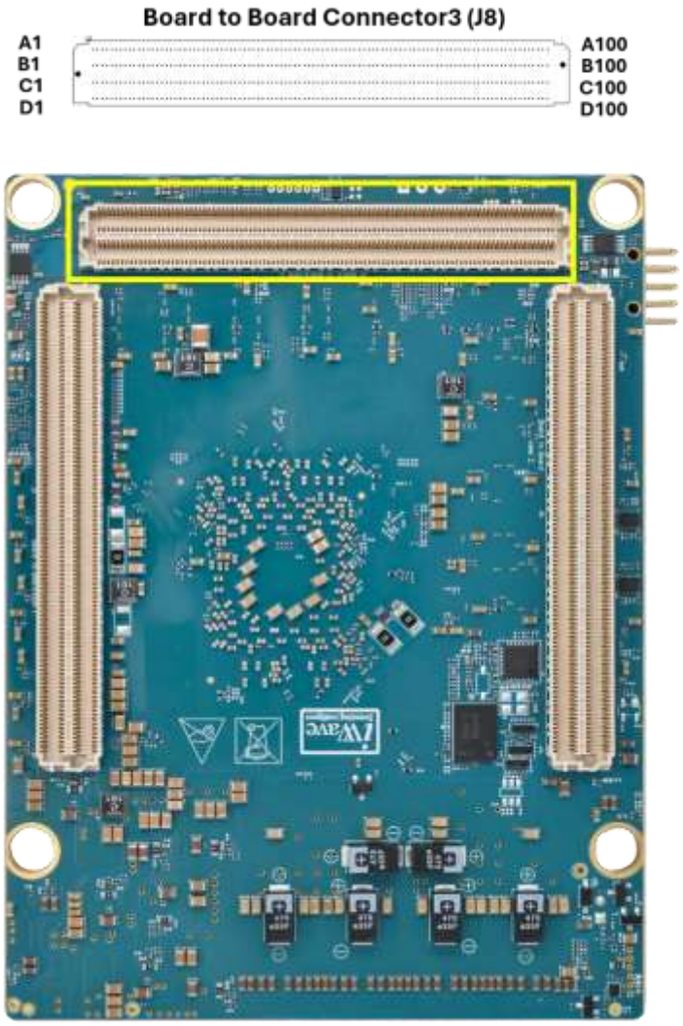

Figure 9: Board-to-Board Connector3

Number of Pins - 400

Connector Part Number - ASP-209946-01 from Samtech

Mating Connector - ASP-214802-01 from Samtech

Staking Height - 5mm

Table 12: Board to Board Connector3 Pinout

B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name
Row-A		Row-B		Row-C		Row-D	
A1	GND	B1	GND	C1	GND	D1	GND
A2	FGTL12A_TX_Q3_CH0P	B2	FGTL12A_RX_Q3_CH0P	C2	FGTL13C_TX_Q0_CH0P	D2	FGTL13C_RX_Q0_CH0P
A3	FGTL12A_TX_Q3_CH0N	B3	FGTL12A_RX_Q3_CH0N	C3	FGTL13C_TX_Q0_CH0N	D3	FGTL13C_RX_Q0_CH0N
A4	GND	B4	GND	C4	GND	D4	GND
A5	FGTL12A_TX_Q3_CH1P	B5	FGTL12A_RX_Q3_CH1P	C5	FGTL13C_TX_Q0_CH1P	D5	FGTL13C_RX_Q0_CH1P
A6	FGTL12A_TX_Q3_CH1N	B6	FGTL12A_RX_Q3_CH1N	C6	FGTL13C_TX_Q0_CH1N	D6	FGTL13C_RX_Q0_CH1N
A7	GND	B7	GND	C7	GND	D7	GND
A8	FGTL12A_TX_Q3_CH2P	B8	FGTL12A_RX_Q3_CH2P	C8	FGTL13C_TX_Q0_CH2P	D8	FGTL13C_RX_Q0_CH2P
A9	FGTL12A_TX_Q3_CH2N	B9	FGTL12A_RX_Q3_CH2N	C9	FGTL13C_TX_Q0_CH2N	D9	FGTL13C_RX_Q0_CH2N
A10	GND	B10	GND	C10	GND	D10	GND
A11	FGTL12A_TX_Q3_CH3P	B11	FGTL12A_RX_Q3_CH3P	C11	FGTL13C_TX_Q0_CH3P	D11	FGTL13C_RX_Q0_CH3P
A12	FGTL12A_TX_Q3_CH3N	B12	FGTL12A_RX_Q3_CH3N	C12	FGTL13C_TX_Q0_CH3N	D12	FGTL13C_RX_Q0_CH3N
A13	GND	B13	GND	C13	GND	D13	GND
A14	REFCLK_FGTL12A_Q3_RX_CH6P	B14	REFCLK_FGTL12A_Q3_RX_CH7P	C14	REFCLK_FGTL13C_Q0_RX_CH0P	D14	REFCLK_FGTL13C_Q0_RX_CH1P
A15	REFCLK_FGTL12A_Q3_RX_CH6N	B15	REFCLK_FGTL12A_Q3_RX_CH7N	C15	REFCLK_FGTL13C_Q0_RX_CH0N	D15	REFCLK_FGTL13C_Q0_RX_CH1N
A16	GND	B16	GND	C16	GND	D16	GND
A17	FGTL13C_TX_Q1_CH0P	B17	FGTL13C_RX_Q1_CH0P	C17	FGTL13C_TX_Q2_CH0P	D17	FGTL13C_RX_Q2_CH0P
A18	FGTL13C_TX_Q1_CH0N	B18	FGTL13C_RX_Q1_CH0N	C18	FGTL13C_TX_Q2_CH0N	D18	FGTL13C_RX_Q2_CH0N
A19	GND	B19	GND	C19	GND	D19	GND
A20	FGTL13C_TX_Q1_CH1P	B20	FGTL13C_RX_Q1_CH1P	C20	FGTL13C_TX_Q2_CH1P	D20	FGTL13C_RX_Q2_CH1P
A21	FGTL13C_TX_Q1_CH1N	B21	FGTL13C_RX_Q1_CH1N	C21	FGTL13C_TX_Q2_CH1N	D21	FGTL13C_RX_Q2_CH1N
A22	GND	B22	GND	C22	GND	D22	GND
A23	FGTL13C_TX_Q1_CH2P	B23	FGTL13C_RX_Q1_CH2P	C23	FGTL13C_TX_Q2_CH2P	D23	FGTL13C_RX_Q2_CH2P
A24	FGTL13C_TX_Q1_CH2N	B24	FGTL13C_RX_Q1_CH2N	C24	FGTL13C_TX_Q2_CH2N	D24	FGTL13C_RX_Q2_CH2N
A25	GND	B25	GND	C25	GND	D25	GND
A26	FGTL13C_TX_Q1_CH3P	B26	FGTL13C_RX_Q1_CH3P	C26	FGTL13C_TX_Q2_CH3P	D26	FGTL13C_RX_Q2_CH3P
A27	FGTL13C_TX_Q1_CH3N	B27	FGTL13C_RX_Q1_CH3N	C27	FGTL13C_TX_Q2_CH3N	D27	FGTL13C_RX_Q2_CH3N
A28	GND	B28	GND	C28	GND	D28	GND
A29	REFCLK_FGTL13C_Q1_RX_CH2P	B29	REFCLK_FGTL13C_Q1_RX_CH3P	C29	REFCLK_FGTL13C_Q2_RX_CH5P	D29	REFCLK_FGTL13C_Q2_CH8P
A30	REFCLK_FGTL13C_Q1_RX_CH2N	B30	REFCLK_FGTL13C_Q1_RX_CH3N	C30	REFCLK_FGTL13C_Q2_RX_CH5N	D30	REFCLK_FGTL13C_Q2_CH8N
A31	GND	B31	GND	C31	GND	D31	GND
A32	FGTL13C_TX_Q3_CH0P	B32	FGTL13C_RX_Q3_CH0P	C32	FHTR13C_TX_CH0P	D32	FHTR13C_RX_CH0P
A33	FGTL13C_TX_Q3_CH0N	B33	FGTL13C_RX_Q3_CH0N	C33	FHTR13C_TX_CH0N	D33	FHTR13C_RX_CH0N
A34	GND	B34	GND	C34	GND	D34	GND
A35	FGTL13C_TX_Q3_CH1P	B35	FGTL13C_RX_Q3_CH1P	C35	FHTR13C_TX_CH1P	D35	FHTR13C_RX_CH1P
A36	FGTL13C_TX_Q3_CH1N	B36	FGTL13C_RX_Q3_CH1N	C36	FHTR13C_TX_CH1N	D36	FHTR13C_RX_CH1N
A37	GND	B37	GND	C37	GND	D37	GND
A38	FGTL13C_TX_Q3_CH2P	B38	FGTL13C_RX_Q3_CH2P	C38	FHTR13C_TX_CH2P	D38	FHTR13C_RX_CH2P
A39	FGTL13C_TX_Q3_CH2N	B39	FGTL13C_RX_Q3_CH2N	C39	FHTR13C_TX_CH2N	D39	FHTR13C_RX_CH2N

B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name
A40	GND	**B40**	GND	**C40**	GND	**D40**	GND
A41	FGTL13C_TX_Q3_CH3P	**B41**	FGTL13C_RX_Q3_CH3P	**C41**	FHTR13C_TX_CH3P	**D41**	FHTR13C_RX_CH3P
A42	FGTL13C_TX_Q3_CH3N	**B42**	FGTL13C_RX_Q3_CH3N	**C42**	FHTR13C_TX_CH3N	**D42**	FHTR13C_RX_CH3N
A43	GND	**B43**	GND	**C43**	GND	**D43**	GND
A44	REFCLK_FGTL13C_Q3_RX_CH6P	**B44**	REFCLK_FGTL13C_Q3_RX_CH7P	**C44**	REFCLK_FHTR13C_CH0P	**D44**	REFCLK_FHTR13C_CH1P
A45	REFCLK_FGTL13C_Q3_RX_CH6N	**B45**	REFCLK_FGTL13C_Q3_RX_CH7N	**C45**	REFCLK_FHTR13C_CH0N	**D45**	REFCLK_FHTR13C_CH1N
A46	GND	**B46**	GND	**C46**	GND	**D46**	GND
A47	FHTR13A_TX_CH0P	**B47**	FHTR13A_RX_CH0P	**C47**	FGTL13A_TX_Q0_CH0P	**D47**	FGTL13A_RX_Q0_CH0P
A48	FHTR13A_TX_CH0N	**B48**	FHTR13A_RX_CH0N	**C48**	FGTL13A_TX_Q0_CH0N	**D48**	FGTL13A_RX_Q0_CH0N
A49	GND	**B49**	GND	**C49**	GND	**D49**	GND
A50	FHTR13A_TX_CH1P	**B50**	FHTR13A_RX_CH1P	**C50**	FGTL13A_TX_Q0_CH1P	**D50**	FGTL13A_RX_Q0_CH1P
A51	FHTR13A_TX_CH1N	**B51**	FHTR13A_RX_CH1N	**C51**	FGTL13A_TX_Q0_CH1N	**D51**	FGTL13A_RX_Q0_CH1N
A52	GND	**B52**	GND	**C52**	GND	**D52**	GND
A53	FHTR13A_TX_CH2P	**B53**	FHTR13A_RX_CH2P	**C53**	FGTL13A_TX_Q0_CH2P	**D53**	FGTL13A_RX_Q0_CH2P
A54	FHTR13A_TX_CH2N	**B54**	FHTR13A_RX_CH2N	**C54**	FGTL13A_TX_Q0_CH2N	**D54**	FGTL13A_RX_Q0_CH2N
A55	GND	**B55**	GND	**C55**	GND	**D55**	GND
A56	FHTR13A_TX_CH3P	**B56**	FHTR13A_RX_CH3P	**C56**	FGTL13A_TX_Q0_CH3P	**D56**	FGTL13A_RX_Q0_CH3P
A57	FHTR13A_TX_CH3N	**B57**	FHTR13A_RX_CH3N	**C57**	FGTL13A_TX_Q0_CH3N	**D57**	FGTL13A_RX_Q0_CH3N
A58	GND	**B58**	GND	**C58**	GND	**D58**	GND
A59	REFCLK_FHTR13A_CH0P	**B59**	REFCLK_FHTR13A_CH1P	**C59**	REFCLK_FGTL13A_Q0_RX_CH0P	**D59**	REFCLK_FGTL13A_Q0_RX_CH1P
A60	REFCLK_FHTR13A_CH0N	**B60**	REFCLK_FHTR13A_CH1N	**C60**	REFCLK_FGTL13A_Q0_RX_CH0N	**D60**	REFCLK_FGTL13A_Q0_RX_CH1N
A61	GND	**B61**	GND	**C61**	GND	**D61**	GND
A62	FGTL13A_TX_Q1_CH0P	**B62**	FGTL13A_RX_Q1_CH0P	**C62**	FGTL13A_TX_Q2_CH0P	**D62**	FGTL13A_RX_Q2_CH0P
A63	FGTL13A_TX_Q1_CH0N	**B63**	FGTL13A_RX_Q1_CH0N	**C63**	FGTL13A_TX_Q2_CH0N	**D63**	FGTL13A_RX_Q2_CH0N
A64	GND	**B64**	GND	**C64**	GND	**D64**	GND
A65	FGTL13A_TX_Q1_CH1P	**B65**	FGTL13A_RX_Q1_CH1P	**C65**	FGTL13A_TX_Q2_CH1P	**D65**	FGTL13A_RX_Q2_CH1P
A66	FGTL13A_TX_Q1_CH1N	**B66**	FGTL13A_RX_Q1_CH1N	**C66**	FGTL13A_TX_Q2_CH1N	**D66**	FGTL13A_RX_Q2_CH1N
A67	GND	**B67**	GND	**C67**	GND	**D67**	GND
A68	FGTL13A_TX_Q1_CH2P	**B68**	FGTL13A_RX_Q1_CH2P	**C68**	FGTL13A_TX_Q2_CH2P	**D68**	FGTL13A_RX_Q2_CH2P
A69	FGTL13A_TX_Q1_CH2N	**B69**	FGTL13A_RX_Q1_CH2N	**C69**	FGTL13A_TX_Q2_CH2N	**D69**	FGTL13A_RX_Q2_CH2N
A70	GND	**B70**	GND	**C70**	GND	**D70**	GND
A71	FGTL13A_TX_Q1_CH3P	**B71**	FGTL13A_RX_Q1_CH3P	**C71**	FGTL13A_TX_Q2_CH3P	**D71**	FGTL13A_RX_Q2_CH3P
A72	FGTL13A_TX_Q1_CH3N	**B72**	FGTL13A_RX_Q1_CH3N	**C72**	FGTL13A_TX_Q2_CH3N	**D72**	FGTL13A_RX_Q2_CH3N
A73	GND	**B73**	GND	**C73**	GND	**D73**	GND
A74	REFCLK_FGTL13A_Q1_RX_CH2P	**B74**	REFCLK_FGTL13A_Q1_RX_CH3P	**C74**	REFCLK_FGTL13A_Q2_RX_CH5P	**D74**	REFCLK_FGTL13A_Q2_CH8P
A75	REFCLK_FGTL13A_Q1_RX_CH2N	**B75**	REFCLK_FGTL13A_Q1_RX_CH3N	**C75**	REFCLK_FGTL13A_Q2_RX_CH5N	**D75**	REFCLK_FGTL13A_Q2_CH8N
A76	GND	**B76**	GND	**C76**	GND	**D76**	GND
A77	FGTL13A_TX_Q3_CH0p	**B77**	FGTL13A_RX_Q3_CH0P	**C77**	NC	**D77**	NC
A78	FGTL13A_TX_Q3_CH0n	**B78**	FGTL13A_RX_Q3_CH0N	**C78**	NC	**D78**	NC
A79	GND	**B79**	GND	**C79**	GND	**D79**	GND
A80	FGTL13A_TX_Q3_CH1p	**B80**	FGTL13A_RX_Q3_CH1P	**C80**	NC	**D80**	NC

B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name
A81	FGTL13A_TX_Q3_CH1n	**B81**	FGTL13A_RX_Q3_CH1N	**C81**	NC	**D81**	NC
A82	GND	**B82**	GND	**C82**	GND	**D82**	GND
A83	FGTL13A_TX_Q3_CH2p	**B83**	FGTL13A_RX_Q3_CH2P	**C83**	NC	**D83**	NC
A84	FGTL13A_TX_Q3_CH2n	**B84**	FGTL13A_RX_Q3_CH2N	**C84**	NC	**D84**	NC
A85	GND	**B85**	GND	**C85**	GND	**D85**	GND
A86	FGTL13A_TX_Q3_CH3p	**B86**	FGTL13A_RX_Q3_CH3P	**C86**	NC	**D86**	NC
A87	FGTL13A_TX_Q3_CH3n	**B87**	FGTL13A_RX_Q3_CH3N	**C87**	NC	**D87**	NC
A88	GND	**B88**	GND	**C88**	GND	**D88**	GND
A89	REFCLK_FGTL13A_Q3_RX_CH6P	**B89**	REFCLK_FGTL13A_Q3_RX_CH7P	**C89**	NC	**D89**	NC
A90	REFCLK_FGTL13A_Q3_RX_CH6N	**B90**	REFCLK_FGTL13A_Q3_RX_CH7N	**C90**	NC	**D90**	NC
A91	GND	**B91**	GND	**C91**	GND	**D91**	GND
A92	NC	**B92**	NC	**C92**	NC	**D92**	NC
A93	NC	**B93**	NC	**C93**	NC	**D93**	NC
A94	GND	**B94**	GND	**C94**	GND	**D94**	GND
A95	NC	**B95**	NC	**C95**	NC	**D95**	NC
A96	NC	**B96**	NC	**C96**	NC	**D96**	NC
A97	GND	**B97**	GND	**C97**	GND	**D97**	GND
A98	NC	**B98**	NC	**C98**	TEMPDIODE_DTS_DP	**D98**	TEMPDIODE_13A_GXF_DP
A99	NC	**B99**	NC	**C99**	TEMPDIODE_DTS_DN	**D99**	TEMPDIODE_13A_GXF_DN
A100	GND	**B100**	GND	**C100**	GND	**D100**	GND

2.8.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector3 from Intel Agilex 7 SoC and FPGA device's FPGA is explained in the following section.

2.8.1.1 High Speed Transceivers

The Intel Agilex 7 SoC and FPGA SOM supports 44 high speed transceiver channels (4 Channels from FGT_12A Bank Quad3, 16 Channels from FGT_13A Bank Quad [3:0], 16 Channels from FGT_13C Bank Quad [3:0], 4 Channels from FHT_13A Bank and 4 Channels from FHT_13C Bank) on Board-to-Board connector3. In Intel Agilex 7 SoC and FPGA SOM, the FGT Transceivers connected to Board-to-Board Connector3 is capable of running up to a maximum speed of 32Gbps in NRZ Format or 58Gbps in PAM4 Format while the FHT Transceivers are capable of running up to a maximum of 58Gbps in NRZ Format or 116Gbps speed in PAM4 Format. These transceivers can be used to interface to multiple high-speed interface protocols. Each 4 Channel Transceiver Bank supports two dedicated reference clock input pairs.

For more details on FGTL 12A transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT12A Q3 Channels				
B3	FGTL12A_RX_Q3_CH0N	FGTL12A_RX_Q3_CH0N/ BT65	I, DIFF	Bank FGTL12A-Q3 channel0 High speed differential receiver negative.
B2	FGTL12A_RX_Q3_CH0P	FGTL12A_RX_Q3_CH0P/ BU66	I, DIFF	Bank FGTL12A-Q3 channel0 High speed differential receiver positive.
B6	FGTL12A_RX_Q3_CH1N	FGTL12A_RX_Q3_CH1N/ BR68	O, DIFF	Bank FGTL12A-Q3 channel1 High speed differential receiver negative.
B5	FGTL12A_RX_Q3_CH1P	FGTL12A_RX_Q3_CH1P/ BP69	O, DIFF	Bank FGTL12A-Q3 channel1 High speed differential receiver positive.
B9	FGTL12A_RX_Q3_CH2N	FGTL12A_RX_Q3_CH2N/ BM65	I, DIFF	Bank FGTL12A-Q3 channel2 High speed differential receiver negative.
B8	FGTL12A_RX_Q3_CH2P	FGTL12A_RX_Q3_CH2P/ BN66	I, DIFF	Bank FGTL12A-Q3 channel2 High speed differential receiver positive.
B12	FGTL12A_RX_Q3_CH3N	FGTL12A_RX_Q3_CH3N/ BL68	O, DIFF	Bank FGTL12A-Q3 channel3 High speed differential receiver negative.
B11	FGTL12A_RX_Q3_CH3P	FGTL12A_RX_Q3_CH3P/ BK69	O, DIFF	Bank FGTL12A-Q3 channel3 High speed differential receiver positive.
A3	FGTL12A_TX_Q3_CH0N	FGTL12A_TX_Q3_CH0N/ BT59	I, DIFF	Bank FGTL12A-Q3 channel0 High speed differential transmitter negative.
A2	FGTL12A_TX_Q3_CH0P	FGTL12A_TX_Q3_CH0P/ BU60	I, DIFF	Bank FGTL12A-Q3 channel0 High speed differential transmitter positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A6	FGTL12A_TX_Q3_CH1N	FGTL12A_TX_Q3_CH1N/ BR62	O, DIFF	Bank FGTL12A-Q3 channel1 High speed differential transmitter negative.
A5	FGTL12A_TX_Q3_CH1P	FGTL12A_TX_Q3_CH1P/ BP63	O, DIFF	Bank FGTL12A-Q3 channel1 High speed differential transmitter positive.
A9	FGTL12A_TX_Q3_CH2N	FGTL12A_TX_Q3_CH2N/ BM59	I, DIFF	Bank FGTL12A-Q3 channel2 High speed differential transmitter negative.
A8	FGTL12A_TX_Q3_CH2P	FGTL12A_TX_Q3_CH2P/ BN60	I, DIFF	Bank FGTL12A-Q3 channel2 High speed differential transmitter positive.
A12	FGTL12A_TX_Q3_CH3N	FGTL12A_TX_Q3_CH3N/ BL62	O, DIFF	Bank FGTL12A-Q3 channel3 High speed differential transmitter negative.
A11	FGTL12A_TX_Q3_CH3P	FGTL12A_TX_Q3_CH3P/ BK63	O, DIFF	Bank FGTL12A-Q3 channel3 High speed differential transmitter positive.
A15	REFCLK_FGTL12A_Q3_ RX_CH6N	REFCLK_FGTL12A_Q3_RX _CH6N/ BR56	I, DIFF	Bank FGT12A-Q3 High speed differential Clock1 positive. Regional reference clock, this clock can be used for 12A Bank Q2 and Q3 Transceivers.
A14	REFCLK_FGTL12A_Q3_ RX_CH6P	REFCLK_FGTL12A_Q3_RX _CH6P/ BP57	I, DIFF	Bank FGT12A-Q3 High speed differential Clock1 negative. Regional reference clock, this clock can be used for 12A Bank Q2 and Q3 Transceivers.
B15	REFCLK_FGTL12A_Q3_ RX_CH7N	REFCLK_FGTL12A_Q3_RX _CH7N/ BN56	I, DIFF	Bank FGT12A-Q3 High speed differential Clock2 positive. Regional reference clock, this clock can be used for 12A Bank Q2 and Q3 Transceivers.
B14	REFCLK_FGTL12A_Q3_ RX_CH7P	REFCLK_FGTL12A_Q3_RX _CH7P/ BL56	I, DIFF	Bank FGT12A-Q3 High speed differential Clock2 negative. Regional reference clock, this clock can be used for 12A Bank Q2 and Q3 Transceivers.

For more details on FGTL 13A transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT_13A Quad0 Channels				
D48	FGTL13A_RX_Q0_CH0N	FGTR13A_RX_Q0_CH0N/ BL2	I, DIFF	Bank FGTL13A-Q0 channel0 High speed differential receiver negative.
D47	FGTL13A_RX_Q0_CH0P	FGTR13A_RX_Q0_CH0P/ BM1	I, DIFF	Bank FGTL13A-Q0 channel0 High speed differential receiver positive.
D51	FGTL13A_RX_Q0_CH1N	FGTR13A_RX_Q0_CH1N/ BP5	I, DIFF	Bank FGTL13A-Q0 channel1 High speed differential receiver negative.
D50	FGTL13A_RX_Q0_CH1P	FGTR13A_RX_Q0_CH1P/ BN4	I, DIFF	Bank FGTL13A-Q0 channel1 High speed differential receiver positive.
D54	FGTL13A_RX_Q0_CH2N	FGTR13A_RX_Q0_CH2N/ BR2	I, DIFF	Bank FGTL13A-Q0 channel2 High speed differential receiver negative.
D53	FGTL13A_RX_Q0_CH2P	FGTR13A_RX_Q0_CH2P/ BT1	I, DIFF	Bank FGTL13A-Q0 channel2 High speed differential receiver positive.
D57	FGTL13A_RX_Q0_CH3N	FGTR13A_RX_Q0_CH3N/ BV5	I, DIFF	Bank FGTL13A-Q0 channel3 High speed differential receiver negative.
D56	FGTL13A_RX_Q0_CH3P	FGTR13A_RX_Q0_CH3P/ BU4	I, DIFF	Bank FGTL13A-Q0 channel3 High speed differential receiver positive.
C48	FGTL13A_TX_Q0_CH0N	FGTR13A_TX_Q0_CH0N/ BK11	I, DIFF	Bank FGTL13A-Q0 channel0 High speed differential transmitter negative.
C47	FGTL13A_TX_Q0_CH0P	FGTR13A_TX_Q0_CH0P/ BJ10	I, DIFF	Bank FGTL13A-Q0 channel0 High speed differential transmitter positive.
C51	FGTL13A_TX_Q0_CH1N	FGTR13A_TX_Q0_CH1N/ BL8	O, DIFF	Bank FGTL13A-Q0 channel1 High speed differential transmitter negative.
C50	FGTL13A_TX_Q0_CH1P	FGTR13A_TX_Q0_CH1P/ BM7	O, DIFF	Bank FGTL13A-Q0 channel1 High speed differential transmitter positive.
C54	FGTL13A_TX_Q0_CH2N	FGTR13A_TX_Q0_CH2N/ BP11	O, DIFF	Bank FGTL13A-Q0 channel2 High speed differential transmitter negative.
C53	FGTL13A_TX_Q0_CH2P	FGTR13A_TX_Q0_CH2P/ BN10	O, DIFF	Bank FGTL13A-Q0 channel2 High speed differential transmitter positive.
C57	FGTL13A_TX_Q0_CH3N	FGTR13A_TX_Q0_CH3N/ BR8	O, DIFF	Bank FGTL13A-Q0 channel3 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C56	FGTL13A_TX_Q0_CH3P	FGTR13A_TX_Q0_CH3P/ BT7	O, DIFF	Bank FGTL13A-Q0 channel3 High speed differential transmitter positive.
C60	REFCLK_FGTL13A_Q0_ RX_CH0N	REFCLK_FGTR13A_Q0_RX _CH0N/ BU14	I, DIFF	Bank FGTL 13A-Q0 differential reference clock0 negative. Regional reference clock, this clock can be used for 13A Bank Q0 Transceivers.
C59	REFCLK_FGTL13A_Q0_ RX_CH0P	REFCLK_FGTR13A_Q0_RX _CH0P/ BR14	I, DIFF	Bank FGTL 13A-Q0 differential reference clock0 positive. Regional reference clock, this clock can be used for 13A Bank Q0 Transceivers.
D60	REFCLK_FGTL13A_Q0_ RX_CH1N	REFCLK_FGTR13A_Q0_RX _CH1N/ BJ14	I, DIFF	Bank FGTL 13A-Q0 differential reference clock1 negative. Regional reference clock, this clock can be used for 13A Bank Q0 Transceivers.
D59	REFCLK_FGTL13A_Q0_ RX_CH1P	REFCLK_FGTR13A_Q0_RX _CH1P/ BK13	I, DIFF	Bank FGTL 13A-Q0 differential reference clock1 positive. Regional reference clock, this clock can be used for 13A Bank Q0 Transceivers.
BANK-FGT_13A Quad1 Channels				
B63	FGTL13A_RX_Q1_CH0N	FGTR13A_RX_Q1_CH0N/ BW2	I, DIFF	Bank FGTR13A-Q1 channel0 High speed differential receiver negative.
B62	FGTL13A_RX_Q1_CH0P	FGTR13A_RX_Q1_CH0P/ BY1	I, DIFF	Bank FGTR13A-Q1 channel0 High speed differential receiver positive.
B66	FGTL13A_RX_Q1_CH1N	FGTR13A_RX_Q1_CH1N/ CB5	I, DIFF	Bank FGTR13A-Q1 channel1 High speed differential receiver negative.
B65	FGTL13A_RX_Q1_CH1P	FGTR13A_RX_Q1_CH1P/ CA4	I, DIFF	Bank FGTR13A-Q1 channel1 High speed differential receiver positive.
B69	FGTL13A_RX_Q1_CH2N	FGTR13A_RX_Q1_CH2N/ CC2	I, DIFF	Bank FGTR13A-Q1 channel2 High speed differential receiver negative.
B68	FGTL13A_RX_Q1_CH2P	FGTR13A_RX_Q1_CH2P/ CD1	I, DIFF	Bank FGTR13A-Q1 channel2 High speed differential receiver positive.
B72	FGTL13A_RX_Q1_CH3N	FGTR13A_RX_Q1_CH3N/ CF5	I, DIFF	Bank FGTR13A-Q1 channel3 High speed differential receiver negative.
B71	FGTL13A_RX_Q1_CH3P	FGTR13A_RX_Q1_CH3P/ CE4	I, DIFF	Bank FGTR13A-Q1 channel3 High speed differential receiver positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A63	FGTL13A_TX_Q1_CH0N	FGTR13A_TX_Q1_CH0N/ BV11	O, DIFF	Bank FGTR13A-Q1 channel0 High speed differential transmitter negative.
A62	FGTL13A_TX_Q1_CH0P	FGTR13A_TX_Q1_CH0P/ BU10	O, DIFF	Bank FGTR13A-Q1 channel0 High speed differential transmitter positive.
A66	FGTL13A_TX_Q1_CH1N	FGTR13A_TX_Q1_CH1N/ BW8	O, DIFF	Bank FGTR13A-Q1 channel1 High speed differential transmitter negative.
A65	FGTL13A_TX_Q1_CH1P	FGTR13A_TX_Q1_CH1P/ BY7	O, DIFF	Bank FGTR13A-Q1 channel1 High speed differential transmitter positive.
A69	FGTL13A_TX_Q1_CH2N	FGTR13A_TX_Q1_CH2N/ CB11	O, DIFF	Bank FGTR13A-Q1 channel2 High speed differential transmitter negative.
A68	FGTL13A_TX_Q1_CH2P	FGTR13A_TX_Q1_CH2P/ CA10	O, DIFF	Bank FGTR13A-Q1 channel2 High speed differential transmitter positive.
A72	FGTL13A_TX_Q1_CH3N	FGTR13A_TX_Q1_CH3N/ CC8	O, DIFF	Bank FGTR13A-Q1 channel3 High speed differential transmitter negative.
A71	FGTL13A_TX_Q1_CH3P	FGTR13A_TX_Q1_CH3P/ CD7	O, DIFF	Bank FGTR13A-Q1 channel3 High speed differential transmitter positive.
A75	REFCLK_FGTL13A_Q1_ RX_CH2N	REFCLK_FGTR13A_Q1_RX _CH2N/ BP13	I, DIFF	Bank FGTR13A-Q1 differential reference clock0 negative. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2, Q3 Transceivers.
A74	REFCLK_FGTL13A_Q1_ RX_CH2P	REFCLK_FGTR13A_Q1_RX _CH2P/ BN14	I, DIFF	Bank FGTR13A-Q1 differential reference clock0 positive. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2, Q3 Transceivers.
B75	REFCLK_FGTL13A_Q1_ RX_CH3N	REFCLK_FGTR13A_Q1_RX _CH3N/ CC14	I, DIFF	Bank FGTR13A-Q1 differential reference clock1 negative. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2, Q3 Transceivers.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B74	REFCLK_FGTL13A_Q1_ RX_CH3P	REFCLK_FGTR13A_Q1_RX _CH3P/ CE14	I, DIFF	Bank FGTR13A-Q1 differential reference clock1 positive. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2, Q3 Transceivers.
BANK-FGT_13A Quad2 Channels				
D63	FGTL13A_RX_Q2_CH0N	FGTR13A_RX_Q2_CH0N/ CG2	I, DIFF	Bank FGTR13A-Q2 channel0 High speed differential receiver negative.
D62	FGTL13A_RX_Q2_CH0P	FGTR13A_RX_Q2_CH0P/ CH1	I, DIFF	Bank FGTR13A-Q2 channel0 High speed differential receiver positive.
D66	FGTL13A_RX_Q2_CH1N	FGTR13A_RX_Q2_CH1N/ CK5	I, DIFF	Bank FGTR13A-Q2 channel1 High speed differential receiver negative.
D65	FGTL13A_RX_Q2_CH1P	FGTR13A_RX_Q2_CH1P/ CJ4	I, DIFF	Bank FGTR13A-Q2 channel1 High speed differential receiver positive.
D69	FGTL13A_RX_Q2_CH2N	FGTR13A_RX_Q2_CH2N/ CL2	I, DIFF	Bank FGTR13A-Q2 channel2 High speed differential receiver negative.
D68	FGTL13A_RX_Q2_CH2P	FGTR13A_RX_Q2_CH2P/ CM1	I, DIFF	Bank FGTR13A-Q2 channel2 High speed differential receiver positive.
D72	FGTL13A_RX_Q2_CH3N	FGTR13A_RX_Q2_CH3N/ CP5	I, DIFF	Bank FGTR13A-Q2 channel3 High speed differential receiver negative.
D71	FGTL13A_RX_Q2_CH3P	FGTR13A_RX_Q2_CH3P/ CN4	I, DIFF	Bank FGTR13A-Q2 channel3 High speed differential receiver positive.
C63	FGTL13A_TX_Q2_CH0N	FGTR13A_TX_Q2_CH0N/ CF11	O, DIFF	Bank FGTR13A-Q2 channel0 High speed differential transmitter negative.
C62	FGTL13A_TX_Q2_CH0P	FGTR13A_TX_Q2_CH0P/ CE10	O, DIFF	Bank FGTR13A-Q2 channel0 High speed differential transmitter positive.
C66	FGTL13A_TX_Q2_CH1N	FGTR13A_TX_Q2_CH1N/ CG8	O, DIFF	Bank FGTR13A-Q2 channel1 High speed differential transmitter negative.
C65	FGTL13A_TX_Q2_CH1P	FGTR13A_TX_Q2_CH1P/ CH7	O, DIFF	Bank FGTR13A-Q2 channel1 High speed differential transmitter positive.
C69	FGTL13A_TX_Q2_CH2N	FGTR13A_TX_Q2_CH2N/ CK11	O, DIFF	Bank FGTR13A-Q2 channel2 High speed differential transmitter negative.
C68	FGTL13A_TX_Q2_CH2P	FGTR13A_TX_Q2_CH2P/ CJ10	O, DIFF	Bank FGTR13A-Q2 channel2 High speed differential transmitter positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C72	FGTL13A_TX_Q2_CH3N	FGTR13A_TX_Q2_CH3N/ CL8	O, DIFF	Bank FGTR13A-Q2 channel3 High speed differential transmitter negative.
C71	FGTL13A_TX_Q2_CH3P	FGTR13A_TX_Q2_CH3P/ CM7	O, DIFF	Bank FGTR13A-Q2 channel3 High speed differential transmitter positive.
D75	REFCLK_FGTL13A_Q2_ CH8N	REFCLK_FGTR13A_Q2_C H8N/ CU14	IO, DIFF	Bank FGTR13A-Q2 differential reference clock0 negative. Bidirectional Local reference clock, this clock can be used for 13A Bank Q2
D74	REFCLK_FGTL13A_Q2_ CH8P	REFCLK_FGTR13A_Q2_C H8P/ CR14	IO, DIFF	Bank FGTR13A-Q2 differential reference clock0 positive. Bidirectional Local reference clock, this clock can be used for 13A Bank Q2
C75	REFCLK_FGTL13A_Q2_ RX_CH5N	REFCLK_FGTR13A_Q2_RX _CH5N/ BW14	I, DIFF	Bank FGTR13A-Q2 differential reference clock1 negative. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2, Q3 Transceivers.
C74	REFCLK_FGTL13A_Q2_ RX_CH5P	REFCLK_FGTR13A_Q2_RX _CH5P/ BV13	I, DIFF	Bank FGTR13A-Q2 differential reference clock1 positive. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2, Q3 Transceivers.
BANK-FGT_13A Quad3 Channels				
B78	FGTL13A_RX_Q3_CH0N	FGTR13A_RX_Q3_CH0N/ CR2	I, DIFF	Bank FGTR13A-Q3 channel0 High speed differential receiver negative.
B77	FGTL13A_RX_Q3_CH0P	FGTR13A_RX_Q3_CH0P/ CT1	I, DIFF	Bank FGTR13A-Q3 channel0 High speed differential receiver positive.
B81	FGTL13A_RX_Q3_CH1N	FGTR13A_RX_Q3_CH1N/ CV5	O, DIFF	Bank FGTR13A-Q3 channel1 High speed differential receiver negative.
B80	FGTL13A_RX_Q3_CH1P	FGTR13A_RX_Q3_CH1P/ CU4	O, DIFF	Bank FGTR13A-Q3 channel1 High speed differential receiver positive.
B84	FGTL13A_RX_Q3_CH2N	FGTR13A_RX_Q3_CH2N/ CW2	I, DIFF	Bank FGTR13A-Q3 channel2 High speed differential receiver negative.
B83	FGTL13A_RX_Q3_CH2P	FGTR13A_RX_Q3_CH2P/ CY1	I, DIFF	Bank FGTR13A-Q3 channel2 High speed differential receiver positive.
B87	FGTL13A_RX_Q3_CH3N	FGTR13A_RX_Q3_CH3N/ DC2	O, DIFF	Bank FGTR13A-Q3 channel3 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B86	FGTL13A_RX_Q3_CH3P	FGTR13A_RX_Q3_CH3P/ DD1	O, DIFF	Bank FGTR13A-Q3 channel3 High speed differential receiver positive.
A78	FGTL13A_TX_Q3_CH0n	FGTR13A_TX_Q3_CH0N/ CP11	I, DIFF	Bank FGTR13A-Q3 channel0 High speed differential transmitter negative.
A77	FGTL13A_TX_Q3_CH0p	FGTR13A_TX_Q3_CH0P/ CN10	I, DIFF	Bank FGTR13A-Q3 channel0 High speed differential transmitter positive.
A81	FGTL13A_TX_Q3_CH1N	FGTR13A_TX_Q3_CH1N/ CR8	O, DIFF	Bank FGTR13A-Q3 channel1 High speed differential transmitter negative.
A80	FGTL13A_TX_Q3_CH1P	FGTR13A_TX_Q3_CH1P/ CT7	O, DIFF	Bank FGTR13A-Q3 channel1 High speed differential transmitter positive.
A84	FGTL13A_TX_Q3_CH2N	FGTR13A_TX_Q3_CH2N/ CV11	I, DIFF	Bank FGTR13A-Q3 channel2 High speed differential transmitter negative.
A83	FGTL13A_TX_Q3_CH2P	FGTR13A_TX_Q3_CH2P/ CU10	I, DIFF	Bank FGTR13A-Q3 channel2 High speed differential transmitter positive.
A87	FGTL13A_TX_Q3_CH3N	FGTR13A_TX_Q3_CH3N/ CW8	O, DIFF	Bank FGTR13A-Q3 channel3 High speed differential transmitter negative.
A86	FGTL13A_TX_Q3_CH3P	FGTR13A_TX_Q3_CH3P/ CY7	O, DIFF	Bank FGTR13A-Q3 channel3 High speed differential transmitter positive.
A90	REFCLK_FGTL13A_Q3_ RX_CH6N	REFCLK_FGTR13A_Q3_RX _CH6N/ CF13	I, DIFF	Bank FGTR13A-Q3 differential reference clock0 negative. Regional reference clock, this clock can be used for 13A Bank Q2 and Q3 Transceivers.
A89	REFCLK_FGTL13A_Q3_ RX_CH6P	REFCLK_FGTR13A_Q3_RX _CH6P/ CG14	I, DIFF	Bank FGTR13A-Q3 differential reference clock0 positive. Regional reference clock, this clock can be used for 13A Bank Q3 Transceivers.
B90	REFCLK_FGTL13A_Q3_ RX_CH7N	REFCLK_FGTR13A_Q3_RX _CH7N/ CN14	I, DIFF	Bank FGTR13A-Q3 differential reference clock1 negative. Regional reference clock, this clock can be used for 13A Bank Q3 Transceivers.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B89	REFCLK_FGTL13A_Q3_ RX_CH7P	REFCLK_FGTR13A_Q3_RX _CH7P/ CP13	I, DIFF	Bank FGTR13A-Q3 differential reference clock1 positive. Regional reference clock, this clock can be used for 13A Bank Q3 Transceivers.

For more details on FGTL 13C transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT_13C Quad0 Channels				
D3	FGTL13C_RX_Q0_CH0N	FGTR13C_RX_Q0_CH0N/ B11	I, DIFF	Bank FGTR13C-Q0 channel0 High speed differential receiver negative.
D2	FGTL13C_RX_Q0_CH0P	FGTR13C_RX_Q0_CH0P/ C10	I, DIFF	Bank FGTR13C-Q0 channel0 High speed differential receiver positive.
D6	FGTL13C_RX_Q0_CH1N	FGTR13C_RX_Q0_CH1N/ E8	I, DIFF	Bank FGTR13C-Q0 channel1 High speed differential receiver negative.
D5	FGTL13C_RX_Q0_CH1P	FGTR13C_RX_Q0_CH1P/ D7	I, DIFF	Bank FGTR13C-Q0 channel1 High speed differential receiver positive.
D9	FGTL13C_RX_Q0_CH2N	FGTR13C_RX_Q0_CH2N/ C4	I, DIFF	Bank FGTR13C-Q0 channel2 High speed differential receiver negative.
D8	FGTL13C_RX_Q0_CH2P	FGTR13C_RX_Q0_CH2P/ B3	I, DIFF	Bank FGTR13C-Q0 channel2 High speed differential receiver positive.
D12	FGTL13C_RX_Q0_CH3N	FGTR13C_RX_Q0_CH3N/ J8	I, DIFF	Bank FGTR13C-Q0 channel3 High speed differential receiver negative.
D11	FGTL13C_RX_Q0_CH3P	FGTR13C_RX_Q0_CH3P/ H7	I, DIFF	Bank FGTR13C-Q0 channel3 High speed differential receiver positive.
C3	FGTL13C_TX_Q0_CH0N	FGTR13C_TX_Q0_CH0N/ B17	O, DIFF	Bank FGTR13C-Q0 channel0 High speed differential transmitter negative.
C2	FGTL13C_TX_Q0_CH0P	FGTR13C_TX_Q0_CH0P/ C16	O, DIFF	Bank FGTR13C-Q0 channel0 High speed differential transmitter positive.
C6	FGTL13C_TX_Q0_CH1N	FGTR13C_TX_Q0_CH1N/ F17	O, DIFF	Bank FGTR13C-Q0 channel1 High speed differential transmitter negative.
C5	FGTL13C_TX_Q0_CH1P	FGTR13C_TX_Q0_CH1P/ G16	O, DIFF	Bank FGTR13C-Q0 channel1 High speed differential transmitter positive.
C9	FGTL13C_TX_Q0_CH2N	FGTR13C_TX_Q0_CH2N/ E14	O, DIFF	Bank FGTR13C-Q0 channel2 High speed differential transmitter negative.
C8	FGTL13C_TX_Q0_CH2P	FGTR13C_TX_Q0_CH2P/ D13	O, DIFF	Bank FGTR13C-Q0 channel2 High speed differential transmitter positive.
C12	FGTL13C_TX_Q0_CH3N	FGTR13C_TX_Q0_CH3N/ J14	O, DIFF	Bank FGTR13C-Q0 channel3 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C11	FGTL13C_TX_Q0_CH3P	FGTR13C_TX_Q0_CH3P/ H13	O, DIFF	Bank FGTR13C-Q0 channel3 High speed differential transmitter positive.
C15	REFCLK_FGTL13C_Q0_ RX_CH0N	REFCLK_FGTR13C_Q0_RX _CH0N/ AD17	I, DIFF	Bank FGTR13C-Q0 differential reference clock0 negative. Regional reference clock, this clock can be used for 13C Bank Q0 Transceivers.
C14	REFCLK_FGTL13C_Q0_ RX_CH0P	REFCLK_FGTR13C_Q0_RX _CH0P/ AF17	I, DIFF	Bank FGTR13C-Q0 differential reference clock0 positive. Regional reference clock, this clock can be used for 13C Bank Q0 Transceivers
D15	REFCLK_FGTL13C_Q0_ RX_CH1N	REFCLK_FGTL13C_Q0_RX _CH1N/ AA16	I, DIFF	Bank FGTR13C-Q0 differential reference clock1 negative. Regional reference clock, this clock can be used for 13C Bank Q0 Transceivers.
D14	REFCLK_FGTL13C_Q0_ RX_CH1P	REFCLK_FGTR13C_Q0_RX _CH1P/ W16	I, DIFF	Bank FGTR13C-Q0 differential reference clock1 positive. Regional reference clock, this clock can be used for 13C Bank Q0 Transceivers.
BANK-FGT_13C Quad1 Channels				
B18	FGTL13C_RX_Q1_CH0N	FGTR13C_RX_Q1_CH0N/ F5	I, DIFF	Bank FGTR13C-Q1 channel0 High speed differential receiver negative.
B17	FGTL13C_RX_Q1_CH0P	FGTR13C_RX_Q1_CH0P/ G4	I, DIFF	Bank FGTR13C-Q1 channel0 High speed differential receiver positive.
B21	FGTL13C_RX_Q1_CH1N	FGTR13C_RX_Q1_CH1N/ K5	O, DIFF	Bank FGTR13C-Q1 channel1 High speed differential receiver negative.
B20	FGTL13C_RX_Q1_CH1P	FGTR13C_RX_Q1_CH1P/ L4	O, DIFF	Bank FGTR13C-Q1 channel1 High speed differential receiver positive.
B24	FGTL13C_RX_Q1_CH2N	FGTR13C_RX_Q1_CH2N/ J2	I, DIFF	Bank FGTR13C-Q1 channel2 High speed differential receiver negative.
B23	FGTL13C_RX_Q1_CH2P	FGTR13C_RX_Q1_CH2P/ H1	I, DIFF	Bank FGTR13C-Q1 channel2 High speed differential receiver positive.
B27	FGTL13C_RX_Q1_CH3N	FGTR13C_RX_Q1_CH3N/ P5	I, DIFF	Bank FGTR13C-Q1 channel3 High speed differential receiver negative.
B26	FGTL13C_RX_Q1_CH3P	FGTR13C_RX_Q1_CH3P/ R4	I, DIFF	Bank FGTR13C-Q1 channel3 High speed differential receiver positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A18	FGTL13C_TX_Q1_CH0N	FGTR13C_TX_Q1_CH0N/ F11	O, DIFF	Bank FGTR13C-Q1 channel0 High speed differential transmitter negative.
A17	FGTL13C_TX_Q1_CH0P	FGTR13C_TX_Q1_CH0P/ G10	O, DIFF	Bank FGTR13C-Q1 channel0 High speed differential transmitter positive.
A21	FGTL13C_TX_Q1_CH1N	FGTR13C_TX_Q1_CH1N/ K11	O, DIFF	Bank FGTR13C-Q1 channel1 High speed differential transmitter negative.
A20	FGTL13C_TX_Q1_CH1P	FGTR13C_TX_Q1_CH1P/ L10	O, DIFF	Bank FGTR13C-Q1 channel1 High speed differential transmitter positive.
A24	FGTL13C_TX_Q1_CH2N	FGTR13C_TX_Q1_CH2N/ N8	O, DIFF	Bank FGTR13C-Q1 channel2 High speed differential transmitter negative.
A23	FGTL13C_TX_Q1_CH2P	FGTR13C_TX_Q1_CH2P/ M7	O, DIFF	Bank FGTR13C-Q1 channel2 High speed differential transmitter positive.
A27	FGTL13C_TX_Q1_CH3N	FGTR13C_TX_Q1_CH3N/ P11	O, DIFF	Bank FGTR13C-Q1 channel3 High speed differential transmitter negative.
A26	FGTL13C_TX_Q1_CH3P	FGTR13C_TX_Q1_CH3P/ R10	O, DIFF	Bank FGTR13C-Q1 channel3 High speed differential transmitter positive.
A30	REFCLK_FGTL13C_Q1_ RX_CH2N	REFCLK_FGTR13C_Q1_RX _CH2N/ N14	I, DIFF	Bank FGTR13C-Q1 differential reference clock0 negative. Global reference clock, this clock can be used for 13C Bank Q0, Q1, Q2, Q3 Transceivers.
A29	REFCLK_FGTL13C_Q1_ RX_CH2P	REFCLK_FGTR13C_Q1_RX _CH2P/ P13	I, DIFF	Bank FGTR13C-Q1 differential reference clock0 positive. Global reference clock, this clock can be used for 13C Bank Q0, Q1, Q2, Q3 Transceivers.
B30	REFCLK_FGTL13C_Q1_ RX_CH3N	REFCLK_FGTR13C_Q1_RX _CH3N/ AM11	I, DIFF	Bank FGTR13C-Q1 differential reference clock1 negative. Global reference clock, this clock can be used for 13C Bank Q0, Q1, Q2, Q3 Transceivers.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B29	REFCLK_FGTL13C_Q1_ RX_CH3P	REFCLK_FGTR13C_Q1_RX _CH3P/ AL12	I, DIFF	Bank FGTR13C-Q1 differential reference clock1 positive. Global reference clock, this clock can be used for 13C Bank Q0, Q1, Q2, Q3 Transceivers.
BANK-FGT_13C Quad2 Channels				
D18	FGTL13C_RX_Q2_CH0N	FGTR13C_RX_Q2_CH0N/ N2	I, DIFF	Bank FGTR13C-Q2 channel0 High speed differential receiver negative.
D17	FGTL13C_RX_Q2_CH0P	FGTR13C_RX_Q2_CH0P/ M1	I, DIFF	Bank FGTR13C-Q2 channel0 High speed differential receiver positive.
D21	FGTL13C_RX_Q2_CH1N	FGTR13C_RX_Q2_CH1N/ V5	I, DIFF	Bank FGTR13C-Q2 channel1 High speed differential receiver negative.
D20	FGTL13C_RX_Q2_CH1P	FGTR13C_RX_Q2_CH1P/ W4	I, DIFF	Bank FGTR13C-Q2 channel1 High speed differential receiver positive.
D24	FGTL13C_RX_Q2_CH2N	FGTR13C_RX_Q2_CH2N/ U2	I, DIFF	Bank FGTR13C-Q2 channel2 High speed differential receiver negative.
D23	FGTL13C_RX_Q2_CH2P	FGTR13C_RX_Q2_CH2P/ T1	I, DIFF	Bank FGTR13C-Q2 channel2 High speed differential receiver positive.
D27	FGTL13C_RX_Q2_CH3N	FGTR13C_RX_Q2_CH3N/ AB5	I, DIFF	Bank FGTR13C-Q2 channel3 High speed differential receiver negative.
D26	FGTL13C_RX_Q2_CH3P	FGTR13C_RX_Q2_CH3P/ AC4	I, DIFF	Bank FGTR13C-Q2 channel3 High speed differential receiver positive.
C18	FGTL13C_TX_Q2_CH0N	FGTR13C_TX_Q2_CH0N/ U8	I, DIFF	Bank FGTR13C-Q2 channel0 High speed differential transmitter negative.
C17	FGTL13C_TX_Q2_CH0P	FGTR13C_TX_Q2_CH0P/ T7	I, DIFF	Bank FGTR13C-Q2 channel0 High speed differential transmitter positive.
C21	FGTL13C_TX_Q2_CH1N	FGTR13C_TX_Q2_CH1N/ V11	O, DIFF	Bank FGTR13C-Q2 channel1 High speed differential transmitter negative.
C20	FGTL13C_TX_Q2_CH1P	FGTR13C_TX_Q2_CH1P/ W10	O, DIFF	Bank FGTR13C-Q2 channel1 High speed differential transmitter positive.
C24	FGTL13C_TX_Q2_CH2N	FGTR13C_TX_Q2_CH2N/ AA8	I, DIFF	Bank FGTR13C-Q2 channel2 High speed differential transmitter negative.
C23	FGTL13C_TX_Q2_CH2P	FGTR13C_TX_Q2_CH2P/ Y7	I, DIFF	Bank FGTR13C-Q2 channel2 High speed differential transmitter positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C27	FGTL13C_TX_Q2_CH3N	FGTR13C_TX_Q2_CH3N/ AB11	O, DIFF	Bank FGTR13C-Q2 channel3 High speed differential transmitter negative.
C26	FGTL13C_TX_Q2_CH3P	FGTR13C_TX_Q2_CH3P/ AC10	O, DIFF	Bank FGTR13C-Q2 channel3 High speed differential transmitter positive.
D30	REFCLK_FGTL13C_Q2_ CH8N	REFCLK_FGTR13C_Q2_CH 8N/ AB13	IO, DIFF	Bank FGTR13C-Q2 differential reference clock negative. Bidirectional Local reference clock, this clock can be used for 13C Bank Q2
D29	REFCLK_FGTL13C_Q2_ CH8P	REFCLK_FGTR13C_Q2_CH 8P/ AA14	IO, DIFF	Bank FGTR13C-Q2 differential reference clock positive. Bidirectional Local reference clock, this clock can be used for 13C Bank Q2
C30	REFCLK_FGTL13C_Q2_ RX_CH5N	REFCLK_FGTR13C_Q2_RX _CH5N/ AU12	I, DIFF	Bank FGTR13C-Q2 differential reference clock negative. Global reference clock, this clock can be used for 13C Bank Q0, Q1, Q2, Q3 Transceivers.
C29	REFCLK_FGTL13C_Q2_ RX_CH5P	REFCLK_FGTR13C_Q2_RX _CH5P/ AV11	I, DIFF	Bank FGTR13C-Q2 differential reference clock positive. Global reference clock, this clock can be used for 13C Bank Q0, Q1, Q2, Q3 Transceivers.
BANK-FGT_13C Quad3 Channels				
B33	FGTL13C_RX_Q3_CH0N	FGTR13C_RX_Q3_CH0N/ AA2	I, DIFF	Bank FGTR13C-Q3 channel0 High speed differential receiver negative.
B32	FGTL13C_RX_Q3_CH0P	FGTR13C_RX_Q3_CH0P/ Y1	I, DIFF	Bank FGTR13C-Q3 channel0 High speed differential receiver positive.
B36	FGTL13C_RX_Q3_CH1N	FGTR13C_RX_Q3_CH1N/ AF5	I, DIFF	Bank FGTR13C-Q3 channel1 High speed differential receiver negative.
B35	FGTL13C_RX_Q3_CH1P	FGTR13C_RX_Q3_CH1P/ AG4	I, DIFF	Bank FGTR13C-Q3 channel1 High speed differential receiver positive.
B39	FGTL13C_RX_Q3_CH2N	FGTR13C_RX_Q3_CH2N/ AE2	I, DIFF	Bank FGTR13C-Q3 channel2 High speed differential receiver negative.
B38	FGTL13C_RX_Q3_CH2P	FGTR13C_RX_Q3_CH2P/ AD1	I, DIFF	Bank FGTR13C-Q3 channel2 High speed differential receiver positive.
B42	FGTL13C_RX_Q3_CH3N	FGTR13C_RX_Q3_CH3N/ AJ2	I, DIFF	Bank FGTR13C-Q3 channel3 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B41	FGTL13C_RX_Q3_CH3P	FGTR13C_RX_Q3_CH3P/ AH1	I, DIFF	Bank FGTR13C-Q3 channel3 High speed differential receiver positive.
A33	FGTL13C_TX_Q3_CH0N	FGTR13C_TX_Q3_CH0N/ AE8	O, DIFF	Bank FGTR13C-Q3 channel0 High speed differential transmitter negative.
A32	FGTL13C_TX_Q3_CH0P	FGTR13C_TX_Q3_CH0P/ AD7	O, DIFF	Bank FGTR13C-Q3 channel0 High speed differential transmitter positive.
A36	FGTL13C_TX_Q3_CH1N	FGTR13C_TX_Q3_CH1N/ AF11	O, DIFF	Bank FGTR13C-Q3 channel1 High speed differential transmitter negative.
A35	FGTL13C_TX_Q3_CH1P	FGTR13C_TX_Q3_CH1P/ AG10	O, DIFF	Bank FGTR13C-Q3 channel1 High speed differential transmitter positive.
A39	FGTL13C_TX_Q3_CH2N	FGTR13C_TX_Q3_CH2N/ AJ8	O, DIFF	Bank FGTR13C-Q3 channel2 High speed differential transmitter negative.
A38	FGTL13C_TX_Q3_CH2P	FGTR13C_TX_Q3_CH2P/ AH7	O, DIFF	Bank FGTR13C-Q3 channel2 High speed differential transmitter positive.
A42	FGTL13C_TX_Q3_CH3N	FGTR13C_TX_Q3_CH3N/ AN8	O, DIFF	Bank FGTR13C-Q3 channel3 High speed differential transmitter negative.
A41	FGTL13C_TX_Q3_CH3P	FGTR13C_TX_Q3_CH3P/ AM7	O, DIFF	Bank FGTR13C-Q3 channel3 High speed differential transmitter positive.
A45	REFCLK_FGTL13C_Q3_ RX_CH6N	REFCLK_FGTR13C_Q3_RX _CH6N/ AE14	I, DIFF	Bank FGTR13C-Q3 differential reference clock0 negative. Regional reference clock, this clock can be used for 13C Bank Q2 and Q3 Transceivers.
A44	REFCLK_FGTL13C_Q3_ RX_CH6P	REFCLK_FGTR13C_Q3_RX _CH6P/ AC14	I, DIFF	Bank FGTR13C-Q3 differential reference clock0 positive. Regional reference clock, this clock can be used for 13C Bank Q2 and Q3 Transceivers.
B45	REFCLK_FGTL13C_Q3_ RX_CH7N	REFCLK_FGTR13C_Q3_RX _CH7N/ AG14	I, DIFF	Bank FGTR13C-Q3 differential reference clock1 negative. Regional reference clock, this clock can be used for 13C Bank Q2 and Q3 Transceivers.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B44	REFCLK_FGTL13C_Q3_ RX_CH7P	REFCLK_FGTR13C_Q3_RX _CH7P/ AF13	I, DIFF	Bank FGTL 13C-Q3 differential reference clock1 positive. Regional reference clock, this clock can be used for 13C Bank Q2 and Q3 Transceivers.

For more details on FHT 13A transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT_13A Channels				
B48	FHTR13A_RX_CH0N	FHTR13A_RX_CH0N/ DD9	I, DIFF	Bank FHTR13A channel0 High speed differential receiver negative.
B47	FHTR13A_RX_CH0P	FHTR13A_RX_CH0P/ DC10	I, DIFF	Bank FHTR13A channel0 High speed differential receiver positive.
B51	FHTR13A_RX_CH1N	FHTR13A_RX_CH1N/ DE12	I, DIFF	Bank FHTR13A channel1 High speed differential receiver negative.
B50	FHTR13A_RX_CH1P	FHTR13A_RX_CH1P/ DD13	I, DIFF	Bank FHTR13A channel1 High speed differential receiver positive.
B54	FHTR13A_RX_CH2N	FHTR13A_RX_CH2N/ DH13	I, DIFF	Bank FHTR13A channel2 High speed differential receiver negative.
B53	FHTR13A_RX_CH2P	FHTR13A_RX_CH2P/ DJ12	I, DIFF	Bank FHTR13A channel2 High speed differential receiver positive.
B57	FHTR13A_RX_CH3N	FHTR13A_RX_CH3N/ DJ16	I, DIFF	Bank FHTR13A channel3 High speed differential receiver negative.
B56	FHTR13A_RX_CH3P	FHTR13A_RX_CH3P/ DK15	I, DIFF	Bank FHTR13A channel3 High speed differential receiver positive.
A48	FHTR13A_TX_CH0N	FHTR13A_TX_CH0N/ DG6	O, DIFF	Bank FHTR13A channel0 High speed differential transmitter negative.
A47	FHTR13A_TX_CH0P	FHTR13A_TX_CH0P/ DF7	O, DIFF	Bank FHTR13A channel0 High speed differential transmitter positive.
A51	FHTR13A_TX_CH1N	FHTR13A_TX_CH1N/ DH9	O, DIFF	Bank FHTR13A channel1 High speed differential transmitter negative.
A50	FHTR13A_TX_CH1P	FHTR13A_TX_CH1P/ DG10	O, DIFF	Bank FHTR13A channel1 High speed differential transmitter positive.
A54	FHTR13A_TX_CH2N	FHTR13A_TX_CH2N/ DL10	O, DIFF	Bank FHTR13A channel2 High speed differential transmitter negative.
A53	FHTR13A_TX_CH2P	FHTR13A_TX_CH2P/ DM9	O, DIFF	Bank FHTR13A channel2 High speed differential transmitter positive.
A57	FHTR13A_TX_CH3N	FHTR13A_TX_CH3N/ DM13	O, DIFF	Bank FHTR13A channel3 High speed differential transmitter negative.
A56	FHTR13A_TX_CH3P	FHTR13A_TX_CH3P/ DN12	O, DIFF	Bank FHTR13A channel3 High speed differential transmitter positive.
A60	REFCLK_FHTR13A_CH0N	REFCLK_FHTR13A_CH0N/ DB15	I, DIFF	Bank FHTR13A differential reference Clock0 negative.
A59	REFCLK_FHTR13A_CH0P	REFCLK_FHTR13A_CH0P/ DA16	I, DIFF	Bank FHTR13A differential reference Clock0 positive.
B60	REFCLK_FHTR13A_CH1N	REFCLK_FHTR13A_CH1N/ DE16	I, DIFF	Bank FHTR13A differential reference Clock1 negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B59	REFCLK_FHTR13A_CH1P	REFCLK_FHTR13A_CH1P/ DF15	I, DIFF	Bank FHTR13A differential reference Clock1 positive.

For more details on FHT 13C transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT13C Channels				
D33	FHTR13C_RX_CH0N	FHTR13C_RX_CH0N/ AR6	I, DIFF	Bank FHTR13C channel0 High speed differential receiver negative.
D32	FHTR13C_RX_CH0P	FHTR13C_RX_CH0P/ AT5	I, DIFF	Bank FHTR13C channel0 High speed differential receiver positive.
D36	FHTR13C_RX_CH1N	FHTR13C_RX_CH1N/ AW6	I, DIFF	Bank FHTR13C channel1 High speed differential receiver negative.
D35	FHTR13C_RX_CH1P	FHTR13C_RX_CH1P/ AY5	I, DIFF	Bank FHTR13C channel1 High speed differential receiver positive.
D39	FHTR13C_RX_CH2N	FHTR13C_RX_CH2N/ BD5	I, DIFF	Bank FHTR13C channel2 High speed differential receiver negative.
D38	FHTR13C_RX_CH2P	FHTR13C_RX_CH2P/ BC6	I, DIFF	Bank FHTR13C channel2 High speed differential receiver positive.
D42	FHTR13C_RX_CH3N	FHTR13C_RX_CH3N/ BH5	I, DIFF	Bank FHTR13C channel3 High speed differential receiver negative.
D41	FHTR13C_RX_CH3P	FHTR13C_RX_CH3P/ BG6	I, DIFF	Bank FHTR13C channel3 High speed differential receiver positive.
C33	FHTR13C_TX_CH0N	FHTR13C_TX_CH0N/ AP3	O, DIFF	Bank FHTR13C channel0 High speed differential transmitter negative.
C32	FHTR13C_TX_CH0P	FHTR13C_TX_CH0P/ AN2	O, DIFF	Bank FHTR13C channel0 High speed differential transmitter positive.
C36	FHTR13C_TX_CH1N	FHTR13C_TX_CH1N/ AV3	O, DIFF	Bank FHTR13C channel1 High speed differential transmitter negative.
C35	FHTR13C_TX_CH1P	FHTR13C_TX_CH1P/ AU2	O, DIFF	Bank FHTR13C channel1 High speed differential transmitter positive.
C39	FHTR13C_TX_CH2N	FHTR13C_TX_CH2N/ BA2	O, DIFF	Bank FHTR13C channel2 High speed differential transmitter negative.
C38	FHTR13C_TX_CH2P	FHTR13C_TX_CH2P/ BB3	O, DIFF	Bank FHTR13C channel2 High speed differential transmitter positive.
C42	FHTR13C_TX_CH3N	FHTR13C_TX_CH3N/ BE2	O, DIFF	Bank FHTR13C channel3 High speed differential transmitter negative.
C41	FHTR13C_TX_CH3P	FHTR13C_TX_CH3P/ BF3	O, DIFF	Bank FHTR13C channel3 High speed differential transmitter positive.
C45	REFCLK_FHTR13C_CH0N	REFCLK_FHTR13C_CH0N/ BC10	I, DIFF	Bank FHTR13C differential reference Clock0 negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C44	REFCLK_FHTR13C_CH0P	REFCLK_FHTR13C_CH0P/ BB11	I, DIFF	Bank FHTR13C differential reference Clock0 positive.
D45	REFCLK_FHTR13C_CH1N	REFCLK_FHTR13C_CH1N/ BE8	I, DIFF	Bank FHTR13C differential reference Clock1 negative.
D44	REFCLK_FHTR13C_CH1P	REFCLK_FHTR13C_CH1P/ BF9	I, DIFF	Bank FHTR13C differential reference Clock1 positive.

2.8.2 Power, Control & Reset Input

The Intel Agilex 7 SoC and FPGA SOM works with 12V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. In Board-to-Board Connector1, Ground pins are also distributed throughout the connector for better performance. In Board-to-Board Connector2, there are also Hardware Reset signal for resetting the CPU from Carrier Board and SOM Power Enable Signal for turning ON/OFF the SOM Power from the Carrier Board. Also, 1.8V RTC Power & 5V standby powers are connected to Board-to-Board Connector2.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-3 Pin No	B2B Connector3 Signal Name	Pin Name	Signal Type/ Termination	Description
A1, A10, A100, A13, A16, A19, A22, A25, A28, A31, A34, A37, A4, A40, A43, A46, A49, A52, A55, A58, A61, A64, A67, A7, A70, A73, A76, A79, A82, A85, A88, A91, A94, A97, B1, B10, B100, B13, B16, B19, B22, B25, B28, B31, B34, B37, B4, B40, B43, B46, B49, B52, B55, B58, B61, B64, B67, B7, B70, B73, B76, B79, B82, B85, B88, B91, B94, B97, C1, C10, C100, C13, C16, C19, C22, C25, C28, C31, C34, C37, C4, C40, C43, C46, C49, C52, C55, C58, C61, C64, C67, C7, C70, C73, C76, C79, C82, C85, C88, C91, C94, C97, D1, D10, D100, D13, D16, D19, D22, D25, D28, D31, D34, D37, D4, D40, D43, D46, D49, D52, D55, D58, D61, D64, D67, D7, D70, D73, D76, D79, D82, D85, D88, D91, D94, D97	GND	NA	Power	Ground.

2.9 Intel Agilex 7 SoC and FPGA HPS Pin Multiplexing

The Intel Agilex 7 SoC and FPGA HPS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of Intel Agilex 7 SoC HPS IO pins can be configured as GPIOs if required.

The below table provides the details of HPS pin connections on Intel Agilex 7 SoC and FPGA with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring HPS I/O configuration in Quartus Tool.

To know the complete available alternate functions, refer the HPS I/O configuration in the latest Quartus Tool

Table 13: HPS IOMUX on Intel Agilex 7 SoC and FPGA SOM

Interface/ Function	B2B Connector Pin Number	Intel Agilex 7 SoC & FPGA Pin Name	GPIO	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
On SOM Features from Intel Agilex 7 SoC HPS												
eMMC FLASH	NA	HPS_IOB_13	GPIO1_IO12	EMAC2_TX_CLK	SDMMC_DATA0	Trace_D10	NAND_ALE	I2C1_SDA				GPIO1_IO12
	NA	HPS_IOB_14	GPIO1_IO13	EMAC2_TX_CTL	SDMMC_CMD	Trace_D9	NAND_RB	I2C1_SCL				GPIO1_IO13
	NA	HPS_IOB_15	GPIO1_IO14	EMAC2_RX_CLK	SDMMC_CCLK	Trace_D8	NAND_CE_N		UART1_TX			GPIO1_IO14
	NA	HPS_IOB_16	GPIO1_IO15	EMAC2_RX_CTL	SDMMC_DATA1	Trace_D7			UART1_RX			GPIO1_IO15
	NA	HPS_IOB_17	GPIO1_IO16	EMAC2_TXD0	SDMMC_DATA2	Trace_D6	NAND_ADQ8		UART1_CTS_N			GPIO1_IO16
	NA	HPS_IOB_18	GPIO1_IO17	EMAC2_TXD1	SDMMC_DATA3	Trace_D5	NAND_ADQ9		UART1_RTS_N		SPIM0_SS1_N	GPIO1_IO17
	NA	HPS_IOB_19	GPIO1_IO18	EMAC2_RXD0	SDMMC_DATA4	Trace_D4	NAND_ADQ10	I2C_EMAC1_SDA	MDIO1_MDIO		SPIM0_MISO	GPIO1_IO18
	NA	HPS_IOB_20	GPIO1_IO19	EMAC2_RXD1	SDMMC_DATA5	Trace_CLK	NAND_ADQ11	I2C_EMAC1_SCL	MDIO1_MDC		SPIM0_SS0_N	GPIO1_IO19
	NA	HPS_IOB_21	GPIO1_IO20	EMAC2_TXD2	SDMMC_DATA6	Trace_D0	NAND_ADQ12	I2C_EMAC2_SDA		SPIS1_CLK	SPIM0_CLK	GPIO1_IO20
	NA	HPS_IOB_22	GPIO1_IO21	EMAC2_TXD3	SDMMC_DATA7	Trace_D1	NAND_ADQ13	I2C_EMAC2_SCL		SPIS1_MOSI	SPIM0_MOSI	GPIO1_IO21
	NA	HPS_IOB_23	GPIO1_IO22	EMAC2_RXD2	SDMMC_PWR_EN	Trace_D2	NAND_ADQ14	I2C_EMAC0_SDA	MDIO0_MDIO	SPIS1_SS0_N	SPIM0_MISO	GPIO1_IO22
ENET	NA	HPS_IOB_1	GPIO1_IO0	EMAC1_TX_CLK		Trace_D10	NAND_ADQ0		UART0_CTS_N		SPIM1_CLK	GPIO1_IO0
	NA	HPS_IOB_2	GPIO1_IO1	EMAC1_TX_CTL		Trace_D9	NAND_ADQ1		UART0_RTS_N		SPIM1_MOSI	GPIO1_IO1
	NA	HPS_IOB_3	GPIO1_IO2	EMAC1_RX_CLK		Trace_D8	NAND_WE_N	I2C0_SDA	UART0_TX		SPIM1_MISO	GPIO1_IO2
	NA	HPS_IOB_4	GPIO1_IO3	EMAC1_RX_CTL		Trace_D7	NAND_RE_N	I2C0_SCL	UART0_RX		SPIM1_SS0_N	GPIO1_IO3
	NA	HPS_IOB_5	GPIO1_IO4	EMAC1_TXD0		Trace_D6	NAND_WP_N		UART1_CTS_N	SPIS1_CLK	SPIM1_SS1_N	GPIO1_IO4
	NA	HPS_IOB_6	GPIO1_IO5	EMAC1_TXD1		Trace_D5	NAND_ADQ2		UART1_RTS_N	SPIS1_MOSI		GPIO1_IO5
	NA	HPS_IOB_7	GPIO1_IO6	EMAC1_RXD0		Trace_D4	NAND_ADQ3	I2C1_SDA	UART1_TX	SPIS1_SS0_N		GPIO1_IO6
	NA	HPS_IOB_8	GPIO1_IO7	EMAC1_RXD1		Trace_D15	NAND_CLE	I2C1_SCL	UART1_RX	SPIS1_MISO		GPIO1_IO7
	NA	HPS_IOB_9	GPIO1_IO8	EMAC1_TXD2		Trace_D14	NAND_ADQ4	I2C_EMAC2_SDA	MDIO2_MDIO	SPIS0_CLK	JTAG_TCK	GPIO1_IO8
	NA	HPS_IOB_10	GPIO1_IO9	EMAC1_TXD3		Trace_D13	NAND_ADQ5	I2C_EMAC2_SCL	MDIO2_MDC	SPIS0_MOSI	JTAG_TMS	GPIO1_IO9
	NA	HPS_IOB_11	GPIO1_IO10	EMAC1_RXD2		Trace_D12	NAND_ADQ6	I2C_EMAC0_SDA	MDIO0_MDIO	SPIS0_SS0_N	JTAG_TDO	GPIO1_IO10
	NA	HPS_IOB_12	GPIO1_IO11	EMAC1_RXD3		Trace_D11	NAND_ADQ7	I2C_EMAC0_SCL	MDIO0_MDC	SPIS0_MISO	JTAG_TDI	GPIO1_IO11
	NA	HPS_IOA_9	GPIO0_IO8	SDMMC_DATA6	USB0_DATA4	Trace_D14	NAND_ADQ4	I2C_EMAC1_SDA	MDIO1_MDIO	SPIS1_CLK	SPIM1_CLK	GPIO0_IO8
	NA	HPS_IOA_10	GPIO0_IO9	SDMMC_DATA7	USB0_DATA5	Trace_D13	NAND_ADQ5	I2C_EMAC1_SCL	MDIO1_MDC	SPIS1_MOSI	SPIM1_MOSI	GPIO0_IO9
	NA	HPS_IOA_12	GPIO0_IO11		USB0_DATA7	Trace_D11	NAND_ADQ7	I2C_EMAC0_SCL	MDIO0_MDC	SPIS1_MISO	SPIM1_SS0_N	GPIO0_IO11
USB2.0	NA	HPS_IOA_13	GPIO0_IO12	EMAC0_TX_CLK	USB1_CLK	Trace_D10	NAND_ALE					GPIO0_IO12
	NA	HPS_IOA_14	GPIO0_IO13	EMAC0_TX_CTL	USB1_STP	Trace_D9	NAND_RB					GPIO0_IO13
	NA	HPS_IOA_15	GPIO0_IO14	EMAC0_RX_CLK	USB1_DIR	Trace_D8	NAND_CE_N					GPIO0_IO14
	NA	HPS_IOA_16	GPIO0_IO15	EMAC0_RX_CTL	USB1_DATA0	Trace_D7						GPIO0_IO15
	NA	HPS_IOA_17	GPIO0_IO16	EMAC0_TXD0	USB1_DATA1	Trace_D6	NAND_ADQ8					GPIO0_IO16
	NA	HPS_IOA_18	GPIO0_IO17	EMAC0_TXD1	USB1_NXT	Trace_D5	NAND_ADQ9					GPIO0_IO17
	NA	HPS_IOA_19	GPIO0_IO18	EMAC0_RXD0	USB1_DATA2	Trace_D4	NAND_ADQ10					GPIO0_IO18
	NA	HPS_IOA_20	GPIO0_IO19	EMAC0_RXD1	USB1_DATA3	Trace_CLK	NAND_ADQ11				SPIM1_SS1_N	GPIO0_IO19
	NA	HPS_IOA_21	GPIO0_IO20	EMAC0_TXD2	USB1_DATA4	Trace_D0	NAND_ADQ12	I2C1_SDA	UART0_CTS_N	SPIS0_CLK	SPIM1_CLK	GPIO0_IO20
	NA	HPS_IOA_22	GPIO0_IO21	EMAC0_TXD3	USB1_DATA5	Trace_D1	NAND_ADQ13	I2C1_SCL	UART0_RTS_N	SPIS0_MOSI	SPIM1_MOSI	GPIO0_IO21
	NA	HPS_IOA_23	GPIO0_IO22	EMAC0_RXD2	USB1_DATA6	Trace_D2	NAND_ADQ14	I2C0_SDA	UART0_TX	SPIS0_SS0_N	SPIM1_MISO	GPIO0_IO22
	NA	HPS_IOA_24	GPIO0_IO23	EMAC0_RXD3	USB1_DATA7	Trace_D3	NAND_ADQ15	I2C0_SCL	UART0_RX	SPIS0_MISO	SPIM1_SS0_N	GPIO0_IO23
	NA	HPS_IOA_11	GPIO0_IO10	SDMMC_PWR_EN	USB0_DATA6	Trace_D12	NAND_ADQ6	I2C_EMAC0_SDA	MDIO0_MDIO	SPIS1_SS0_N	SPIM1_MISO	GPIO0_IO10

Interface/ Function	B2B Connector Pin Number	Intel Agilex 7 SoC & FPGA Pin Name	GPIO	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
Board-to-Board Connector2 Features from Agilex 7 HPS												
UART0	B29	HPS_IOA_1	GPIO0_IO0	SDMMC_CCLK	USB0_CLK	Trace_D10	NAND_ADQ0		UART0_CTS_N	SPIS0_CLK	SPIM0_SS1_N	GPIO0_IO0
	B30	HPS_IOA_2	GPIO0_IO1	SDMMC_CMD	USB0_STP	Trace_D9	NAND_ADQ1		UART0_RTS_N	SPIS0_MOSI	SPIM1_SS1_N	GPIO0_IO1
	B27	HPS_IOA_3	GPIO0_IO2	SDMMC_DATA0	USB0_DIR	Trace_D8	NAND_WE_N	I2C1_SDA	UART0_TX	SPIS0_SS0_N		GPIO0_IO2
	B28	HPS_IOA_4	GPIO0_IO3	SDMMC_DATA1	USB0_DATA0	Trace_D7	NAND_RE_N	I2C1_SCL	UART0_RX	SPIS0_MISO		GPIO0_IO3
I2C	A27	HPS_IOA_5	GPIO0_IO4	SDMMC_DATA2	USB0_DATA1	Trace_D6	NAND_WP_N	I2C0_SDA	UART1_CTS_N		SPIM0_CLK	GPIO0_IO4
	A26	HPS_IOA_6	GPIO0_IO5	SDMMC_DATA3	USB0_NXT	Trace_D5	NAND_ADQ2	I2C0_SCL	UART1_RTS_N		SPIM0_MOSI	GPIO0_IO5
Debug UART	A30	HPS_IOB_7	GPIO0_IO6	SDMMC_DATA4	USB0_DATA2	Trace_D4	NAND_ADQ3	I2C_EMAC2_SDA	UART1_TX	MDIO2_MDIO	SPIM0_MISO	GPIO0_IO6
	A31	HPS_IOB_8	GPIO0_IO7	SDMMC_DATA5	USB0_DATA3	Trace_D15	NAND_CLE	I2C_EMAC2_SCL	UART1_RX	MDIO2_MDC	SPIM0_SS0_N	GPIO0_IO7

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Intel Agilex 7 SoC and FPGA SOM technical specifications with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Intel Agilex 7 SoC and FPGA SOM.

Table 14: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75	12V	12.25V	±50mV
2	VRTC_1V8	0V	1.8V	1.8V	±20mV

[1] Intel Agilex 7 SoC and FPGA *SOM is designed to work with VCC_12V input power rail from Board-to-Board Connector2.*

3.1.2 Power Input Sequencing

The Intel Agilex 7 SoC and FPGA SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_1V8 must come up at the same time or before VCC_12V comes up.
- SOMPWR_EN signal from Board-to-Board Connector2 must be high at the same time or after VCC_12V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board-to-Board Connector2 must be low at the same time or before VCC_12V goes down.
- VCC_12V must go down at the same time or before VRTC_1V8 goes down.

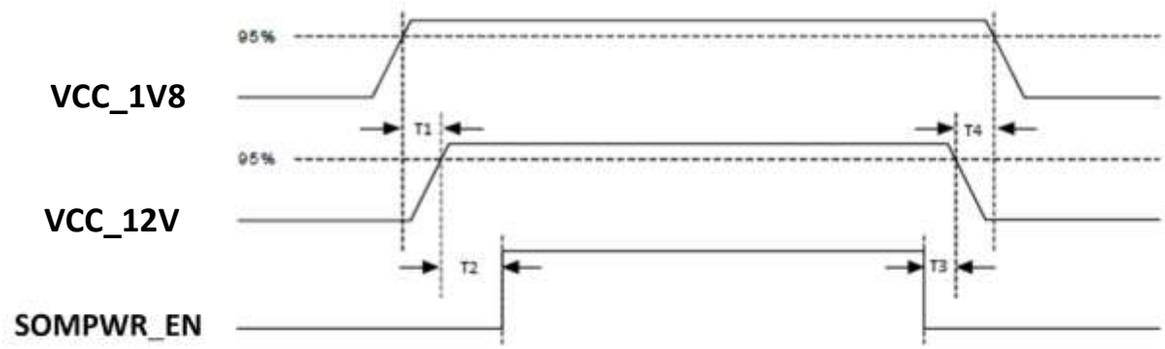

Figure 10: Power Input Sequencing

Table 15: Power Sequence Timing

Item	Description	Value
T1	VRTC_1V8[1] rise time to VCC_12V rise time	≥ 0 ms
T2	VCC_12V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_12V fall time	≥ 0 ms
T4	VCC_12V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_1V8 is the RTC Battery backup supply. This is an optional power.

Important Note: VCC_12V input power to other all the powers are getting stable around TBD in SOM, Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.3 Power Consumption

Table 16: Power Consumption

TBD.

For more accurate power estimation, iWave recommends to use Intel Power Estimator (IPE) tool and calculate the SoC and FPGA power. Also add extra power for other On-SOM peripherals power.

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Intel Agilex 7 SoC and FPGA SOM.

Table 17: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS3 Compliance

iWave's Intel Agilex 7 SoC and FPGA SOM is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Intel Agilex 7 SoC and FPGA SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.

3.3 MechanicalCharacteristics

3.3.1 Intel Agilex 7 SoC and FPGA SOM Mechanical Dimensions

Intel Agilex 7 SoC and FPGA SOM PCB size is 90mm x 120mm x 3.2mm and weight is TBD. SOM mechanical dimension is shown below.

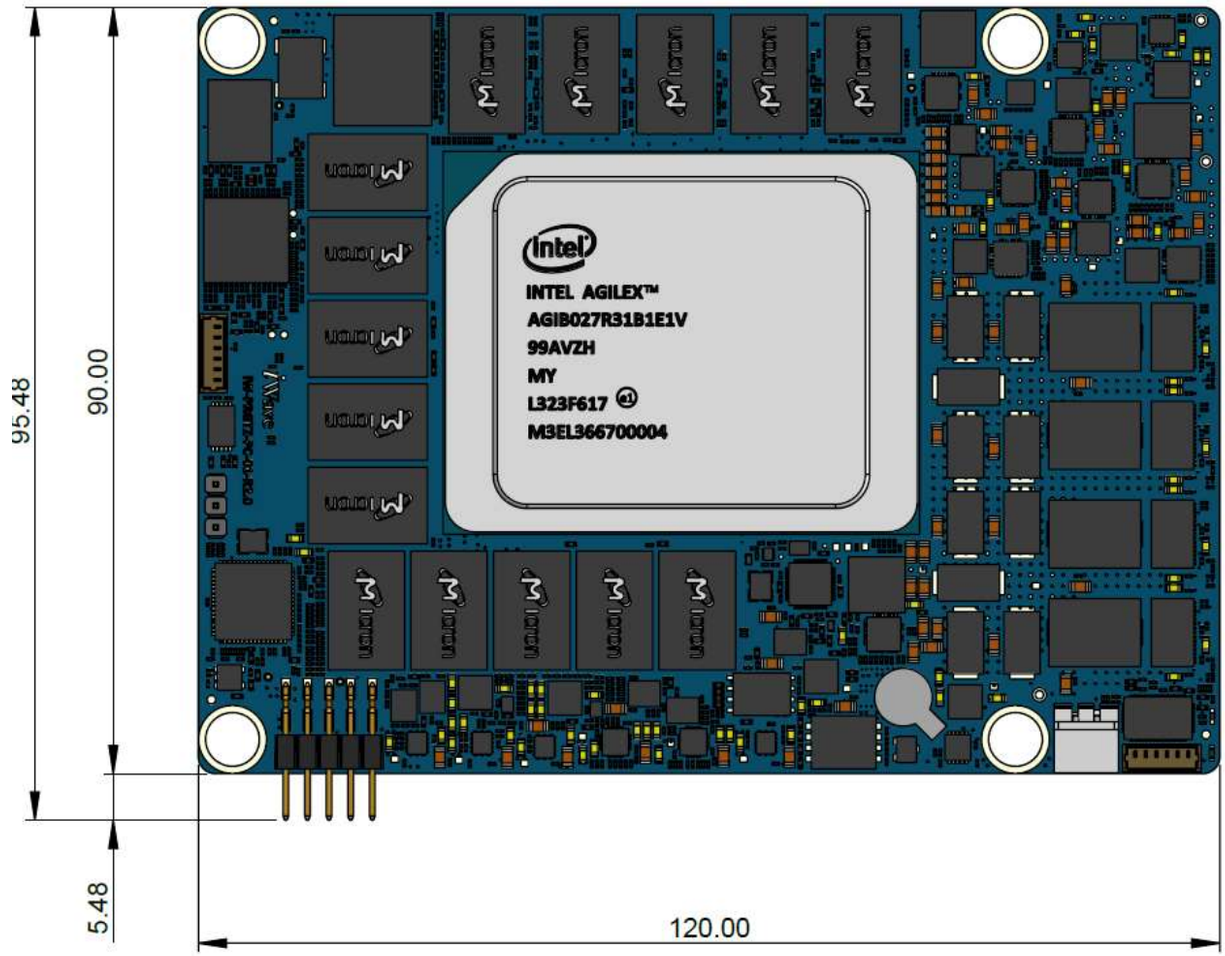

Figure 11: Mechanical dimension of Intel Agilex 7 SoC and FPGA SOM - Top View

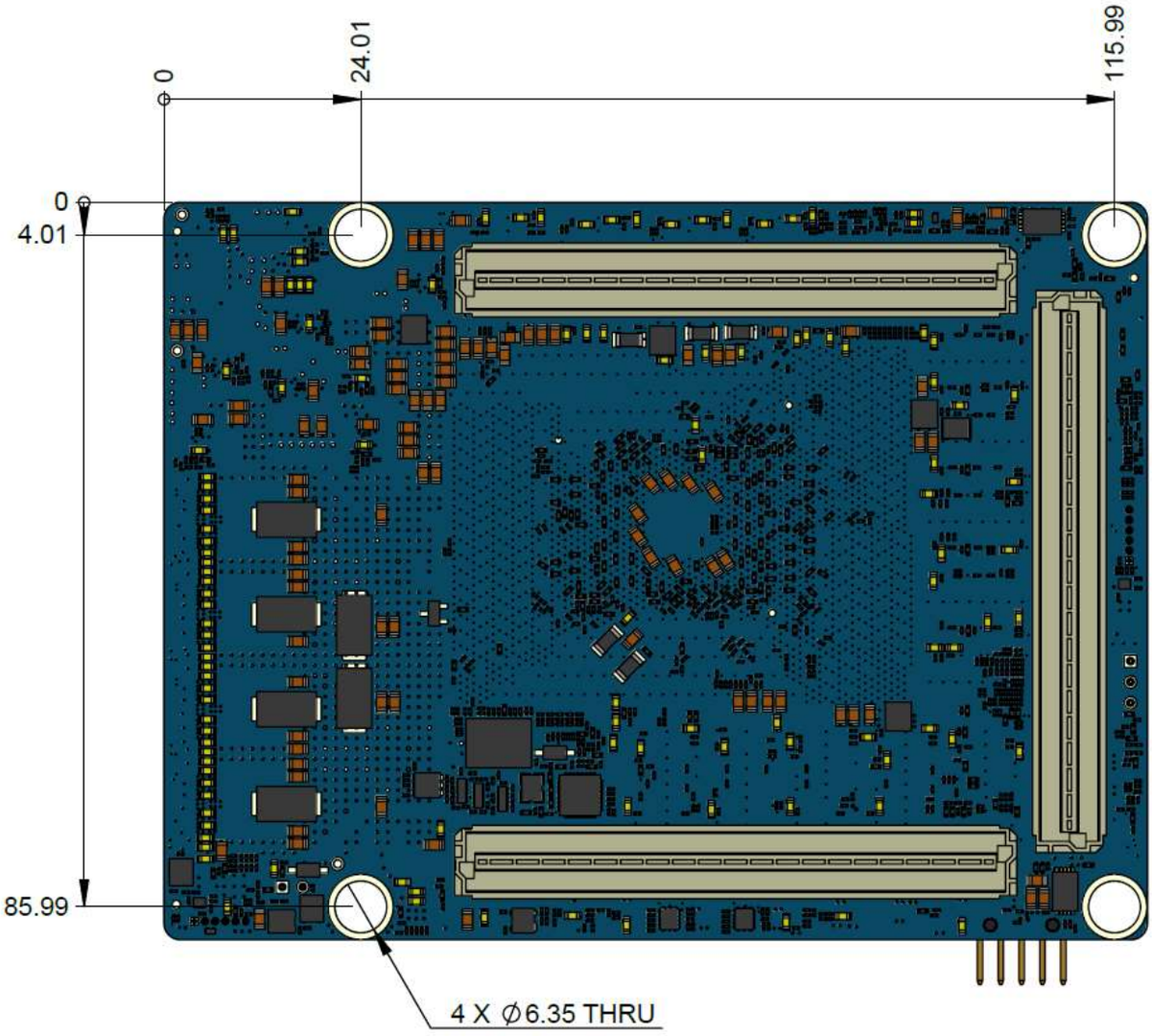

Figure 12: Mechanical dimension of Intel Agilex 7 SoC and FPGA SOM - Bottom View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Intel Agilex 7 SoC and FPGA SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 18: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G43M - AGIB027 (-1 speed) R31B Agilex 7 SOC SOM		
iW-G43M-AI27-4E008G-E0032G-BEA	AGIB027 (-1 speed) R31B Agilex 7 7 SOC SOM with 8GB HPS DDR4, Dual 8GB FPGA DDR4, 32GB eMMC SOM, Extended	-40°C to 85°C

5. APPENDIX

5.1 Intel Agilex 7 SoC and FPGA SOM Development Platform

iWave Systems supports iW-RainboW-G43D – Intel Agilex 7 SoC and FPGA SOM Development Platform which is targeted for quick validation of Intel Agilex 7 SoC and FPGA based SOM. iWave's Intel Agilex 7 SoC and FPGA Development Board incorporates Intel Agilex 7 SoC and FPGA SOM and High-performance Carrier board with complete BSP support.

For more details on Intel Agilex 7 SoC and FPGA SOM Development Platform, visit the below web link:

Link: *https://www.iwavesystems.com/product/Agilex 7-r31b-r31c-soc-fpga-som/*

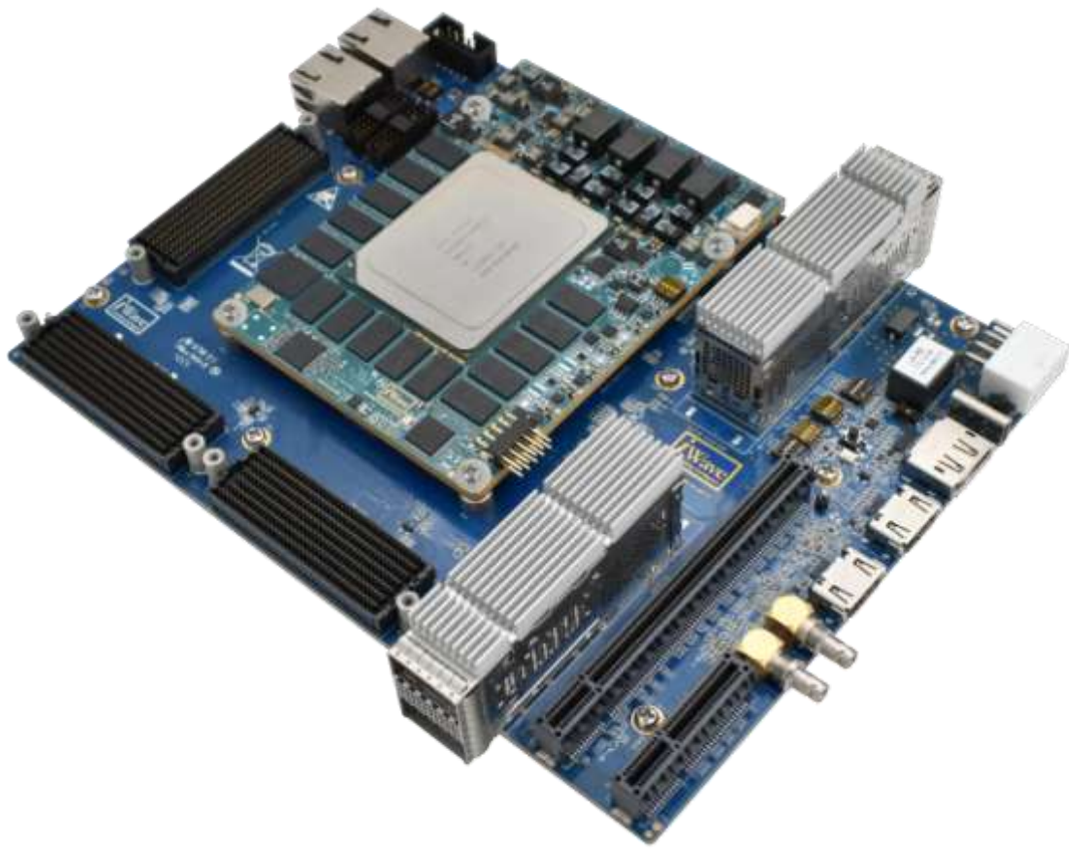

Figure 13: Intel Agilex 7 SoC and FPGA SOM Development Platform


iWave
Embedding Intelligence