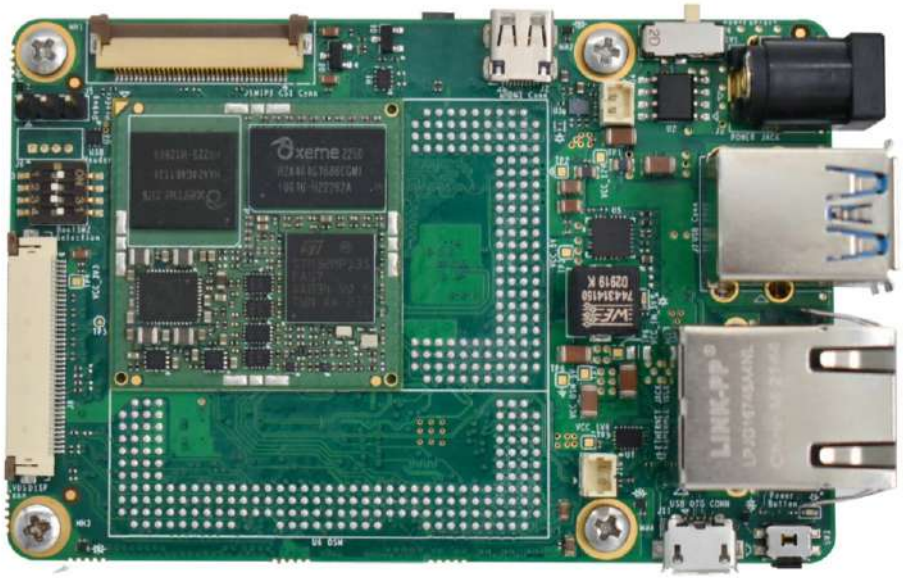
iW-RainboW-G54S
STM32MP135 based
Single Board Computer
Datasheet



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1. INTRODUCTION

1.1 Purpose

This document is the Datasheet for the Single Board Computer based on the STMicroelectronics's STM32MP135 Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the STMicroelectronics's STM32MP135 SBC from a Hardware Systems perspective.

1.2 SBC Overview

The SBC (Single Board Computer) definition targeting application that require low power, low costs, and high security. The SBCs are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies and GBe are concentrated on the SBC.

STMicroelectronics's STM32MP135 MPU based Single Board Computer is rich with STM32MP135 features along with Gigabit Ethernet PHY, Micro SD, eMMC and comes in compact 85mm x 56mm form factor.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
OTG	On-The-Go
PCB	Printed Circuit Sheet
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory

Acronyms	Abbreviations
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SBC	Single Board Computer
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on SBC.

1.5 References

- STM32MP131_Datasheet.pdf
- STM32MP133_Datasheet.pdf
- STM32MP135_Datasheet.pdf
- STM32MP13_RM.pdf

1.6 Important Note

In this document, wherever STM32MP135 SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(PA_0)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***PA_0*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about STM32MP135 SBC features and Hardware architecture with high level block diagram.

2.1 STM32MP135 SBC Block Diagram

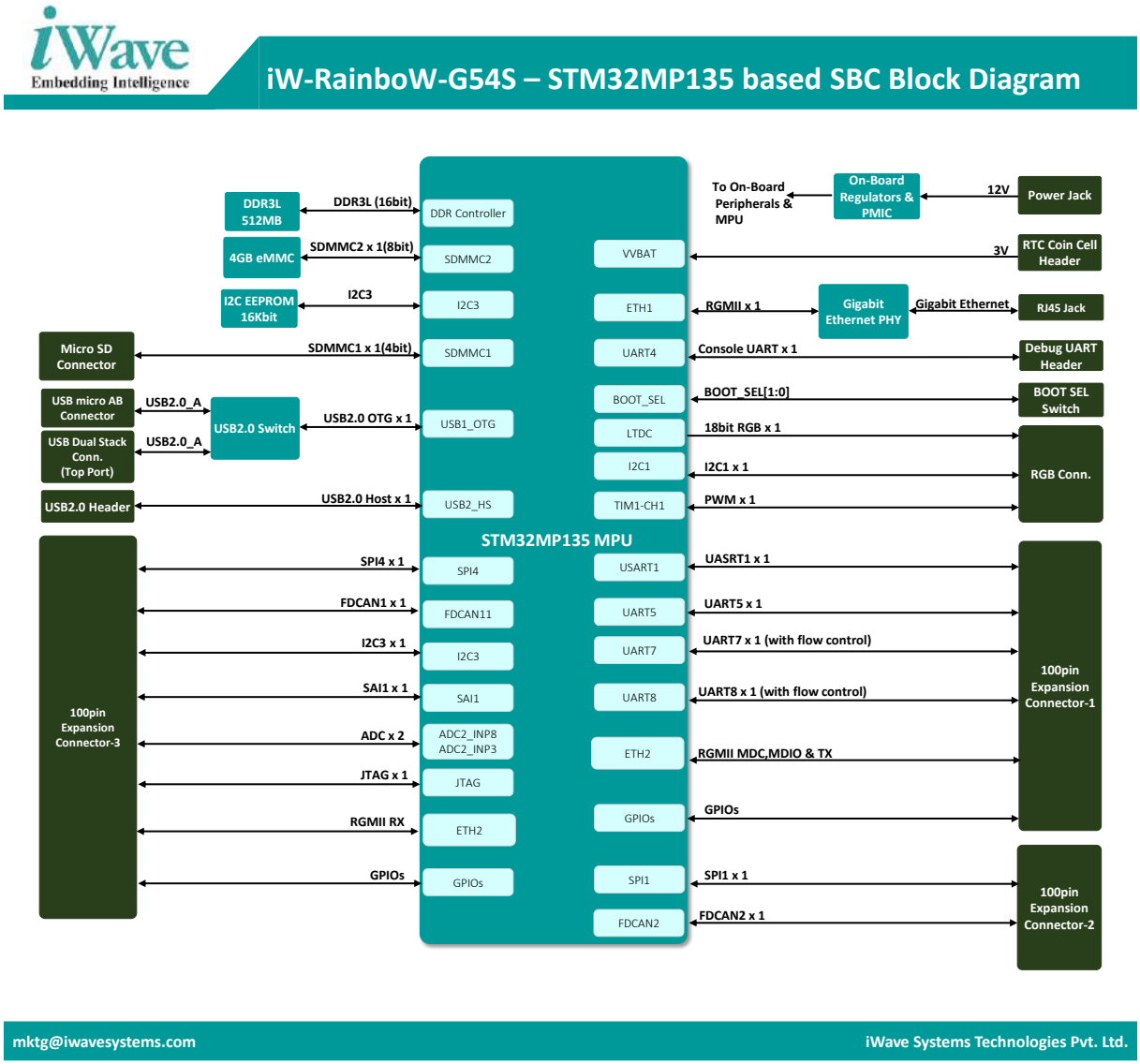

Figure 1: STM32MP135 SBC Block Diagram

2.2 STM32MP135 SBC Features

STM32MP135 SBC supports the following features.

CPU

- STM32MP135 Applications Processor
    - STM32MP135: Cortex®-A7 up to 1 GHz, 30 Communication peripherals including CAN, Ethernet 2

Power

- STPMIC1EPQR PMIC

Memory

- DDR3L – 512MB (Expandable up to 1GB) [1]
- eMMC – 8bit (4GB-Expandable) [1]
- Micro SD slot
- EEPROM - 16Kbit

Network & Communication

- Gigabit Ethernet PHY Transceiver with RJ45 Magjack Connector x 1
- USB 2.0 OTG port through – microAB Receptacle Connector
- USB 2.0 Header x 1

Display interface

- 18 Bit RGB display x 1

Expansion Connector 1, 2 & 3 Interfaces

- FDCAN x 2 Ports
- UART x 2 Ports (with flow control)
- UART x 2 Ports (without flow control)
- SPI X 2 Ports
- SAI X 1Port
- RGMII X 1 Port
- ADC – 2 Ports
- I2C – 1 Port

Miscellaneous Interfaces

- Debug UART Connector
- RTC Battery Connector
- FAN Connector

General Specification

- Power Supply : 12V, 2A
- Form Factor : 85mm x 56mm

1. *Memory Size will differ based on iWave's SBC Product Part Number.*

2.3 CPU

iW-RainboW-G54S-STM32MP135 SBC can support different STM32MP135 SoCs from STMicroelectronics.

2.4 STM32MP135 SoC

iW-RainboW-G54S SBC can support STM32MP135 MPUs from STMicroelectronics. The STM32MP13x family consists of three processors: STM32MP131, STM32MP133, and STM32MP135. We can also support the STM32MP131 and STM32MP133 MPU but with feature deduction as per the CPU.

- STM32MP135: Cortex®-A7 up to 1 GHz, 30 Communication peripherals including CAN, Ethernet 2 and camera interface.

The STM32MP135 processors have advanced multicore processing with symmetric multiprocessing supported by Arm cores. Memory interfaces supporting DDR3L, Quad SPI and a wide range of peripheral I/Os.

STM32MP135

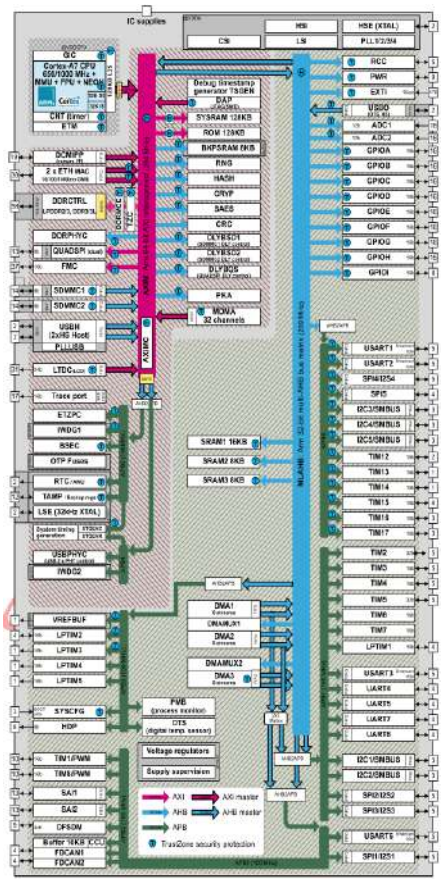

Figure 2: STM32MP135 Block Diagram

Note: The STM32MP135 processor offers numerous advanced features, please refer the latest STM32MP135 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.5 PMIC

The STM32MP135 SBC uses one STPMIC1EPQR (U5) for module power management. The STPMIC1EPQR features six LDOs, four buck and one boost regulator. It is a high-performance Power Management Integrated Circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The STPMIC1EPQR comes in 44 pin WFQFN (5x6) Package and is placed on the Top side of the Module.

2.6 Memory

2.6.1 DDR3L

The STM32MP135 SBC supports 512MB DDR3L SDRAM memory by default using 16bit DDR_CH0 channel of STM32MP135 SoC to support DDR3L up to 533MHz. DDR3L part is placed on Top side of the SBC. To customize the DDR3L memory size (up to 1GB), contact iWave.

2.6.2 eMMC Flash Memory

The STM32MP135 SBC supports 4GB eMMC as a boot as well as storage device. This is directly connected to SDMMC2 controller of the STM32MP135 MPU and operates at 1.8V (I/O supply).

The eMMC flash memory is physically located on Top side of the SBC. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.6.3 Micro SD Connector

The STM32MP135 SBC supports Micro SD slot which can be used to connect Micro SD card as a boot device as well as Mass storage device. Micro SD card connector (J13) is directly connected to the SDMMC1 controller of the STM32MP135 MPU. The main power to Micro SD Card Connector is 3.3 Voltage. The micro–SD Connector is physically located on bottom side of the STM32MP135 SBC as shown below.

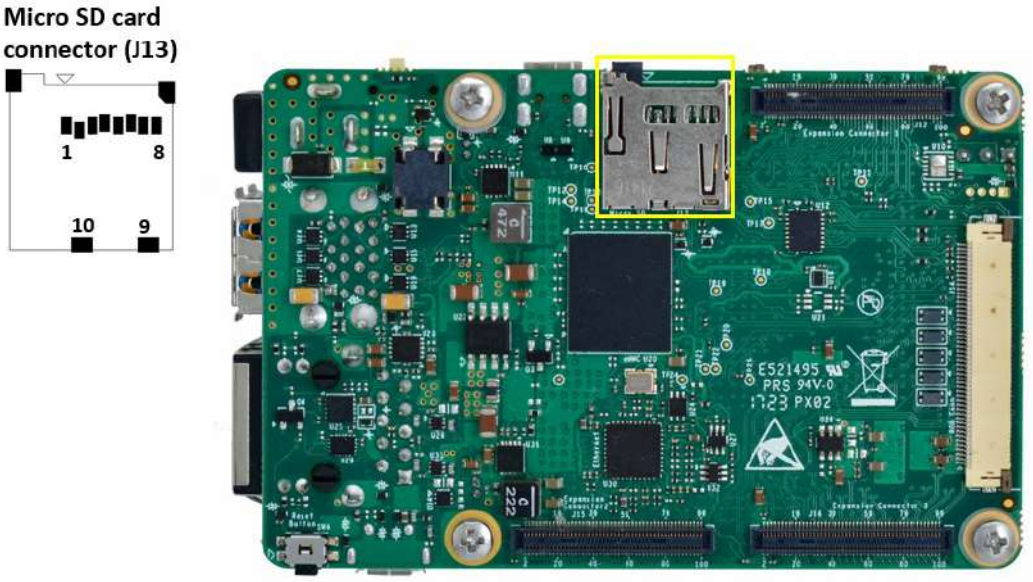

Figure 3: Micro SD Card Connector

2.6.4 Boot Media Setting

STM32MP135 MPU boot process begins at Power on Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. STM32MP135 MPU Boot ROM code uses the state of the internal register BOOT_MODE [2:0] to determine the boot flow behaviour of the device.

The STM32MP135 SBC can boot from the Micro SD and eMMC. Also, for programming, we can make use of either the Debug UART connector or the USB2.0 micro-B Connector.

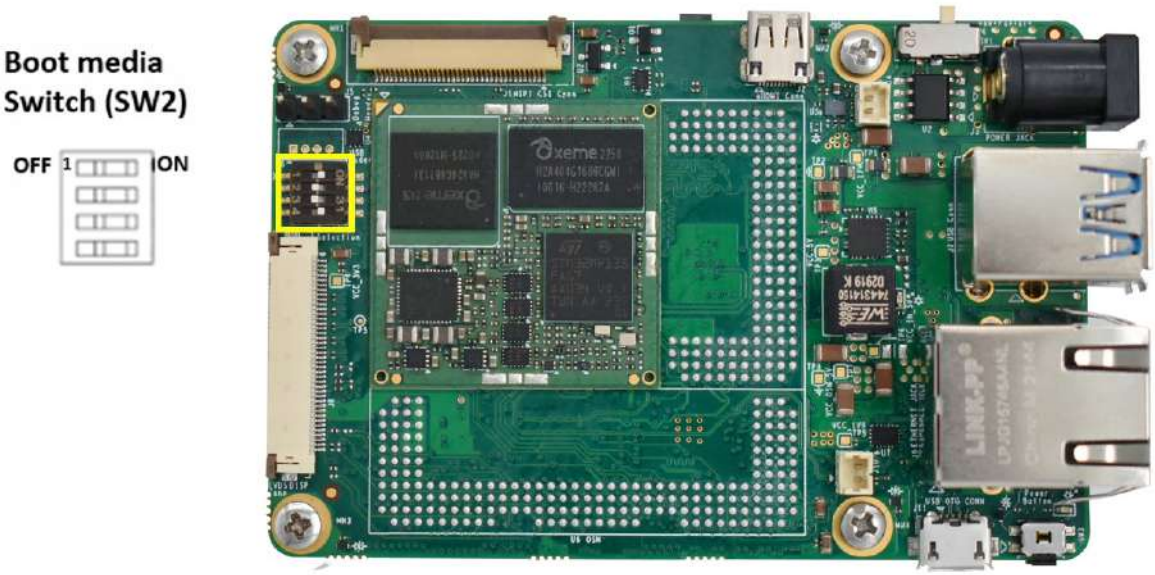

Figure 4: Boot Media Switch

Table 3: Boot Media Settings

Boot Media	SW2		
	POS3 (Force_Recov#)	POS2 (BOOT_SEL1)	POS1 (BOOT_SEL0)
Serial NOR Flash (QSPI)	OFF	ON	ON
SD Card (SDMMC1)	OFF	OFF	ON
UART/USB Boot	ON	-	-

Note: The fourth bit of SW2 is used for selection between USB2.0 Micro-B connector and Top port of the USB dual stack connector. By default, USB2.0 Micro-B Connector is supported and for the same the 4th bit must be turned ON.

2.7 Network & Communication

2.7.1 Gigabit Ethernet Interface

The STM32MP135 SBC supports single Ethernet Port interface through external Ethernet PHY from Analog Devices which supports 10/100/1000Mbps Ethernet.

The Ethernet PHY ADIN1300BCPZ integrates Analog Devices Inc. power-saving technologies and significantly saves power not only during work time but also overtime. Analog Devices Inc. power savings include ultra-low power in cable unplugged mode or port power down mode and automatic optimised power saving based on cable length. The ADIN1300BCPZ also supports the IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Analog Devices Inc. proprietary Smart EEE. The Smart EEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

The Ethernet PHY's output signal GBE0 is directly connected to RJ45 Magjack (J9). Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. The RJ45 Magjack connector is physically located at the top of the board as shown below.

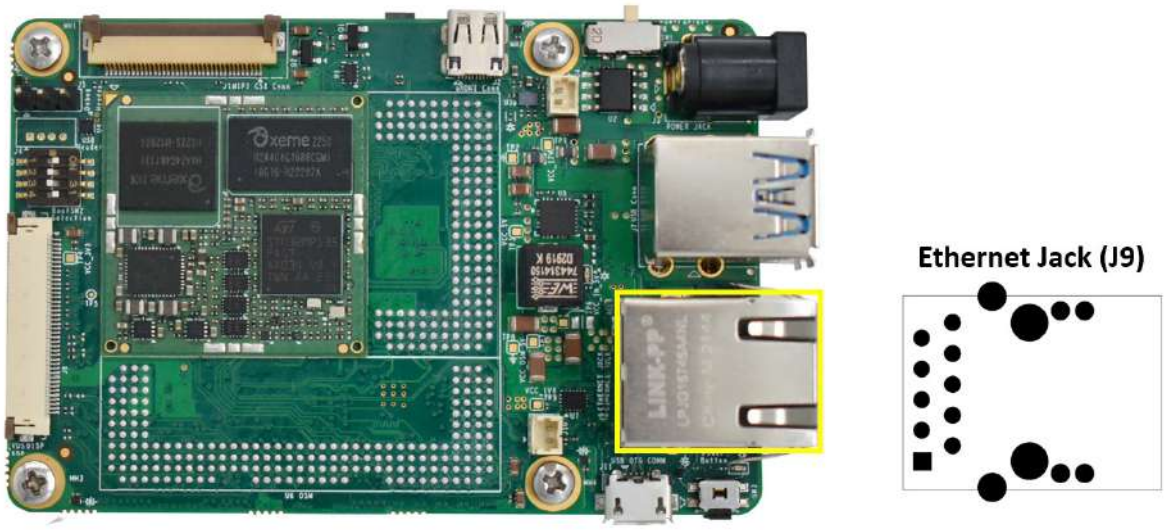

Figure 5: Single RJ45 Magjack

2.7.2 USB2.0 OTG Interface

The STM32MP135 SBC supports USB2.0 OTG interface. This USB2.0 signals is muxed between USB2.0 Micro-AB connector (J11) and USB TOP Port (J7). By default, the USB lines are connected to the Micro-B connector and by turning OFF the pin 4 of Switch (SW2), the connection can be switched to USB top port.

This port can be used for USB OTG functionality which supports USB host and USB device based on the USB ID pin status. This USB2.0 OTG connector is physically located at the top of the board as shown below.

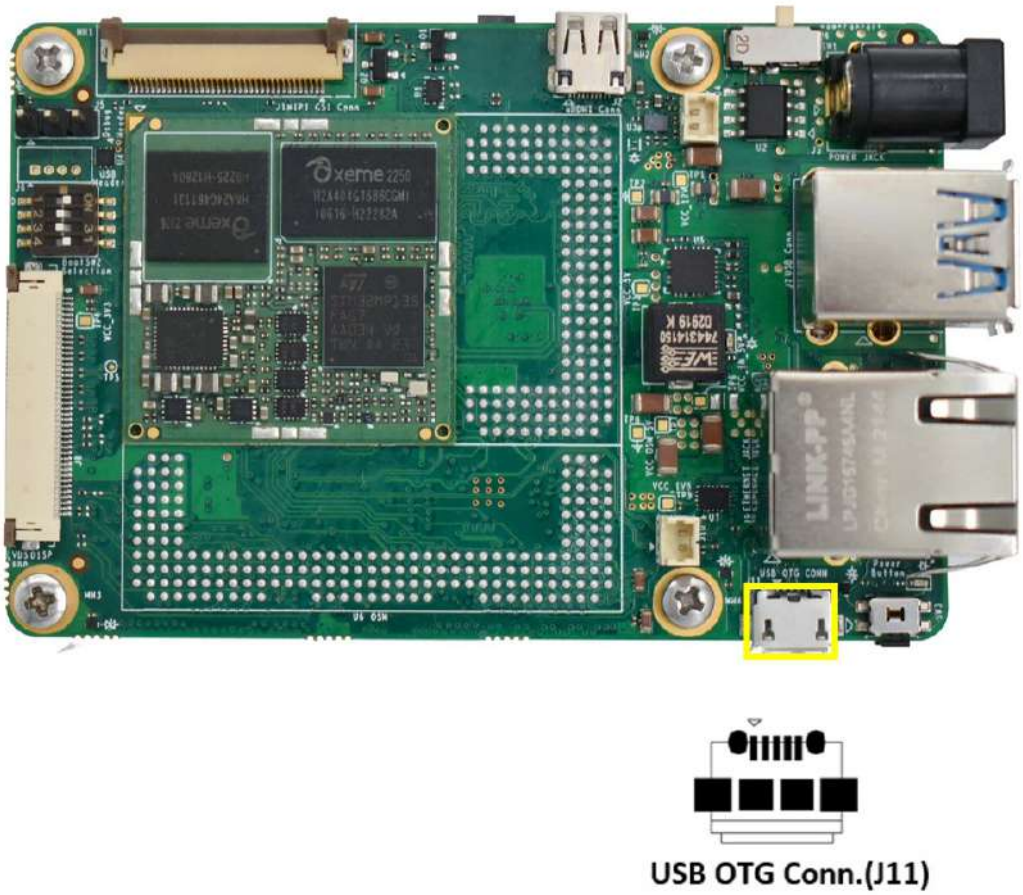

Figure 6: USB OTG Connector

2.7.3 USB Header

The STM32MP135 SBC supports USB2.0 Host interface through a 4pin USB Header. This USB Header(J6) is physically located at the top of the board as shown below.

Connector Part Number: 53047-0410 from Molex

Mating Connector Part Number: 0510210400 from Molex

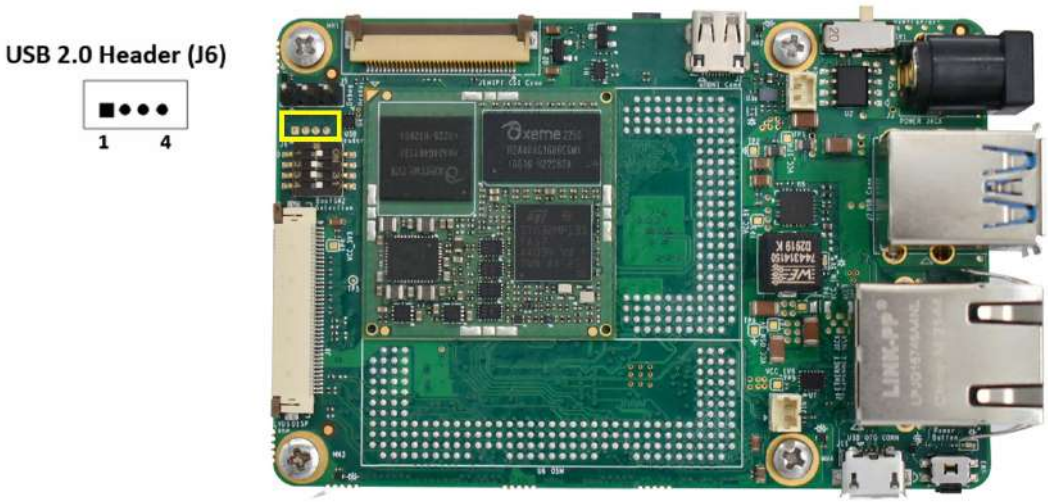

Figure 7: USB Header

Table 4: USB Header Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	1	VBUS_HOST_TP	5V, Power	5V Supply Voltage.
2	2	USB_DM1	I, USB	Differential USB Negative.
3	3	USB_DP1	I, USB	Differential USB Positive.
4	4	GND	Power	Ground.

2.8 Serial Interface Features

2.8.1 Debug UART Interface

The STM32MP135 SBC supports debug interface through STM32MP135 SoC's UART4 interface. This UART4 signals from the SoC is connected to Debug UART header(J5) through a 1.8V to 3.3V level translator. This Debug UART header can be used for debug purpose, and is physically located at the top of the board as shown below:

Number of Pins : 3

Connector Part number : M20-9990345 from Harwin

USB to UART Cable : TTL-232R-RPI from FTDI

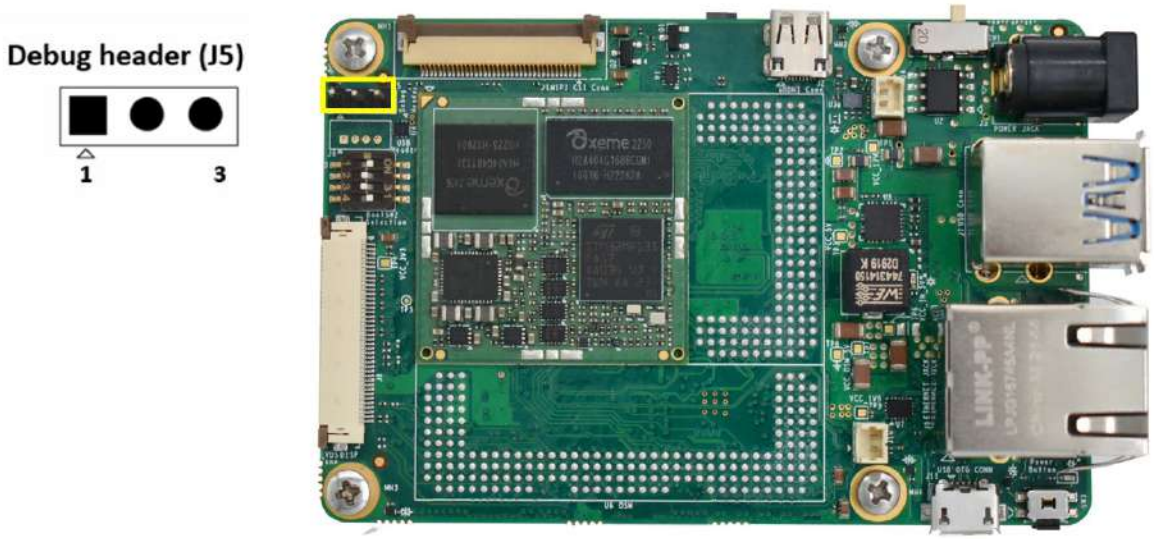

Figure 8: Debug UART Header

Table 5: Debug UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	TX	UART4_TX(PD6)	O, 3.3V CMOS	UART interface Receive signal.
2	RX	UART4_RX(PD8)	I, 3.3V CMOS	UART interface Transmit signal.
3	GND	GND	Power	Ground.

2.9 Display interfaces

2.9.1 50 Pin RGB connector

The STM32MP135 based SBC supports 18bit RGB Display interface through SoC's RGB interface. This 18-bit RGB signals from the SoC is connected to the RGB display Connector (J14) which is a 50-pin connector. This connector is physically placed on the bottom of the board as shown below.

Number of Pins : 50

Connector Part : 541045033 from Molex

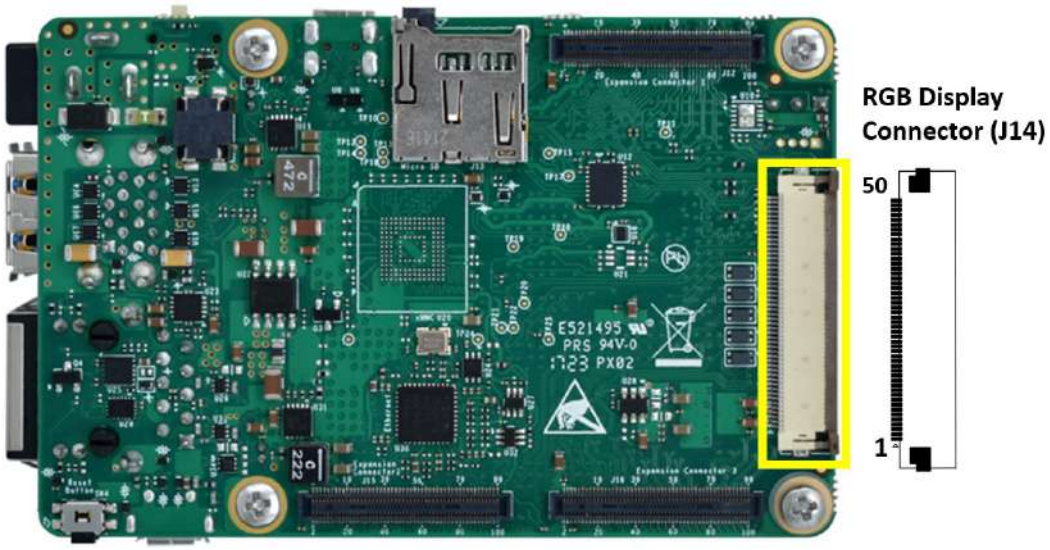

Table 6: RGB Connector(J14) Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VDD1	VCC_3V3	Power	IO Power Input.
2	VDD2	VCC_3V3	Power	IO power Input.
3	VDD3	VCC_3V3	Power	IO Power Input.
4	VDD1	VCC_5V	Power	LED back light power Input.
5	VDD2	VCC_5V	Power	LED Back light Power Input.
6	VDD3	VCC_5V	Power	LED Back light Power Input.
7	GND1	GND	Power	Ground.
8	R0	NC	NC	NC.
9	R1	NC	NC	NC.
10	R2	RGB_D0_LTDC_R2(PG7)3V3	O CMOS	Red data bit 0.
11	R3	RGB_D1_LTDC_R3(PB12)3V3	O CMOS	Red data bit 1.
12	GND2	GND	Power	Ground.
13	R4	RGB_D2_LTDC_R4(PD4)3V3	O CMOS	Red data bit 2.
14	R5	RGB_D3_LTDC_R5(PF5)3V3	O CMOS	Red data bit 3.
15	R6	RGB_D4_LTDC_R6(PH8)3V3	O CMOS	Red data bit 4.
16	R7	RGB_D5_LTDC_R7(PE9)3V3	O CMOS	Red data bit 5.
17	GND3	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
18	G0	NC	NC	NC.
19	G1	NC	NC	NC.
20	G2	RGB_D6_LTDC_G2(PH13)3V3	O CMOS	Green data bit 0.
21	G3	RGB_D7_LTDC_G3(PF3)3V3	O CMOS	Green data bit 1.
22	GND4	GND	Power	Ground.
23	G4	RGB_D8_LTDC_G4(PD5)3V3	O CMOS	Green data bit 2.
24	G5	RGB_D9_LTDC_G5(PG0)3V3	O CMOS	Green data bit 3.
25	G6	RGB_D10_LTDC_G6(PA12)3V3	O CMOS	Green data bit 4.
26	G7	RGB_D11_LTDC_G7(PA15)3V3	O CMOS	Green data bit 5.
27	GND5	GND	Power	Ground.
28	B0	RGB_DISP_EN(PI2)	O CMOS	Primary Display power enable, active high.
29	B1	RGB_BL_EN(PI0)	O CMOS	Primary Display backlight enable, active high.
30	B2	RGB_D12_LTDC_B2(PH7)3V3	O CMOS	Blue data bit 0.
31	B3	RGB_D13_LTDC_B3(PF2)3V3	O CMOS	Blue data bit 1.
32	GND6	GND	Power	Ground.
33	B4	RGB_D14_LTDC_B4(PH3)3V3	O CMOS	Blue data bit 2.
34	B5	RGB_D15_LTDC_B5(PD15)3V3	O CMOS	Blue data bit 3.
35	B6	RGB_D16_LTDC_B6(PB6)3V3	O CMOS	Blue data bit 4.
36	B7	RGB_D17_LTDC_B7(PF1)3V3	O CMOS	Blue data bit 5.
37	GPIO	OSM_GPIO_A_2(PH2)	O CMOS	Touch Reset
38	DE	RGB_LTDC_DE(PH9)3V3	O CMOS	Data Enable.
39	HS	RGB_LTDC_HSYNC(PH10)3V3	O CMOS	Horizontal synch.
40	VS	RGB_LTDC_VSYNC(PG4)3V3	O CMOS	Vertical synch.
41	DCLK	RGB_LTDC_CLK(PD9)3V3	O CMOS	Pixel Clock Signal.
42	GND7	GND	Power	Ground.
43	USB_D+	NC	NC	NC
44	USB _D-	NC	NC	NC
45	GND8	GND	Power	Ground.
46	PWM	TIM1_CH1(PF9)	O CMOS	PWM signal.
47	$\overline{\text{RESET}}$	RGB_LTDC_DE(PH9)3V3	O CMOS	Global Reset signal.
48	I2C3_SCL	I2C1_SCL(PD12)	O CMOS	I2C Clock signal.
49	I2C3_SDA	I2C1_SDA(PD3)	O CMOS	I2C Data signal.
50	INT	OSM_GPIO_A_3(PI3)	NC	NC

2.10 Expansion Connector - 1

The MPU interfaces which are not supported directly on the SBC are made available at the Expansion connectors so that they can be utilized making use of daughter cards. The interfaces which are available at 100 Pin Expansion connectors are explained in the following section. The stack height for this expansion connector is 4mm.These Expansion Connector (J12, J15 & J16) are physically located at the bottom of the SBC as shown below.

Number of Pins : 100

Connector Part : 10164227-1004A1RLF

Mating Connector : 10164228-1001A1RLF

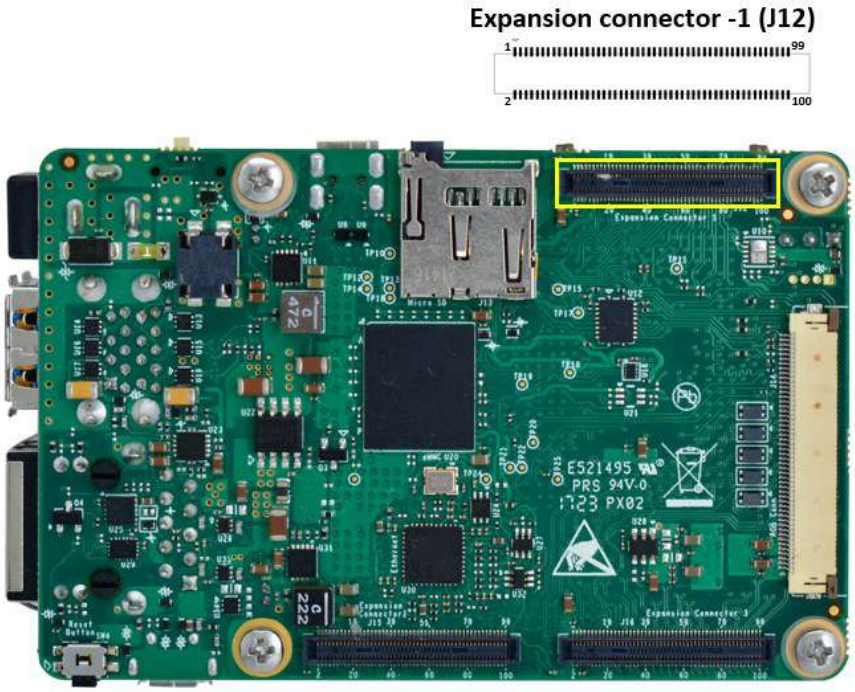

Figure 9: Expansion Connector-1

Table 7: Expansion Connector-1 Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_5V	-	Power	5V Supply Voltage.
2	VCC_5V	-	Power	5V Supply Voltage.
3	VCC_5V	-	Power	5V Supply Voltage.
4	VCC_5V	-	Power	5V Supply Voltage.
5	VCC_5V	-	Power	5V Supply Voltage.
6	VCC_5V	-	Power	5V Supply Voltage.
7	GND	-	Power	Ground.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
8	VCC_5V	-	Power	5V Supply Voltage.
9	USART1_TX(PA9)	PA9/ D2	O, 1.8V CMOS	USART1 Transmitter.
10	GND	-	Power	Ground.
11	USART1_RX(PD13)	PD13/ N1	I, 1.8V CMOS	USART1 Receiver.
12	VCC_1V8	-	Power	1.8V Supply Voltage.
13	NC	-	-	NC
14	VCC_1V8	-	Power	1.8V Supply Voltage.
15	NC	-	-	NC
16	PWR_CPU_ON	NA	I,1.8V	Signal connected to PWR_CPU_ON pin of PMIC
17	NC	-	-	NC
18	UART5_TX(PE7)	PE7/ C4	O, 1.8V CMOS	UART5 Transmitter.
19	NC	-	-	NC
20	UART5_RX(PF13)	PF13/ T3	I, 1.8V CMOS	USART5 Receiver.
21	NC	-	-	NC
22	NC	-	-	NC
23	NC	-	-	NC
24	NC	-	-	NC
25	NC	-	-	NC
26	NC	-	-	NC
27	NC	-	-	NC
28	NC	-	-	NC
29	NC	-	-	NC
30	NC	-	-	NC
31	NC	-	-	NC
32	NC	-	-	NC
33	NC	-	-	NC
34	NC	-	-	NC
35	NC	-	-	NC
36	PWR_LP	PWR_LP/U14	O, 1.8	Connected to CPU PWR_LP pin
37	GND	-	Power	Ground.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
38	UART8_CTS(PD14)	PD14 / F7	I, 1.8V CMOS	USART8 Clear to Send.
39	NC	-	-	NC
40	UART8_RTS(PE14)	PE14/E2	O, 1.8V CMOS	USART8 Request to Send.
41	OSM_GPIO_A_4(PA14)	PA14/R11	IO, 1.8V	General purpose IO
42	GND	-	Power	Ground.
43	NC	-	-	NC
44	UART7_TX(PE8)	PE8/F8	O, 1.8V CMOS	UART7 Transmitter.
45	OSM_GPIO_A_5(PA13)	PA13/K7	IO, 1.8V	General purpose IO
46	UART7_RX(PD11)	PD11/G1	I, 1.8V CMOS	UART7 Receiver.
47	NC	-	-	NC
48	UART7_CTS(PG15)	PG15/G8	I, 1.8V CMOS	UART7 Clear to Send.
49	OSM_GPIO_A_6(PI1)	PI1/N4	IO, 1.8V	General purpose IO
50	UART7_RTS(PF10)	PF10/K2	O, 1.8V CMOS	UART7 Request to Send.
51	NC	-	-	NC
52	UART8_RX(PE0)	PE0/ B3	I, 1.8V CMOS	UART8 Receiver.
53	NC	-	-	NC
54	UART8_TX(PE1)	PE1/C3	O, 1.8V CMOS	UART8 Transmitter.
55	NC	-	-	NC
56	NC	-	-	NC
57	NC	-	-	NC
58	NC	-	-	NC
59	GND	-	Power	Ground.
60	NC	-	-	NC
61	NC	-	-	NC
62	ETH2_MDIO(PB2)	PB2/K3	IO, 1.8V	ETH2 MDIO
63	NC	-	-	NC
64	ETH2_MDC(PG5)	PG5/ H1	O, 1.8V	ETH2 MCD
65	GND	-	Power	Ground.
66	GND	-	Power	Ground.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
67	NC	-	-	NC
68	NC	-	-	NC
69	NC	-	-	NC
70	NC	-	-	NC
71	GND	-	Power	Ground.
72	NC	-	-	NC
73	NC	-	-	NC
74	NC	-	-	NC
75	NC	-	-	NC
76	NC	-	-	NC
77	GND	-	Power	Ground.
78	NC	-	-	NC
79	NC	-	-	NC
80	NC	-	-	NC
81	NC	-	-	NC
82	NC	-	-	NC
83	GND	-	Power	Ground.
84	NC	-	-	NC
85	NC	-	-	NC
86	GND	-	Power	Ground.
87	NC	-	-	NC
88	ETH2_RGMII_ TXD3(PE6)	PE6/ R2	IO,1.8V	ETH2 TX Data 3
89	GND	-	Power	Ground.
90	ETH2_RGMII_ TXD1(PG11)	PG11/ R1	IO,1.8V	ETH2 TX Data 1
91	NC	-	-	NC
92	ETH2_RGMII_ TXD2(PG1)	PG1/ P4	IO,1.8V	ETH2 TX Data 2
93	NC	-	-	NC

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
94	ETH2_RGMII_ TXD0(PF7)	PG11/ R1	IO,1.8V	ETH2 TX Data 0
95	GND	-	Power	Ground.
96	ETH2_RGMII_ TX_CTL(PF6)	PF6/L1	IO,1.8V	ETH2 CTL
97	NC	-	-	NC
98	ETH2_RGMII_ GTX_CLK(PG3)	PG3/ U2	IO,1.8V	ETH2 RGMII CLK
99	NC	-	-	NC
100	GND	-	Power	Ground

*Note: Refer GPIO Column under **"STM32MP135 Pin Multiplexing on Expansion Connector** for details on GPIO options available from Expansion connector.*

2.11 Expansion Connector – 2

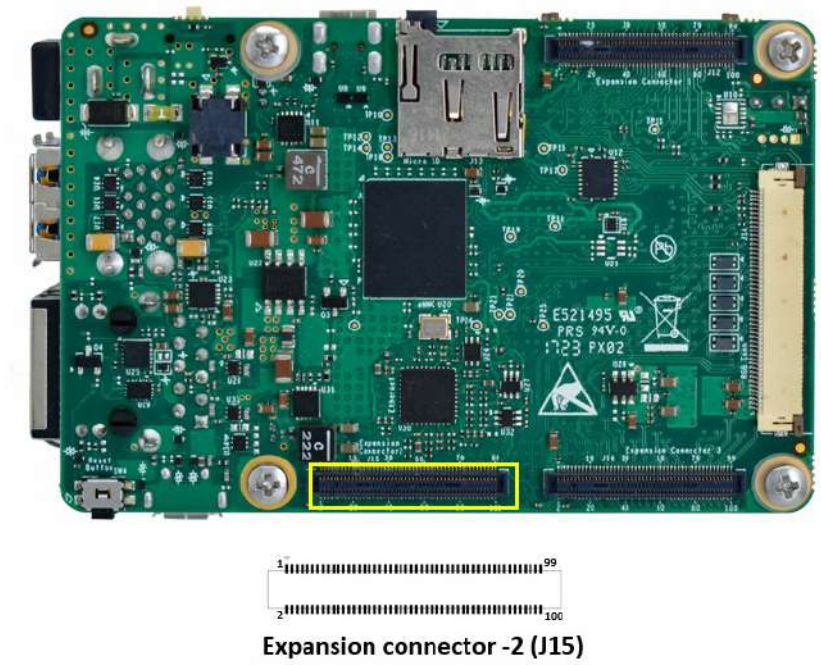

Figure 10: Expansion Connector-2

Table 8: Expansion Connector-2 Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_12V	-	Power	12V Supply Voltage.
2	VCC_12V	-	Power	12V Supply Voltage.
3	VCC_12V	-	Power	12V Supply Voltage.
4	VCC_12V	-	Power	12V Supply Voltage.
5	VCC_12V	-	Power	12V Supply Voltage.
6	VCC_12V	-	Power	12V Supply Voltage.
7	GND	-	Power	Ground.
8	GND	-	Power	Ground.
9	NC	-	-	NC
10	NC	-	-	NC
11	NC	-	-	NC
12	NC	-	-	NC
13	GND	-	Power	Ground.
14	GND	-	Power	Ground.
15	NC	-	-	NC
16	NC	-	-	NC
17	NC	-	-	NC
18	NC	-	-	NC
19	GND	-	Power	Ground.
20	GND	-	Power	Ground.
21	NC	-	-	NC
22	NC	-	-	NC
23	NC	-	-	NC
24	NC	-	-	NC
25	GND	-	Power	Ground.
26	GND	-	Power	Ground.
27	NC	-	-	NC
28	NC	-	-	NC
29	NC	-	-	NC

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
30	NC	-	-	NC
31	NC	-	-	NC
32	GND	-	Power	Ground.
33	NC	-	-	NC
34	NC	-	-	NC
35	NC	-	-	NC
36	NC	-	-	NC
37	NC	-	-	NC
38	GND	-	Power	Ground.
39	NC	-	-	NC
40	NC	-	-	NC
41	NC	-	-	NC
42	NC	-	-	NC
43	NC	-	-	NC
44	GND	-	Power	Ground.
45	NC	-	-	NC
46	NC	-	-	NC
47	NC	-	-	NC
48	NC	-	-	NC
49	NC	-	-	NC
50	GND	-	Power	Ground.
51	NC	-	-	NC
52	NC	-	-	NC
53	NC	-	-	NC
54	NC	-	-	NC
55	GND	-	Power	Ground.
56	GND	-	Power	Ground.
57	NC	-	-	NC
58	NC	-	-	NC
59	NC	-	-	NC
60	NC	-	-	NC

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
61	NC	-	-	NC
62	GND	-	Power	Ground.
63	NC	-	-	NC
64	NC	-	-	NC
65	NC	-	-	NC
66	NC	-	-	NC
67	NC	-	-	NC
68	GND	-	Power	Ground.
69	NC	-	-	NC
70	NC	-	-	NC
71	NC	-	-	NC
72	NC	-	-	NC
73	NC	-	-	NC
74	NC	-	-	NC
75	NC	-	-	NC
76	NC	-	-	NC
77	NC	-	-	NC
78	NC	-	-	NC
79	NC	-	-	NC
80	NC	-	-	NC
81	NC	-	-	NC
82	NC	-	-	NC
83	NC	-	-	NC
84	NC	-	-	NC
85	NC	-	-	NC
86	SPI4_NSS(PD10)	PD10 / D3	O, 1.8V CMOS	SPI4 Master Chip Select 0.
87	NC	-	-	NC
88	NC	-	-	NC
89	NC	-	-	NC
90	SPI4_MOSI(PD1)	PD1 / C2	O, 1.8V CMOS	SPI4 Master OUT and Slave IN.
91	NC	-	-	NC

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
92	SPI4_MISO(PE13)	PE13 / C1	I, 1.8V CMOS	SPI4 Master IN and Slave OUT
93	NC	-	-	NC
94	SPI4_SCK(PE12)	PE12 / B1	O, 1.8V CMOS	SPI4 Serial Data Clock.
95	NC	-	-	NC
96	NC	-	-	NC
97	NC	-	-	NC
98	FDCAN2_TX(PB13)	PB13 / B10	O, 1.8V CMOS	CAN 2 Transmitter.
99	NC	-	-	NC
100	FDCAN2_RX(PB5)	PB5/ F9	I, 1.8V CMOS	CAN 2 Receiver.

*Note: Refer GPIO Column under **"STM32MP135 Pin Multiplexing on Expansion Connector** for details on GPIO options available from Expansion connector.*

2.12 Expansion Connector – 3

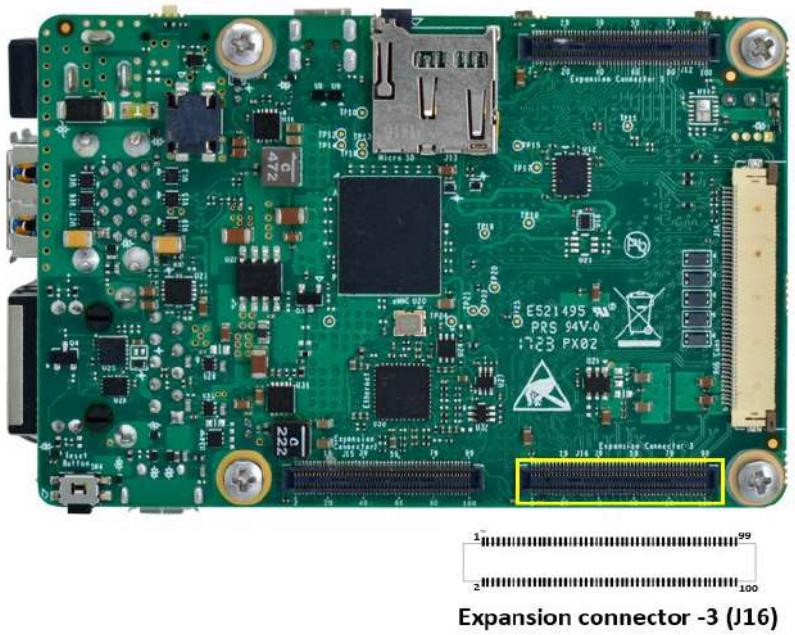

Figure 11: Expansion Connector-3

Table 9: Expansion Connector-3 Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_3V3	-	Power	3V3 Supply Voltage.
2	VCC_1V8	-	Power	1V8 Supply Voltage.
3	VCC_3V3	-	Power	3V3 Supply Voltage.
4	VCC_1V8	-	Power	1V8 Supply Voltage.
5	VCC_3V3	-	Power	3V3 Supply Voltage.
6	GND	-	Power	Ground.
7	VCC_3V3	-	Power	3V3 Supply Voltage.
8	NC	-	-	NC
9	GND	-	Power	Ground.
10	SPI1_NSS(PF12)	PF12/ J9	O, 1.8V CMOS	SPI1 Master Chip Select 0.
11	FDCAN1_RX(PG9)	PG9/ G5	I, 1.8V CMOS	CAN1 Receiver.
12	SAI1_SD_A(PA5)	PA5/ M7	O, 1.8V CMOS	SAI1 Data Out signal
13	FDCAN1_TX(PE10)	PE10/C7	O, 1.8V CMOS	CAN1 Transmitter.
14	I2C3_SDA(PH14)	PH14/B6	IO, 1.8V/1.5K PU	I2C3 DATA
15	NC	-	-	NC
16	I2C3_SCL(PB8)	PB8/ G4	O, 1.8V/1.5K PU	I2C3 Clock
17	NC	-	-	NC
18	GPIO_RSVD4(PA14)	PA14/R11	IO, 1.8V	General Purpose IO
19	NC	-	-	NC
20	NC	-	-	NC
21	NC	-	-	NC
22	SAI2_MCLK_A_RSVD (PA12)	PA12/ F2	O, 1.8V	SAI2 Master clock
23	GND	-	Power	Ground.
24	NC	-	-	NC
25	NC	-	-	NC
26	SAI1_FS_A(PE4)	PE4/K1	I, 1.8V	SAI1 clock
27	NC	-	-	NC
28	GND	-	Power	Ground.
29	GND	-	Power	Ground.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
30	NC	-	-	NC
31	NC	-	-	NC
32	NC	-	-	NC
33	NC	-	-	NC
34	SAI1_SCK_A(PH12)	PH12/G7	O, 1.8V	SAI1 BIT clock
35	GND	-	Power	Ground.
36	SAI1_SD_B(PG10)	PG10/H2	O, 1.8V	SAI1 Data1 input
37	NC	-	-	NC
38	SPI1_MOSI(PC0)	PC0/ T4	O, 1.8V CMOS	SPI1 Master OUT and Slave IN.
39	NC	-	-	NC
40	NC	-	-	NC
41	GND	-	Power	Ground.
42	NC	-	-	NC
43	NC	-	-	NC
44	SPI1_MISO(PA6)	PA6/R8	I, 1.8V CMOS	SPI1 Master IN and Slave OUT
45	NC	-	-	NC
46	SPI1_SCK(PC3)	PC3/ P7	O, 1.8V CMOS	SPI1 Serial Data Clock.
47	GND	-	Power	Ground.
48	NC	-	-	NC
49	NC	-	-	NC
50	NC	-	-	NC
51	NC	-	-	NC
52	JTAG_TDO	PH5/L12	O, 1.8V	JTAG Data Out Signal
53	GND	-	Power	Ground.
54	JTAG_NJTRST	NJTRST/ R10	IO, 1.8V	JTAG Reset
55	NC	-	-	NC
56	NC	-	-	NC
57	NC	-	-	NC
58	NC	-	-	NC
59	GND	-	Power	Ground.
60	JTAG_TDI	PH4/T13	I, 1.8V	JTAG Data In

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
61	NC	-	-	NC
62	JTAG_TCK	PF14/U4	O, 1.8V	JTAG Clock
63	NC	-	-	NC
64	JTAG_TMS	PF15/ L10	IO,1.8V	JTAG TMS
65	GND	-	Power	Ground.
66	ADC2_INP8(PF11)	PF11/ L8	Analog Signal	ADC Analog Input
67	NC	-	-	NC
68	NC	-	-	NC
69	NC	-	-	NC
70	ADC2_INP3(PA0)	PA0/ L7	Analog Signal	ADC Analog Input
71	GND	-	Power	Ground.
72	NC	-	-	NC
73	NC	-	-	NC
74	NC	-	-	NC
75	NC	-	-	NC
76	NC	-	-	NC
77	GND	-	Power	Ground.
78	NC	-	-	NC
79	NC	-	-	NC
80	NC	-	-	NC
81	NC	-	-	NC
82	NC	-	-	NC
83	GND	-	Power	Ground.
84	NC	-	-	NC
85	NC	-	-	NC
86	NC	-	-	NC
87	NC	-	-	NC
88	ETH2_RGMII_ RX_CLK(PH11)	PH11/ H7	O, 1.8V	ETH2 RGMII RX Clock
89	GND	-	Power	Ground.
90	NC	-	-	NC

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
91	NC	-	-	NC
92	ETH2_RGMII_ RXD3(PA8)	PA8/ J8	IO,1.8V	ETH2_RX Data3
93	NC	-	-	NC
94	ETH2_RGMII_ RXD2(PH6)	PH6/ J6	IO,1.8V	ETH2_RX Data2
95	GND	-	Power	Ground.
96	ETH2_RGMII_ RX_CTL(PG12)	PG12/L6	IO,1.8V	ETH2 CTRL signal
97	NC	-	-	NC
98	ETH2_RGMII_ RXD1(PA11)	PA11/N5	IO,1.8V	ETH2_RX Data1
99	NC	-	-	NC
100	ETH2_RGMII_ RXD0(PF4)	PF4/ P3	IO,1.8V	ETH2_RX Data0

*Note: Refer GPIO Column under **"STM32MP135 Pin Multiplexing on Expansion Connector** for details on GPIO options available from Expansion connector.*

2.13 Other Features

2.13.1 Fan Header

The STM32MP135 SBC supports a Fan Header to connect cooling fan if required. For the normal working, the SBC is able to function without any heatsink or fan. This Fan Header (J4) is physically located at the top of the board as shown below.

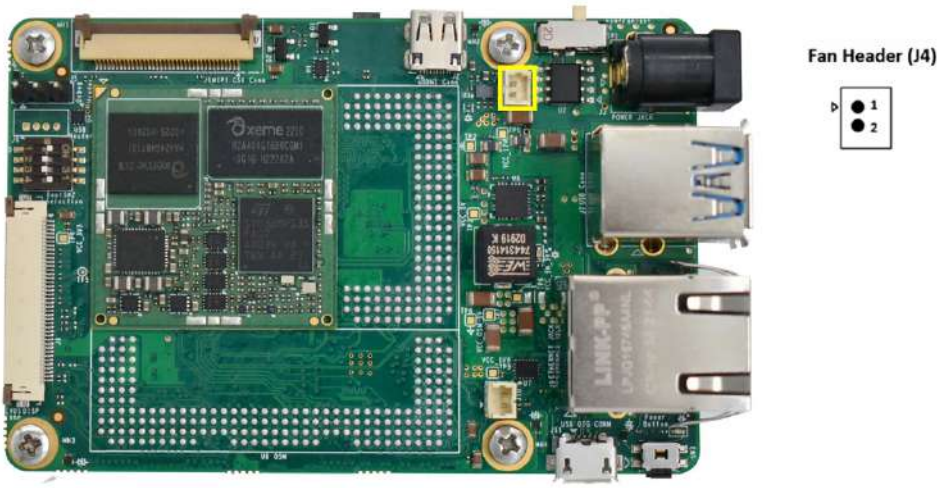

Figure 12: Fan Connector

Number of Pins : 2

Connector Part :10114829-10102LF from Amphenol ICC (FCI)

Table 10: Fan Connector Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN.
2	GND	Power	Ground.

2.13.2 RTC Battery Header

The STM32MP135 SBC supports RTC functionality making use of the MPU internal RTC. For the same an external RTC battery connector is made available. The SBC supports 2pin connector for backup battery or coin cell connection. The battery connected should be of DC 3V rating. This RTC power input is connect directly to the VBAT pin of the STM32MP135 SoC. The 2pin RTC (J4) battery connector is physically located on top side of the SBC as shown below.

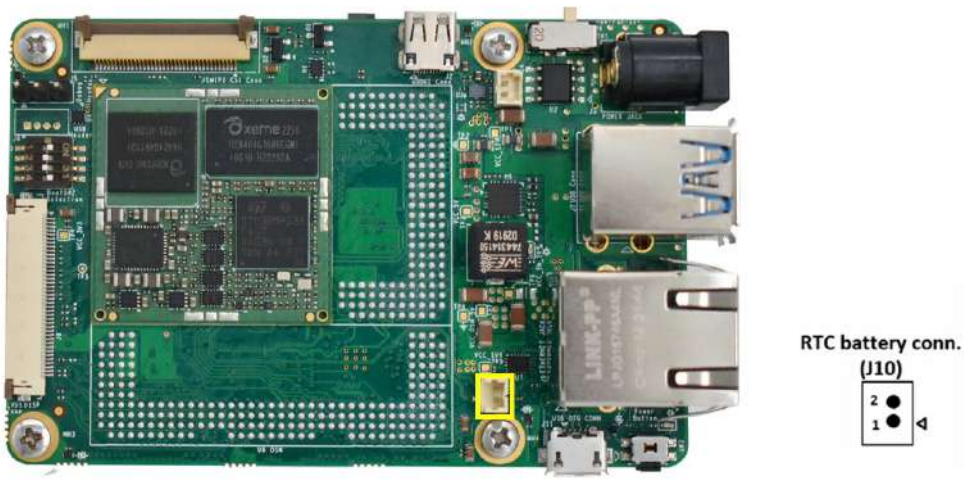

Figure 13: RTC Battery Connector

Number of Pins : 2

Connector Part : 10114829-10102LF from Amphenol ICC (FCI)

Table 11: RTC Battery Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VRTC_3V0	I, Power	+3V Power Input
2	GND	Power	Ground.

Note: Contact iWave support team if External RTC Controller support is required.

2.13.3 Power ON/OFF Switch

The STM32MP135 SBC has power ON/OFF switch (SW1) to control the Main power Input ON/OFF functionality. The Power ON/OFF switch is physically located at the top of the board as shown below.

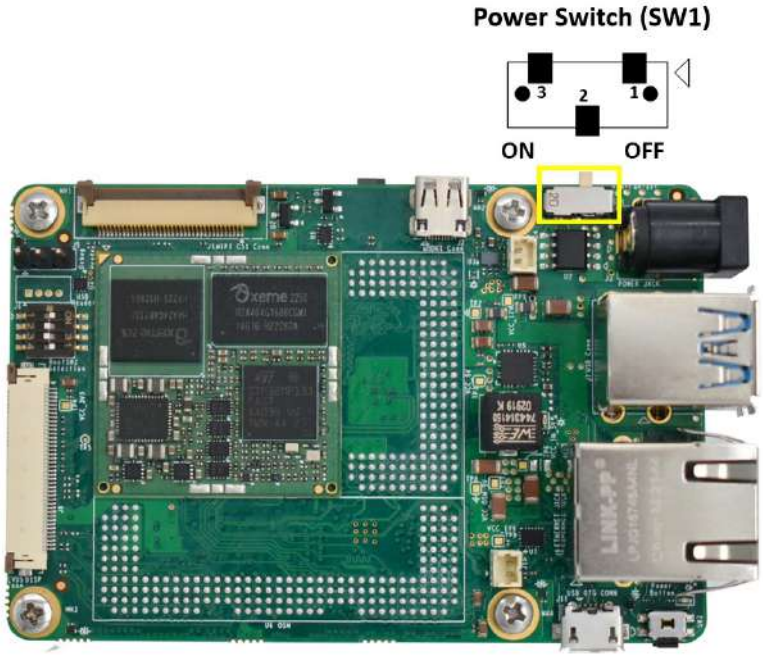

Figure 14: Power ON/OFF Switch

2.13.4 Reset Switch

The STM32MP135 SBC supports Push button switch (SW4) to reset the STM32MP135 CPU. Reset signal is directly connected from Reset Push button switch to the reset signals of SoC and PMIC. This Reset Push button switch is physically located at the bottom of the board as shown below.

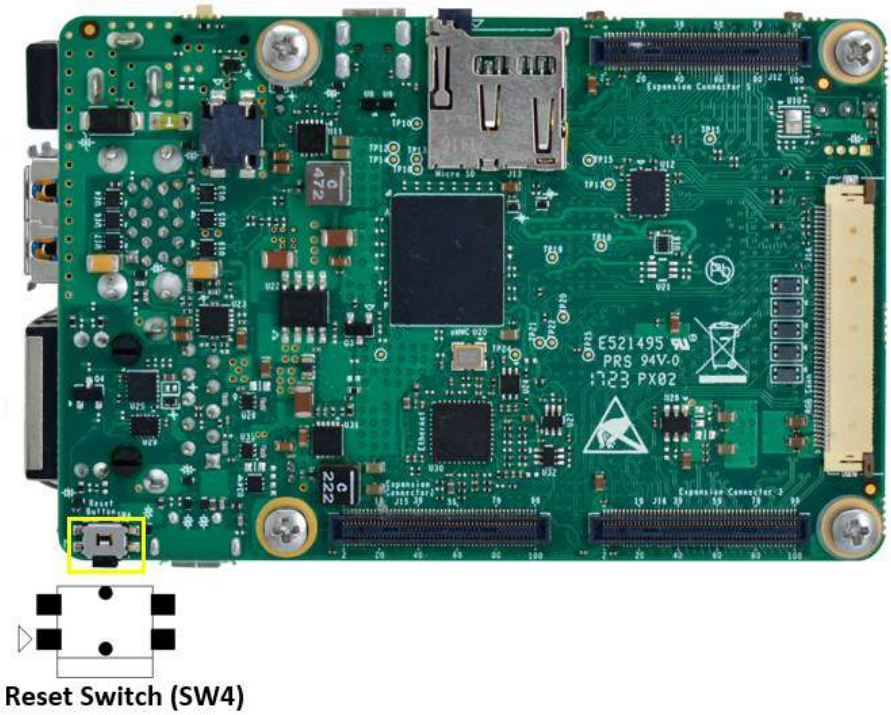

Figure 15: Reset Switch

2.14 STM32MP135 Pin Multiplexing on Expansion Connector

The STM32MP135 SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the STM32MP135 SoC's IO pins can be configured as GPIO if required. The below table provides the details of STM32MP135 SoC pin connections to the expansion connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring STMicroelectronics STM32MP135 Hardware User's Manual.

Important Note:

1. It is strongly recommended to use the pin function same as selected in the SBC for iWave's BSP reusability and to have compatible SBCs in future for upgradability.

Table 12: STM32MP135 SoC IOMUX for Expansion Connector Interfaces

Interface	Expansion Connector - 1 Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
Expansion Connector-1																				
USART1	11	N1		LPTIM2_ETR	TIM4_CH2	TIM8_CH2	SAI1_CK1		SAI1_MCLK_A	USART1_RX		QUADSPI_BK1_IO3		QUADSPI_BK2_IO2(131 &135)	FMC_A18		LTDC_G4			USART1_RX
	9	D2		TIM1_CH2			I2C3_SMBA		DFSDM1_DATIN0	USART1_TX	UART4_TX		FMC_NWAIT			DCMIPP_D0	LTDC_R6			USART1_TX
UART5	20	T3		TIM2_CH1 /TIM2_ETR	SAI1_MCLK_B				DFSDM1_DATIN3	USART2_TX	UART5_RX								ADC1_INP11, ADC1_INN10 , ADC2_INP11, ADC2_INN10	UART5_RX
	18	C4		TIM1_ETR			LPTIM2_IN1				UART5_TX				FMC_D4/FMC_DA4	LTDC_B3	LTDC_R5			UART5_TX
UART8	52	B3							DCMIPP_D12		UART8_RX	FDCAN2_RX		LTDC_B1	FMC_A11	DCMIPP_D1	LTDC_B5			UART8_RX
	54	C3		LPTIM1_IN2							UART8_TX	LTDC_HSYNC		LTDC_R4	FMC_NBL1	DCMIPP_D3	DCMIPP_D12			UART8_TX
	38	F7			TIM4_CH3		I2C3_SDA			USART1_RX	UART8_CTS				FMC_D0/FMC_DA0	DCMIPP_D8	LTDC_R4			UART8_CTS
	40	E2		TIM1_BKIN			SAI1_D4				UART8_DE/UART8_RTS	QUADSPI_BK1_NCS	QUADSPI_BK2_IO2		FMC_D11/FMC_DA11	DCMIPP_D7	LTDC_G0		TAMP_IN6	UART8_RTS
UART7	46	G1				LPTIM2_IN2	I2C4_SMBA			USART3_CTS /USART3_NSS	SPDIFRX_IN0	QUADSPI_BK1_IO2	ETH2_CLK125	LTDC_R7	FMC_A16/FMC_CLE	UART7_RX	DCMIPP_D4			UART7_RX
	44	F8		TIM1_CH1N		DFSDM1_CKIN2		I2C1_SDA		UART7_TX					FMC_D5/FMC_DA5					UART7_TX
	48	G8								USART6_CTS /USART6_NSS	UART7_CTS	QUADSPI_BK1_IO1	ETH2_PHY_INTN	LTDC_B4		DCMIPP_D10	LTDC_B3			UART7_CTS
	50	K2		TIM16_BKIN	SAI1_D3	TIM8_BKIN		SPI5_NSS		USART6_DE/ USART6_RTS	UART7_DE/UART7_RTS	QUADSPI_CLK				DCMIPP_HSYNC	LTDC_B5		TAMP_IN1	UART7_RTS
ETH2	64	H1		TIM17_CH1									ETH2_MDC	LTDC_G4	FMC_A15	DCMIPP_VSYNC	DCMIPP_D3			ETH2_MDC
	62	K3		RTC_OUT2	SAI1_D1			I2S_CKIN	SAI1_SD_A		UART4_RX	QUADSPI_BK1_NCS		ETH2_MDIO	FMC_A6		LTDC_B4		TAMP_IN7	ETH2_MDIO
	96	L1		TIM16_CH1				SPI5_NSS		UART7_RX		QUADSPI_BK1_IO2		ETH2_TX_CTL/ETH2_TX_EN		LTDC_R7	LTDC_G4			ETH2_TX_CTL
	94	J7		TIM17_CH1						UART7_TX	UART4_CTS		ETH1_CLK125	ETH2_TXD0	FMC_A18		LTDC_G2			ETH2_TXD0
	90	R1					SAI2_D3	I2S2_MCK		USART3_TX	UART4_TX		ETH2_TXD1		FMC_A24	DCMIPP_D14	LTDC_B2			ETH2_TXD1
	92	P4		LPTIM1_ETR	TIM4_ETR	SAI2_FS_A	I2C2_SMBA	I2S2_SDI/SPI2_MISO	SAI2_D2			FDCAN2_TX	ETH2_TXD2		FMC_NBL0		LTDC_G7			ETH2_TXD2
	88	R2	RCC_MCO_2	TIM1_BKIN2	SAI2_SCK_B		TIM15_CH2	I2C3_SMBA	SAI1_SCK_B		UART4_DE/UART4_RTS			ETH2_TXD3	FMC_A22	DCMIPP_D7	LTDC_G3			ETH2_TXD3
Expansion Connector-2																				
SPI4	94	B1		TIM1_CH3N				I2S4_CK/SPI4_SCK			UART8_DE/UART8_RTS	LTDC_VSYNC		LTDC_G4	FMC_D9/FMC_DA9	DCMIPP_D11	LTDC_G6	HDP_HDP4		SPI4_SCK
	92	C1		TIM1_CH3			I2C5_SDA	I2S4_SDI/SPI4_MISO						LTDC_B1	FMC_D10/FMC_DA10	DCMIPP_D4	LTDC_R6			SPI4_MISO
	90	C2					I2C5_SCL	I2S4_SDO/SPI4_MOSI			UART4_TX	QUADSPI_BK1_NCS		LTDC_B6	FMC_D3/FMC_DA3	DCMIPP_D13	LTDC_G2			SPI4_MOSI
	86	D3	RTC_REFIN				I2C5_SMBA	I2S4_WS/SPI4_NSS		USART3_CK		LTDC_G5		LTDC_B7	FMC_D15/FMC_DA15	DCMIPP_VSYNC	LTDC_B2			SPI4_NSS
FDCAN2	100	F9	DEBUG_TRACED4	TIM17_BKIN	TIM3_CH2			I2S2_SDI/SPI2_MISO	I2C4_SMBA		SDMMC1_CKIN	FDCAN2_RX		UART5_RX		LTDC_B6	LTDC_DE		DEBUG_TRACED4	FDCAN2_RX
	98	B10	DEBUG_TRACECLK	TIM1_CH1N			LPTIM2_OUT	I2S2_WS/SPI2_NSS	I2C4_SCL		SDMMC1_D123DIR	FDCAN2_TX		UART5_TX		LTDC_CLK			DEBUG_TRACECLK	FDCAN2_TX

Interface	Expansion Connector - 1 Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
Expansion Connector-3																				
SPI1	46	P7			SAI1_CK1	DFSDM1_CKOUT		I2S1_SDI/SPI1_MISO	I2S1_CK/SPI1_SCK		UART5_CTS		SAI1_MCLK_A	ETH1_TX_CLK	ETH2_TX_CLK				ADC1_INP13, ADC1_INN12, TAMP_IN5	SPI1_SCK
	44	R8		TIM1_BKIN	TIM3_CH1	TIM8_BKIN	SAI2_CK2	I2S1_SDI/SPI1_MISO		USART1_CK	UART4_DE/UART4_RTS	TIM13_CH1			SAI2_SCK_A				ADC1_INP17, ADC1_INN16, TAMP_IN2	SPI1_MISO
	38	T4			SAI1_SCK_A		SAI1_CK2	I2S1_MCK	I2S1_SDO/SPI1_MOSI	USART1_TX									ADC1_INP0, ADC1_INN1, ADC2_INP0, ADC2_INN1, TAMP_IN3	SPI1_MOSI
	10	J9						I2S1_WS/SPI1_NSS	SAI1_SD_A		UART4_TX		ETH1_TX_ER	ETH1_CLK125					ADC1_INP6, ADC1_INN2	SPI1_NSS
FDCAN1	11	G5	DEBUG_DBTRGO				I2C2_SDA			USART6_RX	SPDIFRX_IN3	FDCAN1_RX	FMC_NE2		FMC_NCE	DCMIPP_VSYNC				FDCAN1_RX
	13	C7		TIM1_CH2N						UART7_RX		FDCAN1_TX			FMC_D7/FMC_DA7					FDCAN1_TX
SAI1	26	K1		SPI5_MISO	SAI1_D2	DFSDM1_DATIN3	TIM15_CH1N	I2S_CKIN	SAI1_FS_A	UART7_DE/UART7_RTS	UART8_TX	QUADSPI_BK2_NCS	FMC_NCE2		FMC_A25	DCMIPP_D3	LTDC_G7			SAI1_FS_A
		E1			SAI1_MCLK_A				SAI1_CK1			FDCAN1_RX			FMC_D2/FMC_DA2	DCMIPP_D1				SAI1_MCLK_A
	34	G7		USART2_TX	TIM5_CH3	DFSDM1_CKIN1	I2C3_SCL	SPI5_MOSI	SAI1_SCK_A			QUADSPI_BK2_IO2	SAI1_CK2	ETH1_CRS	FMC_A6	DCMIPP_D3				SAI1_SCK_A
	12	M7		TIM2_CH1/TIM2_ETR	USART2_CK	TIM8_CH1N	SAI1_D1	I2S1_WS/SPI1_NSS	SAI1_SD_A				ETH1_PPS_OUT	ETH2_PPS_OUT					ADC1_INP2	SAI1_SD_A
	36	H2						SPI5_SCK	SAI1_SD_B		UART8_CTS	FDCAN1_TX	QUADSPI_BK2_IO1		FMC_NE3	DCMIPP_D2				SAI1_SD_B
ADC	70	L7		TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN		SAI1_SD_B		UART5_TX			ETH1_CRS	ETH2_CRS				ADC1_INP7, ADC1_INN3, ADC2_INP7, ADC2_INN3	ADC2_INN3
	66	L8		USART2_TX	SAI1_D2	DFSDM1_CKIN3			SAI1_FS_A						ETH2_RX_ER				ADC1_INP8, ADC1_INN4, ADC2_INP8, ADC2_INN4	ADC2_INP8
JTAG	62	U4																		DEBUG_JTCK-SWCLK
	64	T13																		DEBUG_JTDI
	60	L12																		DEBUG_JTDO-SWO
	54	R10																		DEBUG_JTRST
I2C3	16	G4		TIM16_CH1	TIM4_CH3		I2C1_SCL	I2C3_SCL	DFSDM1_DATIN1		UART4_RX		SAI1_D1		FMC_D13/FMC_DA13	DCMIPP_D6				I2C3_SCL
	14	B6				DFSDM1_DATIN2	I2C3_SDA		DCMIPP_D8		UART4_RX			LTDC_B4		DCMIPP_D2	DCMIPP_PIXCLK			I2C3_SDA
ETH2	88	H7		SPI5_NSS	TIM5_CH2	SAI2_SD_A		I2S2_WS/SPI2_NSS	I2C4_SCL	USART6_RX		QUADSPI_BK2_IO0		ETH2_REF_CLK/ETH2_RX_CLK	FMC_A12		LTDC_G6			ETH2_RX_CLK
	96	L6		LPTIM1_IN1			SAI2_SCK_A		SAI2_CK2	USART6_DE/USART6_RTS	USART3_CTS		ETH2_PHY_INTN	ETH1_PHY_INTN	ETH2_CRS_DV/ETH2_RX_CTL/ETH2_RX_DV					ETH2_RX_CTL
	100	P3				USART2_RX								ETH2_RXD0	FMC_A4	DCMIPP_D4	LTDC_B6			ETH2_RXD0
	98	N5		TIM1_CH4			I2C5_SCL	I2S2_WS/SPI2_NSS		USART1_CTS/USART1_NSS			ETH2_RXD1	ETH1_CLK		ETH2_CLK				ETH2_RXD1
	94	J6			TIM12_CH1	USART2_CK	I2C5_SDA	I2S2_CK/SPI2_SCK				QUADSPI_BK1_IO2	ETH1_PHY_INTN	ETH1_RX_ER	ETH2_RXD2	QUADSPI_BK1_NCS				ETH2_RXD2
	92	J8	RCC_MCO_1		SAI2_MCLK_A	TIM8_BKIN2	I2C4_SDA	SPI5_MISO	SAI2_CK1	USART1_CK	I2S2_SDO/SPI2_MOSI		USB_OTG_HS_SOF	ETH2_RXD3	FMC_A21		LTDC_B7			ETH2_RXD3

3. TECHNICAL SPECIFICATION

This section provides detailed information about the STM32MP135 SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The STM32MP135 SBC supports 12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Power Input Jack (J3) of STM32MP135 SBC. This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. The Power Jack is physically placed at the top of the board as shown below.

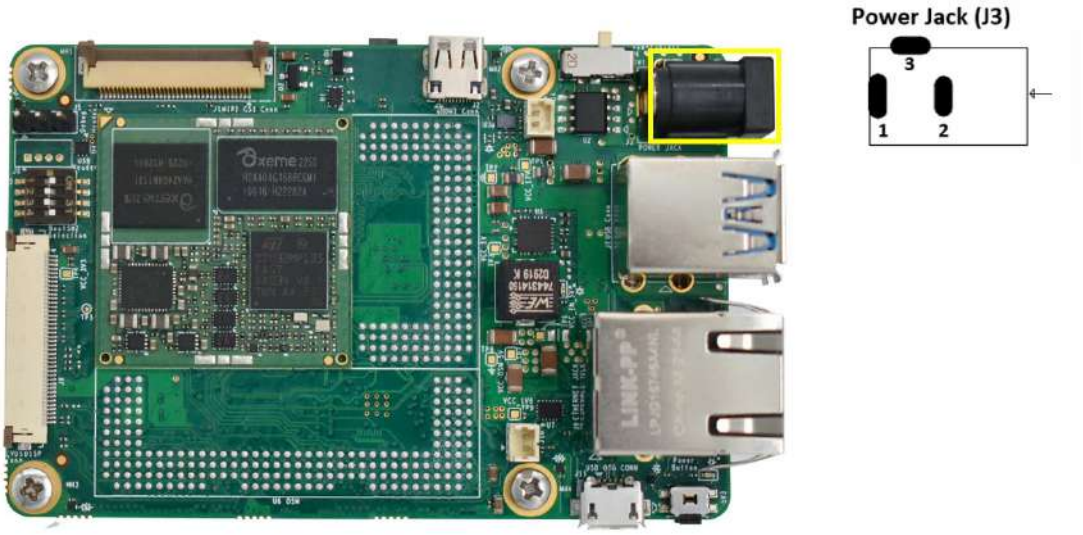

Figure 16: Power Input Jack

Table 13: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[1]	2.8V	3V	3.3V	±20mV

[1] The STM32MP135 SBC uses this voltage as backup power source to SoC VBAT pin when VCC is off.

3.2 Power Consumption

TBD

3.3 EnvironmentalCharacteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of STM32MP135 SBC.

Table 14: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2] For more information on Thermal solution & Heat sink refer the following section.

3.3.2 RoHS Compliance

iWave's STM32MP135 SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's STM32MP135 SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 STM32MP135 SBC Mechanical Dimensions

STM32MP135 SBC PCB size is 85mm x 56mm x 1.2mm. SBC mechanical dimension is shown below. (All dimensions are shown in mm)

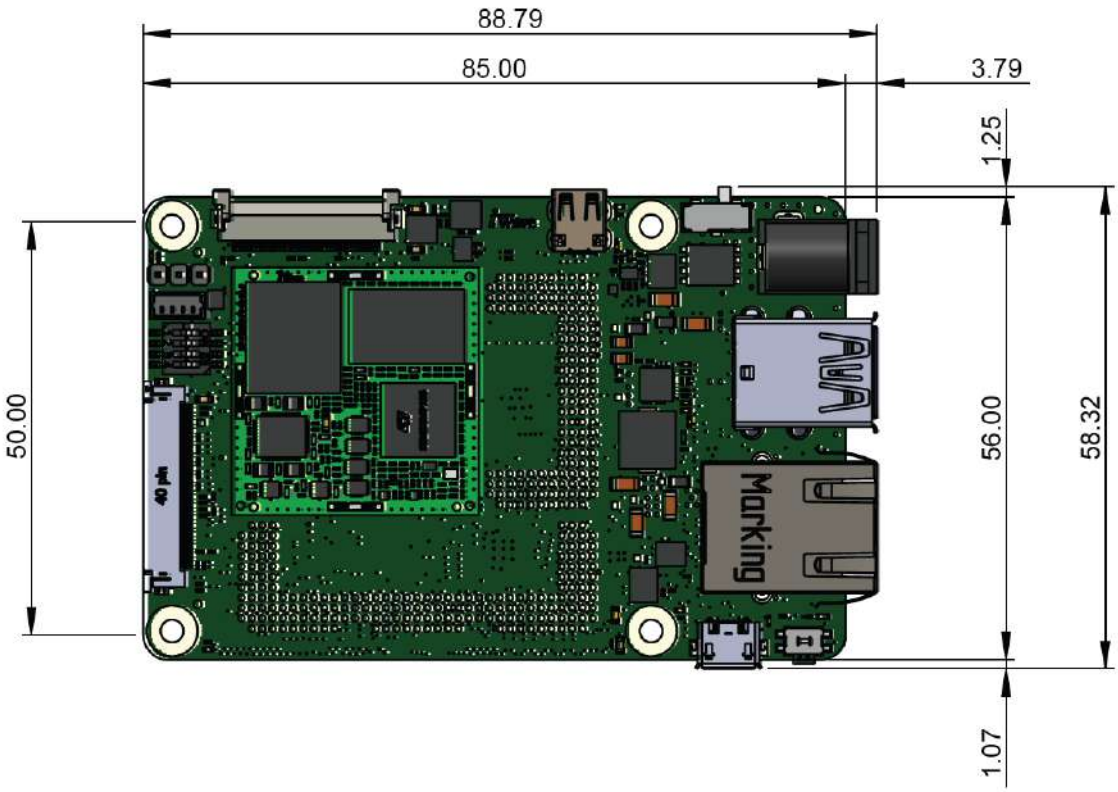

Figure 17: Mechanical Dimensions of STM32MP135 SBC Top View

The STM32MP135 SBC PCB thickness is 1.2mm±0.15mm, top side maximum height component is 16.40mm (Dual Stack USB Connector), followed by Ethernet Connector. In bottom side maximum height component is a common mode choke(3.90mm) followed by an inductor (3.50mm).

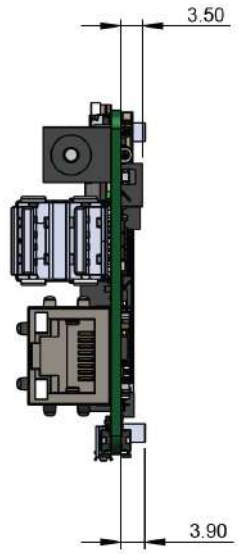

Figure 18: Mechanical Dimensions of STM32MP135 SBC Side View-1

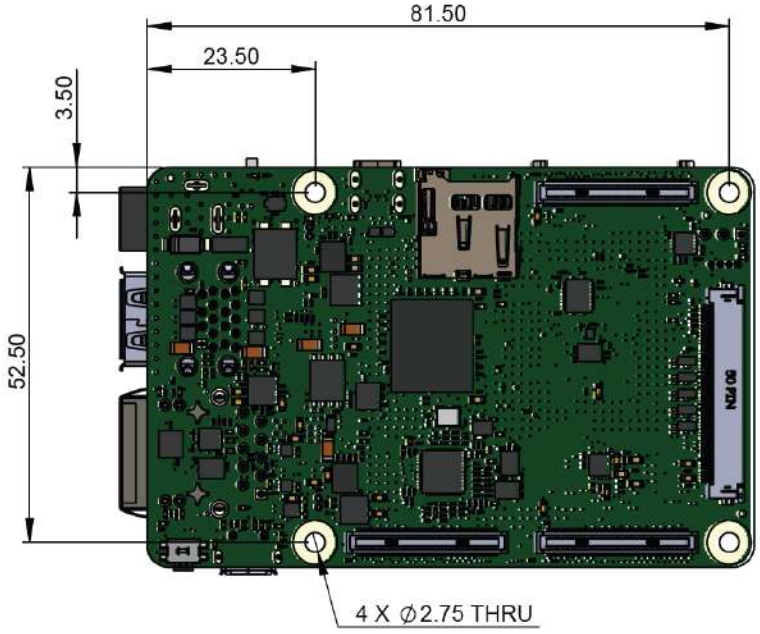

Figure 19: Mechanical Dimensions of STM32MP135 SBC Bottom View

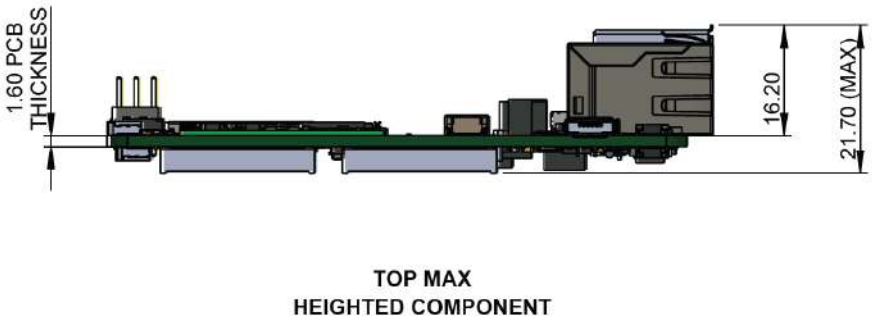

Figure 20: Mechanical Dimensions of STM32MP135 SBC Side View-2

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different STM32MP135 SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 15: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G54S – STM32MP135 SBC		
iW-G54S-OS35-3D512M-E004G-BIA-PP	STM32MP135, DDR3L – 512MB, eMMC 4GB	-40°C to 85°C

Important Note: Some of the above-mentioned Part Numbers are subject to MOQ purchase. Please contact iWave for further details.

For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.