iW-RainboW-G54M

STM32MP135 OSM Size - S

Data Sheet

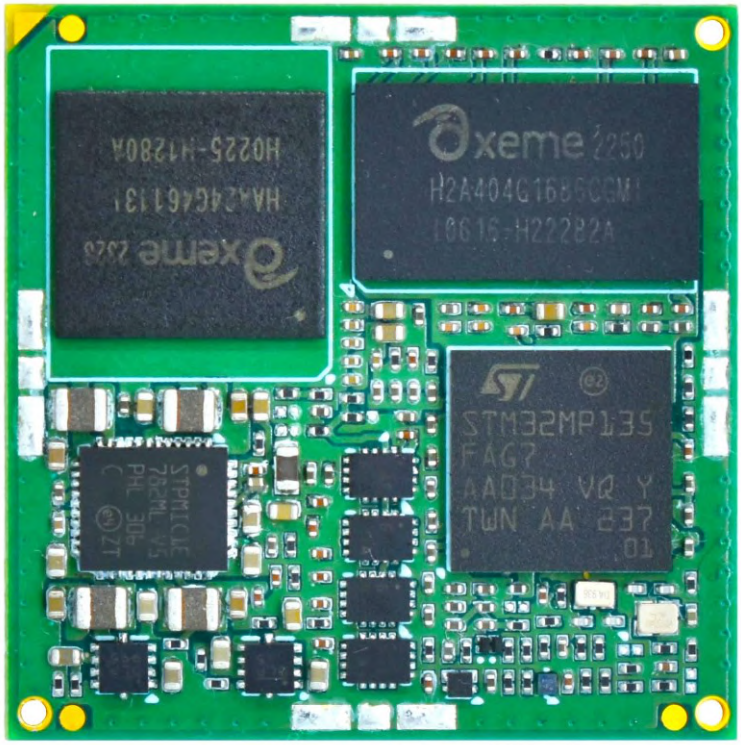

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Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the Hardware Data sheet for the STMicroelectronics's STM32MP135 MPU based OSM v1.1 specification compatible Size-S LGA module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the STM32MP135 OSM Module from a Hardware Systems perspective.

1.2 OSM LGA Module Overview

The OSM V1.1 ("Open Standard Modules™") is a future proof and versatile standard for small size, low-cost embedded computer modules. Combining the following key characteristics like completely machine processible during soldering, assembly and testing, Pre-tinned LGA package in different possible packages for direct PCB soldering without connector.

The OSM Module definition targets application that requires low power, low cost, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as Audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

STMicroelectronics's STM32MP135 MPU based OSM LGA Module is rich with STM32MP135 features along with on Module DDR3L, eMMC and comes in the OSM form factor of 30mm x 30mm form factor (Size-SF). The Module PCB has 332 contacts which can be mounted as LGA on an OSM Carrier Card.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
CAN	Controller Area Network
CPU	Central Processing Unit
CTS	Clear to Send
DDR	Double Data Rate
EMS	Electronics manufacturing services
FLEXCAN	Flexible Control Area Network
GB	Giga Byte

Acronyms	Abbreviations
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
FDCAN	Flexible Controller Area Network
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
MHz	Mega Hertz
MPU	Micro Processor Unit
OSM	Open Standard Module
OTG	On-The-Go
PCB	Printed Circuit Board
SDMMC	Secure Digital and Multimedia Card
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
QSPI	Quad Serial Peripheral Interface

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
USB	Universal Serial Bus
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin

Terminology	Description
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-OSM.

1.5 References

- STM32MP135_Datasheet.pdf
- STM32MP13_RM.pdf
- OSM Hardware Specification V1.1
- OSM Design Guide 1.0

1.6 Important Note

In this document, wherever STM32MP135 SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ETH1_RGMII_TXC

  In this signal, ***ETH1_RGMII_TXC*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about STM32MP135 OSM LGA Module and Hardware architecture with high level block diagram.

2.1 STM32MP135 OSM LGA Module Block Diagram

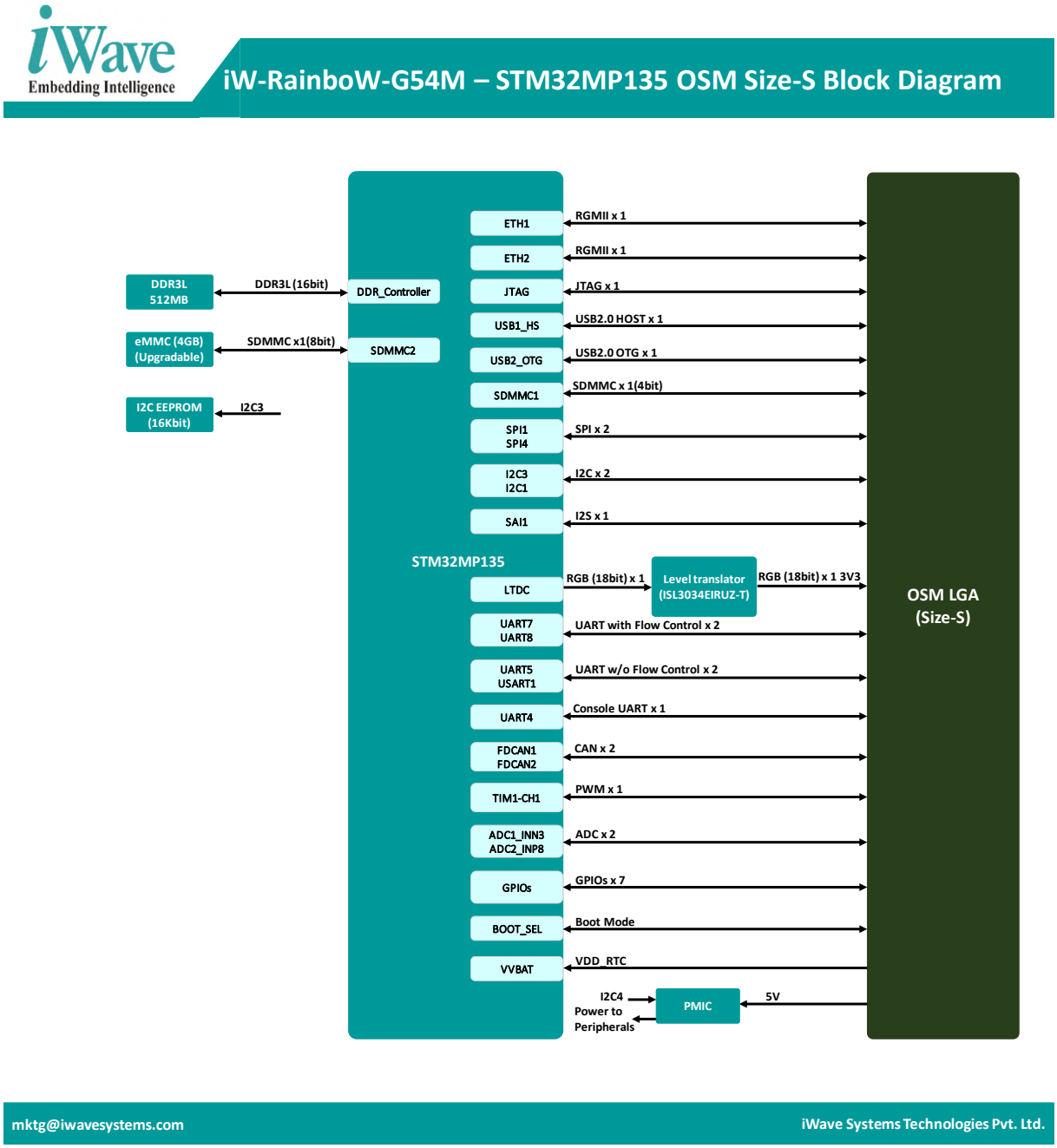

Figure 1: STM32MP135 OSM LGA Module Block Diagram

2.2 STM32MP135 OSM Features

STM32MP135 OSM LGA Module supports the following features.

SoC

- STM32MP135 Applications Processor
    - STM32MP135: Cortex®-A7@upto 1 GHz

Power

- STPMIC1EPQR

Memory

- DDR3L – 512MB (Expandable upto 1GB) [1]
- eMMC – 4GB (Expandable upto 128GB)[1]
- EEPROM – 16Kbit

OSM LGA Interfaces

- RGMII x 1
- 18 bit RGB X 1
- USB 2.0 OTG x 1
- USB 2.0 Host x 1
- SDMMC 4bit x 1
- CAN x 2
- SPI x 2
- Data UART (without CTS & RTS) x 2
- Data UART (with CTS & RTS) x 2
- Debug Console UART x 1
- PWM x 1
- ADC x 2
- I2S x 1
- JTAG x 1
- GPIOs x 7

General Specification

- Power Supply : 5V, 2A
- Form Factor : OSM Size-SF - 30mm X 30mm (OSM V1.1 Specification)

1. *Memory Size will differ based on iWave's Module Product Part Number. Contact iWave to customise the eMMC and DDR3L size.*

2.3 STM32MP135 MPU

iW-RainboW-G54M Size-S OSM LGA Module supports STM32MP135 series MPUs from STMicroelectronics.

STM32MP135: Cortex®-A7 up to 1 GHz, 30 Communication peripherals including CAN, Ethernet 2 and camera interface.

The STM32MP135C/F devices are based on the high-performance Arm® Cortex®-A7 32-bit RISC core operating at up to 1 GHz and supports Memory interfaces including DDR3L, eMMC and a wide range of peripheral I/Os.

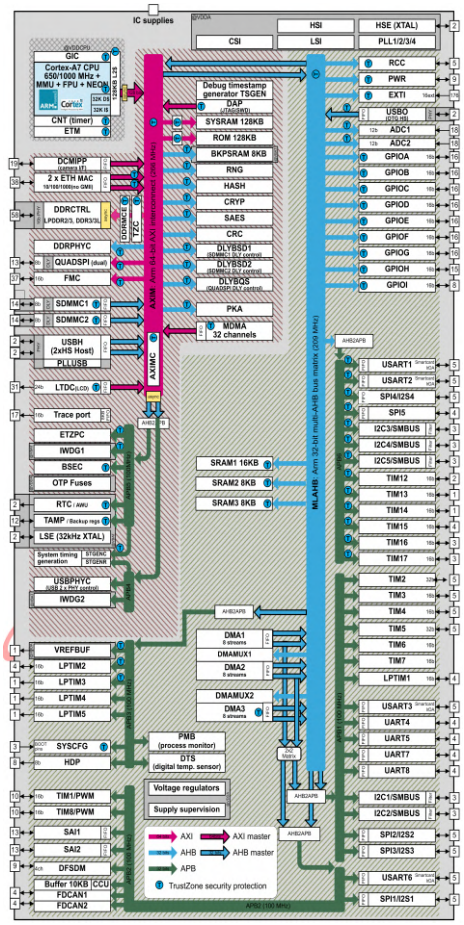

Figure 2: STM32MP135 Block Diagram

Note: The STM32MP135 processor offers numerous advanced features, please refer the latest STM32MP135 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 STPMIC1EPQR PMIC

The STM32MP13x OSM LGA Module uses STPMIC1EPQR (U5) for module power management. The STPMIC1EPQR features six LDOs, four buck and one boost regulator. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory that stores the key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The STPMIC1 comes in 44 pin WFQFN (5x6) Package and is placed on the Top side of the Module.

2.5 Memory

2.5.1 DDR3L

The STM32MP135 OSM LGA Module supports upto 1GB DDR3L SDRAM memory by using 16bit DDR channel of STM32MP135 MPU at 533MHz frequency. DDR3L part U1 is placed on Top side of the Module. The memory size in default configuration is 5132MB. To customize the DDR3L memory size, contact iWave.

2.5.2 eMMC

The STM32MP135 OSM LGA Module supports 4GB eMMC as default boot and storage device. This is directly connected to SDMMC2 controller of the STM32MP135 SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory (U2) is physically located on top side of the SOM. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 EEPROM

The STM32MP135 OSM LGA Module supports 16KBit EEPROM making use of the M24C16-DFCU6TP/K EEPROM from ST Microelectronics. It is connected to the MPU making use of using I2C3. This EEPROM which can be used for storing system specific data and is placed on the Top side of the board (U11).

2.6 OSM LGA

OSM LGA has standard pinout as per OSM Specification V1.1 The interfaces which are available at 332 contacts are explained in the following sections.

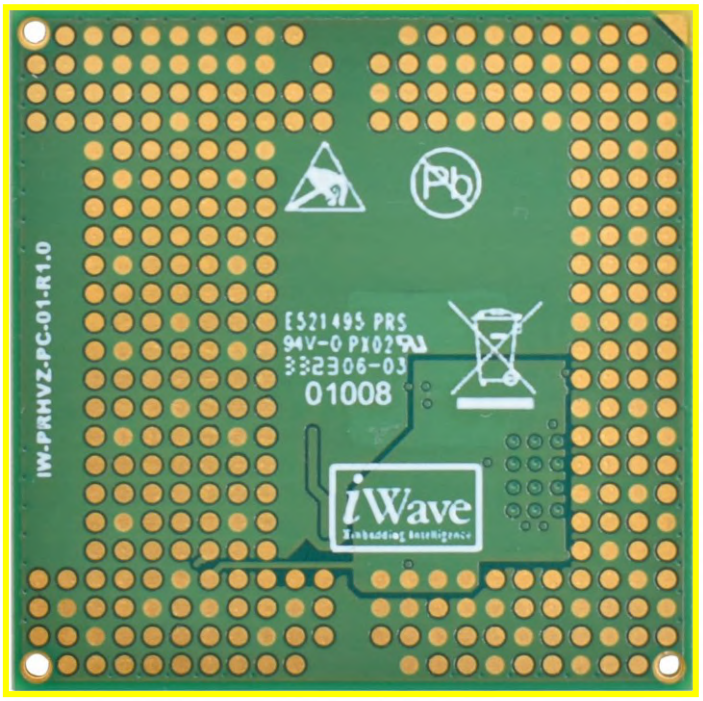

Figure 3: OSM LGA

Number of contacts - : 332

Table 3: OSM Pinouts

OSM Pins	Signal
SIZE 0	
M18	ADC2_INP3(PA0)
N18	ADC2_INP8(PF11)
U19	BOOT_SEL1
R18	BOOT_SEL2
AB17	FDCAN1_RX(PG9)
AC17	FDCAN1_TX(PE10)
AB19	FDCAN2_RX(PB5)
AC19	FDCAN2_TX(PB13)
V17	CARRIER_PWR_EN
A15	GND
A16	NA
A17	GND
A18	GND
A19	GND
A20	NA
A21	GND
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
C15	NA
C17	NA
C19	NA
C21	NA
AC18	NA
F15	NA
E16	NA
R15	ETH1_RGMII_ RX_CLK(PD7)
M15	ETH1_RGMII_ RX_CTL(PA7)
L16	NA
N15	ETH1_RGMII_ RXD2(PB0)
P15	ETH1_RGMII_ RXD3(PB1)
J15	ETH1_RGMII_ GTX_CLK(PC1)
K16	ETH1_RGMII_ TX_CTL(PB11)
K15	ETH1_RGMII_ RXD0(PC4)
L15	ETH1_RGMII_ RXD1(PC5)

OSM Pins	Signal
H15	ETH1_RGMII_ TXD0(PG13)
G15	ETH1_RGMII_ TXD1(PG14)
H16	ETH1_RGMII_ TXD2(PC2)
G16	ETH1_RGMII_ TXD3(PE5)
N16	VDDQ_DDR_1V35
M17	VDD_1V8
T16	ETH1_MDC(PG2)
T15	ETH1_MDIO(PA2)
T17	FORCE_RECOV#
F16	GND
J16	GND
J20	GND
E21	GND
E15	GND
M16	GND
M20	GND
P18	GND
R16	GND
R20	GND
V16	GND
V20	GND
Y18	GND
AA14	GND
AA17	GND
AA19	GND
AA22	GND
AB15	GND
AB21	GND
D18	GND
L18	GND
F20	GND
D17	OSM_GPIO_A_0(PB10)
E17	OSM_GPIO_A_1(PE11)
F17	OSM_GPIO_A_2(PH2)
G17	OSM_GPIO_A_3(PI3)
H17	OSM_GPIO_A_4(PA14)
J17	OSM_GPIO_A_5(PA13)
K17	OSM_GPIO_A_6(PI1)
L17	NA
D19	NA
E19	NA

OSM Pins	Signal
F19	NA
G19	NA
H19	NA
J19	NA
K19	NA
L19	NA
AA15	I2C3_SCL(PB8)
AA16	I2C3_SDA(PH14)
AA20	I2C1_SCL(PD12)
AA21	I2C1_SDA(PD3)
V21	SAI1_SD_B(PG10)
W21	SAI1_SD_A(PA5)
V19	NA
W19	NA
W20	SAI1_SCK_A(PH12)
W18	SAI1_FS_A(PE4)
V18	SAI1_MCLK_A(PD0)
R19	JTAG_NJTRST
P19	NA
N17	JTAG_TCK
P17	JTAG_TDI
R17	JTAG_TDO
N19	JTAG_TMS
E18	TIM1_CH1(PF9)
F18	NA
G18	NA
H18	NA
J18	NA
K18	NA
T18	NA
T19	NA
Y13	NA
Y14	NA
AA13	NA
W17	VDD_RTC
J21	SDMMC1_CD_B(PE2)
F21	SDMMC1_CK(PC12)
E20	SDMMC1_CMD(PD2)
G20	SDMMC1_D0(PC8)
G21	SDMMC1_D1(PC9)
H20	SDMMC1_D2(PC10)

OSM Pins	Signal
H21	SDMMC1_D3(PC11)
C20	VDD_SD1
D21	NA
D20	NA
T21	NA
K20	NA
K21	NA
L20	NA
L21	NA
M21	NA
N20	NA
N21	NA
P20	NA
P21	NA
R21	NA
T20	NA
U21	NA
U20	NA
W15	NA
W16	NA
Y15	SPI1_NSS(PF12)
U16	SPI1_SCK(PC3)
U15	SPI1_MISO(PA6)
V15	SPI1_MOSI(PC0)
AA23	SPI4_NSS(PD10)
Y21	SPI4_SCK(PE12)
Y22	SPI4_MISO(PE13)
Y23	SPI4_MOSI(PD1)
U17	NRST
C18	NA
C14	UART7_CTS(PG15)
C13	UART7_RTS(PF10)
A14	UART7_RX(PD11)
B13	UART7_TX(PE8)
D16	UART8_CTS(PD14)
D15	UART8_RTS(PE14)
D14	UART8_RX(PE0)
D13	UART8_TX(PE1)
A22	UART5_RX(PF13)
B23	UART5_TX(PE7)
D22	UART4_RX(PD8)

OSM Pins	Signal
D23	UART4_TX(PD6)
C22	USART1_RX(PD13)
C23	USART1_TX(PA9)
AB13	USB_OTG_DM2
AC14	USB_OTG_DP2
AC16	USB_OTG_PWR_EN_GPIO(PA3)
AB14	USB_OTG_HS_ID(PA10)
AC15	USB_OTG_OC_GPIO
AB16	VBUS_USBA
AB23	USB_DM1
AC22	USB_DP1
AC20	USB_B_EN
AB22	USB_HS_ID
AC21	USB_HS_OC_GPIO
AB20	USB_B_VBUS
AB18	V_BAT
AA18	V_BAT
M19	VDDCORE_1V25
Y16	VDD_1V8
Y20	VDD_ADC
Y19	VCC_IN_3V3
Y17	VCC_IN_5V
U18	VCC_OUT_IO
B22	PWR_CPU_ON
C16	PWR_LP
P16	NA
SIZE S	
C2	NA
G3	NA
G4	NA
B3	NA
B4	NA
C1	NA
B1	NA
A2	NA
A3	NA
A5	NA
A6	NA
B6	NA
B7	NA
AB8	NA

OSM Pins	Signal
AB7	NA
AB11	NA
AB10	NA
AC9	NA
AC8	NA
AC6	NA
AC5	NA
AB5	NA
AB4	NA
AA3	NA
E1	NA
D2	NA
P1	ETH2_RGMII_ RX_CLK(PH11)
L1	ETH2_RGMII_ RX_CTL(PG12)
K2	NA
M1	ETH2_RGMII_ RXD2(PH6)
N1	ETH2_RGMII_ RXD3(PA8)
H1	ETH2_RGMII_ GTX_CLK(PG3)
J2	ETH2_RGMII_ TX_CTL(PF6)
J1	ETH2_RGMII_ RXD0(PF4)
K1	ETH2_RGMII_ RXD1(PA11)
G1	ETH2_RGMII_ TXD0(PF7)
F1	ETH2_RGMII_ TXD1(PG11)
G2	ETH2_RGMII_ TXD2(PG1)
F2	ETH2_RGMII_ TXD3(PE6)
C6	ETH2_MDC(PG5)
C7	ETH2_MDIO(PB2)
M2	NA
B5	GND
D8	GND
P4	GND
AC10	GND
AC7	GND
AC4	GND
AB9	GND
AB6	GND
AB3	GND
AA11	GND
AA10	GND
AA8	GND
A4	GND

OSM Pins	Signal
A7	GND
A10	GND
B2	GND
B8	GND
B9	GND
C11	GND
D1	GND
D5	GND
E2	GND
H2	GND
H4	GND
L2	GND
L4	GND
P2	GND
U2	GND
U4	GND
V1	GND
W3	GND
Y2	GND
AA1	GND
AA4	GND
AA7	GND
R1	GND
D3	NA
D4	NA
E3	NA
E4	NA
F3	RGB_DISP_EN(PI2)
F4	RGB_BL_EN(PI0)
C4	NA
C3	NA
AB2	NA
AB1	NA
AC3	NA
AC2	NA
V2	NA
W2	NA
Y1	NA
W1	NA
R2	NA
T1	NA

OSM Pins	Signal
U1	NA
T2	NA
AA9	PONKEYN
M4	RGB_LTDC_CLK(PD9)3V3
R4	RGB_D12_LTDC_B2(PH7)3V3
R3	RGB_D13_LTDC_B3(PF2)3V3
P3	RGB_D14_LTDC_B4(PH3)3V3
N3	RGB_D15_LTDC_B5(PD15)3V3
N4	RGB_D16_LTDC_B6(PB6)3V3
M3	RGB_D17_LTDC_B7(PF1)3V3
H3	NA
J4	RGB_LTDC_DE(PH9)3V3
K4	NA
W4	RGB_D6_LTDC_G2(PH13)3V3
V3	RGB_D7_LTDC_G3(PF3)3V3
V4	RGB_D8_LTDC_G4(PD5)3V3
U3	RGB_D9_LTDC_G5(PG0)3V3
T3	RGB_D10_LTDC_G6(PA12)3V3
T4	RGB_D11_LTDC_G7(PA15)3V3
K3	RGB_LTDC_HSYNC(PH10)3V3
Y7	RGB_D0_LTDC_R2(PG7)3V3
AA6	RGB_D1_LTDC_R3(PB12)3V3
Y6	RGB_D2_LTDC_R4(PD4)3V3
AA5	RGB_D3_LTDC_R5(PF5)3V3
Y5	RGB_D4_LTDC_R6(PH8)3V3
Y4	RGB_D5_LTDC_R7(PE9)3V3
J3	RGB_RESET(PG8)3V3
L3	RGB_LTDC_VSYNC(PG4)3V3
AA2	NA
N2	NA
D11	NA
D10	NA
C10	NA
D9	NA
C8	NA
B11	NA
B10	NA
A9	NA
A8	NA
C9	NA
Y3	VDDCPU_1V35

OSM Pins	Signal
C5	VCC_1V8
Y11	VCC_IN_5V
Y10	VCC_IN_5V
Y9	VCC_IN_5V
Y8	VCC_IN_5V
D6	NA
D7	NA

2.6.1 RGMII Interface

The STM32MP135 Size-S OSM LGA Module supports two RGMII interface on OSM LGA. Using the two ethernet controllers ETH0 and ETH1 with TSN support. The IO level of the RGMII lanes is fixed at 1.8V in the module and the same needs to be taken care of in the Carrier Board. The PHY can be selected which operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s as per the requirement off the Module.

For more details on ETH1 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
H15	ETH_A_(S)(R)(G)MII_TXD0	ETH1_RGMII_TXD0(PG13)	PG13/R9	O, 1.8V CMOS	Transmit data bit 0 (transmitted first) port A.
G15	ETH_A_(S)(R)(G)MII_TXD1	ETH1_RGMII_TXD1(PG14)	PG14/T8	O, 1.8V CMOS	Transmit data bit 1 port A.
H16	ETH_A_(S)(R)(G)MII_TXD2	ETH1_RGMII_TXD2(PC2)	PC2/U8	O, 1.8V CMOS	Transmit data bit 2 port A.
G16	ETH_A_(S)(R)(G)MII_TXD3	ETH1_RGMII_TXD3(PE5)	PE5/L9	O, 1.8V CMOS	Transmit data bit 3 port A.
K16	ETH_A_(R)(G)MII_TX_EN(_ER)	ETH1_RGMII_TX_CTL(PB11)	PB11/M6	O, 1.8V CMOS	Transmit enable (Error) port A.
J15	ETH_A_(R)(G)MII_TX_CLK	ETH1_RGMII_GTX_CLK(PC1)	PC1/R7	I/O, 1.8V CMOS	Transmit clock port A.
K15	ETH_A_(S)(R)(G)MII_RXD0	ETH1_RGMII_RXD0(PC4)	PC4/K9	I, 1.8V CMOS	Receive data bit 0 (received first) port A.
L15	ETH_A_(S)(R)(G)MII_RXD1	ETH1_RGMII_RXD1(PC5)	PC5/P8	I, 1.8V CMOS	Receive data bit 1 port A.
N15	ETH_A_(R)(G)MII_RXD2	ETH1_RGMII_RXD2(PB0)	PB0/M8	I, 1.8V CMOS	Receive data bit 2 port A.
P15	ETH_A_(R)(G)MII_RXD3	ETH1_RGMII_RXD3(PB1)	PB1/N8	I, 1.8V CMOS	Receive data bit 3 port A.
M15	ETH_A_(R)(G)MII_RX_DV(_ER)	ETH1_RGMII_RX_CTL(PA7)	PA7/R6	I, 1.8V CMOS	Receive data valid port A.
R15	ETH_A_(R)(G)MII_RX_CLK	ETH1_RGMII_RX_CLK(PD7)	PD7/R3	I/O, 1.8V CMOS	Receive clock port A.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
T15	ETH_MDIO	ETH1_MDIO(PA2)	PA2/R5	I/O, 1.8V CMOS	Management bus data signal for Ethernet.
T16	ETH_MDC	ETH1_MDC(PG2)	PG2/U3	O, 1.8V CMOS	Management bus clock signal for Ethernet.

For more details on ETH2 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
G1	ETH_B_(S)(R)(G)MII_TXD0	ETH2_RGMII_TXD0(PF7)	PF7/ J7	O, 1.8V CMOS	Transmit data bit 0 (transmitted first) port b.
F1	ETH_B_(S)(R)(G)MII_TXD1	ETH2_RGMII_TXD1(PG11)	PG11/R1	O, 1.8V CMOS	Transmit data bit 1 port A.
G2	ETH_B_(S)(R)(G)MII_TXD2	ETH2_RGMII_TXD2(PG1)	PG1/P4	O, 1.8V CMOS	Transmit data bit 2 port A.
F2	ETH_B_(S)(R)(G)MII_TXD3	ETH2_RGMII_TXD3(PE6)	PE6/ R2	O, 1.8V CMOS	Transmit data bit 3 port A.
J2	ETH_B_(R)(G)MII_TX_EN(_ER)	ETH2_RGMII_TX_CTL(PF6)	PF6/ L1	O, 1.8V CMOS	Transmit enable (Error) port A.
H1	ETH_B_(R)(G)MII_TX_CLK	ETH2_RGMII_GTX_CLK(PG3)	PG3/ U2	I/O, 1.8V CMOS	Transmit clock port A.
J1	ETH_B_(S)(R)(G)MII_RXD0	ETH2_RGMII_RXD0(PF4)	PF4/ P3	I, 1.8V CMOS	Receive data bit 0 (received first) port A.
K1	ETH_B_(S)(R)(G)MII_RXD1	ETH2_RGMII_RXD1(PA11)	PA11/ N5	I, 1.8V CMOS	Receive data bit 1 port A.
M1	ETH_B_(R)(G)MII_RXD2	ETH2_RGMII_RXD2(PH6)	PH6/ J6	I, 1.8V CMOS	Receive data bit 2 port A.
N1	ETH_B_(R)(G)MII_RXD3	ETH2_RGMII_RXD3(PA8)	PA8/ J8	I, 1.8V CMOS	Receive data bit 3 port A.
L1	ETH_B_(R)(G)MII_RX_DV(_ER)	ETH2_RGMII_RX_CTL(PG12)	PG12/ L6	I, 1.8V CMOS	Receive data valid port A.
P1	ETH_B_(R)(G)MII_RX_CLK	ETH2_RGMII_RX_CLK(PH11)	PH11/ H7	I/O, 1.8V CMOS	Receive clock port A.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
C7	ETH_B_MDIO	ETH2_MDIO(PB2)	PB2/ K3	I/O, 1.8V CMOS	Management bus data signal for Ethernet.
C6	ETH_B_MDC	ETH2_MDC(PG5)	PG5/ H1	O, 1.8V CMOS	Management bus clock signal for Ethernet.

2.6.2 USB 2.0 OTG & Host Interface

The STM32MP135 Size-S OSM LGA Module supports one USB2.0 OTG interface and one USB2.0 Host interface.

STM32MP135 MPU supports two USB2.0 controllers supporting two independent USB core and includes the PHY and I/O interfaces to support this operation. The USB2 controller of the STM32MP135 MPU supports OTG operation and is connected to the USB_A port of OSM, while the USB1 controller of the STM32MP135 MPU supports only Host operation and is connected to the USB_B port of OSM. Both controllers support High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps). The USB2 controller of the MPU i.e., USB_A of the OSM supports USB On-The-Go supplement to the USB 2.0 specification. For both the USB ports, to support Power enable Over Current functionality, GPIOs are connected to the specified OSM pins.

For more details on USB2.0 OTG pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB13	USB_A_D_N	USB_OTG_DM2	USB_DM2/U9	I/O, USB	USB2.0 Port0 Data Negative.
AC14	USB_A_D_P	USB_OTG_DP2	USB_DP2/T9	I/O, USB	USB2.0 Port0 Data Positive.
AB14	USB_A_ID	USB_OTG_HS_ID(PA10)	PA10/J12	I OD, 1.8V CMOS/ 10K PU	USB OTG ID.
AC15	USB_A_OC#	NA	NA	1.8V CMOS/ 10K PU	The pin is by default pulled up in the module.
AB16	USB_A_VBUS	VBUS_USBA	PI7/USB_OTG_ HS_VBUS/U13	I USB VBUS 5V	USB Port0 Power detection.
AC16	USB_A_EN	USB_OTG_PWR_ EN_GPIO(PA3)	PA3/T7	O, 1.8V CMOS	USB Power enable.

For more details on USB 2.0 Host pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB23	USB_B_D_N	USB_DM1	USB_DM1/U12	I/O, USB	USB2.0 Port1 Data Negative.
AC22	USB_B_D_P	USB_DP1	USB_DP1/T12	I/O, USB	USB2.0 Port1 Data Positive.
AB22	USB_B_ID	NA	NA	I OD, 1.8V CMOS/ 10K PU	The pin is by default pulled up in the module.
AC21	USB_B_OC#	NA	NA	1.8V CMOS/ 10K PU	The pin is by default pulled up in the module.
AC20	USB_B_EN	USB_B_EN	NA	1.8V CMOS/ 10K PU	The pin is by default pulled up in the module.

2.6.3 Audio Interface

The STM32MP135 Size-S OSM LGA Module supports one I2S using the SAI1 controllers of the MPU. The SAI controllers can be configured as Master or Slave and has independent Frame, Bit & Master clocks. To bring flexibility and reconfigurability, each SAI contains two independent audio sub-blocks. Each block has its own clock generator and I/O line controller. Audio sampling frequencies up to 192 kHz are supported.

In STM32MP135 OSM LGA Module the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync. As the OSM supports common Frame, Bit and Master clocks for both the I2S.

For pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
V18	I2S_MCLK	SAI1_MCLK_A(PD0)	PD0/E1	O, 1.8V CMOS	Master Clock output for channel1.
W18	I2S_LRCLK	SAI1_FS_A(PE4)	PE4/K1	O, 1.8V CMOS	I2s channel1 Left Right Synchronization Clock.
W20	I2S_BITCLK	SAI1_SCK_A(PH12)	PH12/G7	O, 1.8V CMOS	I2S Channel1 Digital Audio Clock.
V21	I2S_A_DATA_IN	SAI1_SD_B(PG10)	PG10/H2	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Input.
W21	I2S_A_DATA_OUT	SAI1_SD_A(PA5)	PA5/ M7	O, 1.8V CMOS	Serial Audio Interface Channel1 Data output.

2.6.4 RGB

The STM32MP135 Size-S OSM Module can support 18bit RGB display interface with a maximum resolution of WXGA (1366 × 768) @60 fps or up to Full HD (1920 x 1080) @ 30 fps. The 18bit RGB signals are connected to the RGB pins of the OSM.

For more details on RGB Signals pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M4	RGB_(PIXEL)CLK	RGB_LTDC_CLK(PD9)3V3	PD9/B5	O, 3.3V CMOS	Pixel clock signal
R4	RGB_B0	RGB_D12_LTDC_B2(PH7)3V3	PH7/ L3	O, 3.3V CMOS	Blue data bit 0
R3	RGB_B1	RGB_D13_LTDC_B3(PF2)3V3	PF2/ B7	O, 3.3V CMOS	Blue data bit 1
P3	RGB_B2	RGB_D14_LTDC_B4(PH3)3V3	PH3/ T2	O, 3.3V CMOS	Blue data bit 2
N3	RGB_B3	RGB_D15_LTDC_B5(PD15)3V3	PD15/A5	O, 3.3V CMOS	Blue data bit 3

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
N4	RGB_B4	RGB_D16_LTDC_B6(PB6)3V3	PB6/ G3	O, 3.3V CMOS	Blue data bit 4
M3	RGB_B5	RGB_D17_LTDC_B7(PF1)3V3	PF1/A8	O, 3.3V CMOS	Blue data bit 5
J4	RGB_DE	RGB_LTDC_DE(PH9)3V3	PH9/ D9	O, 3.3V CMOS	Data Enable
W4	RGB_G0	RGB_D6_LTDC_G2(PH13)3V3	PH13/E9	O, 3.3V CMOS	Green data bit 0
V3	RGB_G1	RGB_D7_LTDC_G3(PF3)3V3	PF3/ B9	O, 3.3V CMOS	Green data bit 1
V4	RGB_G2	RGB_D8_LTDC_G4(PD5)3V3	PD5/ B4	O, 3.3V CMOS	Green data bit 2
U3	RGB_G3	RGB_D9_LTDC_G5(PG0)3V3	PG0/ A4	O, 3.3V CMOS	Green data bit 3
T3	RGB_G4	RGB_D10_LTDC_G6(PA12)3V3	PA12/ F2	O, 3.3V CMOS	Green data bit 4
T4	RGB_G5	RGB_D11_LTDC_G7(PA15)3V3	PA15/ E7	O, 3.3V CMOS	Green data bit 5
K3	RGB_HSYNC	RGB_LTDC_HSYNC(PH10)3V3	PH10/ C11	O, 3.3V CMOS	Horizontal sync
Y7	RGB_R0	RGB_D0_LTDC_R2(PG7)3V3	PG7/ C8	O, 3.3V CMOS	Red data bit 0
AA6	RGB_R1	RGB_D1_LTDC_R3(PB12)3V3	PB12/ A7	O, 3.3V CMOS	Red data bit 1
Y6	RGB_R2	RGB_D2_LTDC_R4(PD4)3V3	PD4/ A2	O, 3.3V CMOS	Red data bit 2
AA5	RGB_R3	RGB_D3_LTDC_R5(PF5)3V3	PF5/ D1	O, 3.3V CMOS	Red data bit 3
Y5	RGB_R4	RGB_D4_LTDC_R6(PH8)3V3	PH8/ F1	O, 3.3V CMOS	Red data bit 4
Y4	RGB_R5	RGB_D5_LTDC_R7(PE9)3V3	PE9/ A3	O, 3.3V CMOS	Red data bit 5
J3	RGB_RESET#	RGB_RESET(PG8)3V3	PG8/ J3	O, 3.3V CMOS	Global Reset
L3	RGB_VSYNC	RGB_LTDC_VSYNC(PG4)3V3	PG4/ C9	O, 3.3V CMOS	Vertical sync
F3	GPIO_C_4 / DISP_VDD_EN	RGB_DISP_EN(PI2)	PI2/J4	O, 1.8V	Display power enable, active high
F4	GPIO_C_5 / DISP_BL_EN	RGB_BL_EN(PI0)	PI0/N3	O, 1.8V	Display backlight enable, active high

2.6.5 SPI Interface

The STM32MP135 Size-S OSM supports two Serial Peripheral Interface (SPI) module that allow communication at up to 50 Mbit/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The STM32MP135 OSM supports SPI_A using the SPI1 controller and SPI_B using the SPI4 controller of the MPU.

For more details on SPI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U15	SPI_A_SDI_(IO0)	SPI1_MISO(PA6)	PA6 / R8	I/O, 1.8V CMOS	SPI1 Master IN and Slave OUT.
V15	SPI_A_SDO_(IO1)	SPI1_MOSI(PC0)	PC0 / T4	I/O, 1.8V CMOS	SPI1 Master OUT and Slave IN.
Y15	SPI_A_CS0#	SPI1_NSS(PF12)	PF12/ J9	O, 1.8V CMOS	SPI1 Master Chip Select 0.
U16	SPI_A_SCK	SPI1_SCK(PC3)	PC3/P7	O, 1.8V CMOS	SPI1 Serial Data Clock.
Y22	SPI_B_SDI	SPI4_MISO(PE13)	PE13 /C1	I, 1.8V CMOS	SPI4 Master IN and Slave OUT.
Y23	SPI_B_SDO	SPI4_MOSI(PD1)	PD1 / C2	O, 1.8V CMOS	SPI4 Master IN and Slave OUT.
AA23	SPI_B_CS0#	SPI4_NSS(PD10)	PD10 / D3	O, 1.8V CMOS	SPI 4 Master Chip Select 0.
Y21	SPI_B_SCK	SPI4_SCK(PE12)	PE12/B1	O, 1.8V CMOS	SPI 4 Serial Data Clock.

2.6.6 Data UART

The STM32MP135 Size-S OSM supports four UART channels excluding the console UART. The UART_A and UART_B are connected to the UART7 and UART8 controllers of the MPU and supports flow control. Similarly, the UART_C and UART_D are connected to the UART5 and USART1 controllers of the MPU and does not have flow control. They are able to communicate at speeds of up to 10 Mbit/s.

For more details on UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A14	UART_A_RX	UART7_RX(PD11)	PD11 / G1	I, 1.8V CMOS	UART7 Receiver.
B13	UART_A_TX	UART7_TX(PE8)	PE8 / F8	O, 1.8V CMOS	UART7 Transmitter.
C13	UART_A_RTS	UART7_RTS(PF10)	PF10/K2	O, 1.8V CMOS	"Request to Send" handshake line for UART7.
C14	UART_A_CTS	UART7_CTS(PG15)	PG15 / G8	I, 1.8V CMOS	"Clear to Send" handshake line for UART7.
D14	UART_B_RX	UART8_RX(PE0)	PE0/ B3	I, 1.8V CMOS	UART8 Receiver.
D13	UART_B_TX	UART8_TX(PE1)	PE1/ C3	O, 1.8V CMOS	UART8 Transmitter.
D16	UART_B_CTS	UART8_CTS(PD14)	PD14/ F7	O, 1.8V CMOS	USART8 Clear to Send.
D15	UART_B_RTS	UART8_RTS(PE14)	PE14/ E2	I, 1.8V CMOS	USART8 Request to Send.
A22	UART_C_RX	UART5_RX(PF13)	PF13/ T3	I, 1.8V CMOS	UART5 Receiver.
B23	UART_C_TX	UART5_TX(PE7)	PE7/ C4	O, 1.8V CMOS	UART5 Transmitter.
C22	UART_D_RX	USART1_RX(PD13)	PD13/ N1	I, 1.8V CMOS	USART1 Receiver.
C23	UART_D_TX	USART1_TX(PA9)	PA9/ D2	O, 1.8V CMOS	USART1 Transmitter.

2.6.7 Console UART

In STM32MP135 Size-S OSM Module, UART4 is connected to the Console UART port of OSM and is used for getting the console prints.

For more details on UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D22	UART_CON_RX	UART4_RX(PD8)	PD8/B2	I, 1.8V CMOS	UART4 Receiver.
D23	UART_CON_TX	UART4_TX(PD6)	PD6/G9	O, 1.8V CMOS	UART4 Transmitter.

2.6.8 CAN Interface

The STM32MP135 OSM supports two FDCAN through FDCAN1 and FDCAN2 Controllers of the MPU.Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported by the FlexCAN module.

The STM32MP135 MPU Supports two CAN interface and are connected to OSM LGA. The feature is not available when using STM32MP131 MPU.

For more details of CAN pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC17	CAN_A_TX	FDCAN1_TX(PE10)	PE10/C7	O, 1.8V CMOS	CAN 1 Transmitter.
AB17	CAN_A_RX	FDCAN1_RX(PG9)	PG9/G5	I, 1.8V CMOS	CAN 1 Receiver.
AC19	CAN_B_TX	FDCAN2_TX(PB13)	PB13/ B10	O, 1.8V CMOS	CAN 2 Transmitter.
AB19	CAN_B_RX	FDCAN2_RX(PB5)	PB5/F9	I, 1.8V CMOS	CAN 2 Receiver.

2.6.9 SDIO Interface

STM32MP135 Size-S OSM Module supports one 4-bit SDMMC. SDMMC1 is connected to the 4-bit SDIO_A port of the OSM. They can be used for interfacing with ABH bus, SD Memory Cards and SDIO Cards and MMC devices. It is fully compliant with Multi-Media Card System Specification Version 4.51, SD memory card specifications version 4.1 & SDIO card specification version 4.0.

For more details of SDIO_A pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
F21	SDIO_A_CLK	SDMMC1_CK(PC12)	PC12/B13	O, 1.8V CMOS, 10K PD	SDMMC1 Clock.
E20	SDIO_A_CMD	SDMMC1_CMD(PD2)	PD2/G11	I/ O, 1.8V CMOS	SDMMC1 Command/Response.
G20	SDIO_A_D0	SDMMC1_D0(PC8)	PC8/C13	I/ O, 1.8V CMOS	SDMMC1 Data Lines.
G21	SDIO_A_D1	SDMMC1_D1(PC9)	PC9/G12	I/ O, 1.8V CMOS	SDMMC1 Data Lines.
H20	SDIO_A_D2	SDMMC1_D2(PC10)	PC10/F11	I/ O, 1.8V CMOS	SDMMC1 Data Lines.
H21	SDIO_A_D3	SDMMC1_D3(PC11)	PC11/C12	I/ O, 1.8V CMOS	SDMMC1 Data Lines.
J21	SDIO_A_CD#	SDMMC1_CD_B(PE2)	PE2/ T1	I OD, 1.8V CMOS, PU10K	SDMMC1 Card Detect
D21	SDIO_A_PWR_EN	SDIO_A_PWR_EN	NA	1.8V,10K PU	SDMMC1 Power Enable.
C20	SDIO_A_IOPWR	VDD_SD1	NA	P, 1.8V	SDMMC1 IO Voltage Output

2.6.10ADC Interface

STM32MP135 Size-S OSM Module supports two ADCs through the ADC2 controller of the MPU, whose resolution can be configured to 12, 10, 8 or 6-bit. Each ADC shares up to 18 external channels, performing conversions in the single-shot or scan mode. Each ADC can be served by a DMA controller, thus allowing the automatic transfer of ADC converted values to a destination location without any software action.

For more details on ADC pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M18	ADC_0	ADC2_INP3(PA0)	PA0/ L7	Analog, 0V-1V8	Analog Digital Converter 0.
N18	ADC_1	ADC2_INP8(PF11)	PF11/L8	Analog, 0V-1V8	Analog Digital Converter 1.

2.6.11 I2C Interface

The STM32MP135 OSM supports two I2C interfaces on OSM LGA. STM32MP135 MPU's I2C3 & I2C1 interfaces are connected to the I2C_A and I2C_B ports of the OSM LGA respectively. The I2C bus can be operated in Master and slave modes and is multi-Master capable. These I2Cs can operate in Standard, Fast and Fast Plus modes and can utilize 7-bit or 10-bit addressing.

For more details of I2C pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA15	I2C_A_SCL	I2C3_SCL(PB8)	PB8/ G4	I/O OD, 1.8V CMOS 1.5K PU	I2C3 Clock Signal.
AA16	I2C_A_SDA	I2C3_SDA(PH14)	PH14/B6	I/O OD, 1.8V CMOS 1.5K PU	I2C3 Data Signal.
AA20	I2C_B_SCL	I2C1_SCL(PD12)	PD12/ D7	I/O OD, 1.8V CMOS 1.5K PU	I2C4 Clock Signal.
AA21	I2C_B_SDA	I2C1_SDA(PD3)	PD3/ G6	I/O OD, 1.8V CMOS 1.5K PU	I2C4 Data Signal.

2.6.12 PWM Interface

The STM32MP135 Size-S OSM Module supports 1 PWM Timer over the PWM pins of the OSM. They can have max timer clock frequency of 209MHz.

For more details of PWM pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
E18	PWM_0	TIM1_CH1(PF9)	PF9/ H9	O, 1.8V CMOS	Pulse width modulation 0

2.6.13 JTAG

The STM32MP135 OSM supports JTAG interface for MPU debug purpose. It can be used for Arm® CoreSight™ trace and debug. The PU & PD required are provided in the MPU itself, eliminating the eternal Pull resisters and so can be easily connected to the JTAG debugger. The JTAG port contains an access detection mechanism which blocks unauthorized access via the debug port if configured as a tamper. The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG).

For more details on JTAG pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
N17	JTAG_TCK(SWCLK)	JTAG_TCK(PF14)	PF14/U4	I, 1.8V CMOS	JTAG Test Clock.
N19	JTAG_TMS(SWDIO)	JTAG_TMS(PF15)	PF15/L10	I, 1.8V CMOS	JTAG Test Mode Select.
P17	JTAG_TDI	JTAG_TDI(PH4)	PH4/T13	I, 1.8V CMOS	JTAG Test Data Input.
R17	JTAG_TDO	JTAG_TDO(PH5)	PH5/L12	O, 1.8V CMOS	JTAG Test Data Output.
R19	JTAG_NTRST	JTAG_NJTRST	NJTRST/R10	I, 1.8V CMOS	JTAG Test Reset, Active Low.

2.6.14 OSM GPIOs

The STM32MP135 OSM supports 7 dedicated GPIOs on OSM LGA through the GPIO_A [6:0] of OSM. Most of the STM32MP135 SoC Pins are made available on OSM LGA and can be configured as GPIO with interrupt capable (if not used as other interface). The STM32MP135 MPU's GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, some GPIO peripherals can produce CORE interrupts.

For more details on GPIO Interface pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D17	GPIO_A_0	OSM_GPIO_A_0(PB10)	PB10/G10	I/O, 1.8V CMOS	OSM General Purpose Input/output A0.
E17	GPIO_A_1	OSM_GPIO_A_1(PE11)	PE11/ E4	I/O, 1.8V CMOS	OSM General Purpose Input/output A1.
F17	GPIO_A_2	OSM_GPIO_A_2(PH2)	PH2/ G2	I/O, 1.8V CMOS	OSM General Purpose Input/output A2.
G17	GPIO_A_3	OSM_GPIO_A_3(PI3)	PI3/ H8	I/O, 1.8V CMOS	OSM General Purpose Input/output A3.
H17	GPIO_A_4	OSM_GPIO_A_4(PA14)	PA14/ R11	I/O, 1.8V CMOS	OSM General Purpose Input/output A4.
J17	GPIO_A_5	OSM_GPIO_A_5(PA13)	PA13/ K7	I/O, 1.8V CMOS	OSM General Purpose Input/output A5.
K17	GPIO_A_6/SPI_A_CS1#	OSM_GPIO_A_6(PI1)	PI1/ N4	I/O, 1.8V CMOS	OSM General Purpose Input/output A6.

2.6.15 Control Signals

The STM32MP135 Size-S OSM LGA module supports control signals for the module and Carrier Card control as per the OSM specifications.

For more details on OSM Control Signals pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U17	SYS_RST#	NRST	NA	I OD, 1.8V CMOS 10K PU	Hard RESET Input to Module.
V17	CARRIER_PWR_EN	CARRIER_PWR_EN	NA	O, 1.8V CMOS, 10K PU	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.
C18	TEST_GENERIC	BOOTFAIL_IN(PA13)	PA13/K7	O, 1.8V CMOS	This signal can be used for monitoring Boot failure. Can be used as GPIO.

2.6.16 Boot Selection

STM32MP135 OSM supports two boot selection modes. For more details on Boot Selection Signals pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U19	BOOT_SEL0#	BOOT_SEL0	PI5-BOOT1/N11	I OD, 1.8V CMOS, 1K PU	**BOOT_SEL[1:0]** **01 -** eMMC Boot **10 -** SD Boot (Here 1means the pin left floating)
R18	BOOT_SEL1#	BOOT_SEL1	PI6-BOOT2/M11	I OD, 1.8V CMOS, 1K PU	
T17	FORCE_RECOVERY#	FORCE_RECOV#	NA	I OD, 1.8V CMOS, 10K PU	Pulling this signal low switches the OSM to programming mode irrespective of the state of Boot Selection pins.

2.6.17Vendor defined

In STM32MP135 based Size-S OSM Module, some additionally functionality/GPIOs are supported through Vendor Defined Contacts.

For more details on Vendor defined Signals pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
B22	VENDOR DEFINED1	PWR_CPU_ON	PWR_CPU_ON/R4	I OD, 1.8V CMOS	PMIC User Power On Key
C16	VENDOR DEFINED	PWR_LP	PWR_LP/U14	I/O, 1.8V CMOS	Connected to PMIC control signal

2.6.18Power and GND

The STM32MP135 Size-S OSM LGA Module works with 5V power input (VCC) from OSM LGA and generates all other required powers internally On-Module itself. STM32MP135 OSM LGA Module also supports coin cell power input (VDD_RTC) from OSM LGA to On-Module RTC controller (MPU Internal) for real time clock.

For more details on Power & GND Signals pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y17, Y8, Y9, Y10, Y11	VCC_IN_5V	VCC_IN_5V	NA	I, 5V Power	Supply Voltage.
D18,E15,E21,F16,F20,J16,J20,L18,M16, M20,P18,R16,R20,V16,V20,Y18,AA14,AA17,AA19,AA22,AB15,AB21, A4,A7,A10,B2,B8,B9, C11,D1,D5,E2,H2,H4,L2,L4,P2,U2,U4,V1, W3,Y2,AA1,AA4,AA7,AA8,AA10, D8, P4,R1, AA11,AB3,AB6,AB9, AC4,AC7,AC10	GND	GND	NA	Power	Ground.
W17	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.7 STM32MP135 Pin Multiplexing on OSM BGA

The STM32MP135 MPU IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the STM32MP135 MPU's IO pins can be configured as GPIO if required. The below table provides the details of STM32MP135 MPU pin connections to the OSM LGA and with selected pin function highlighted and available alternate functions. This table has been prepared by referring STMicroelectronics's STM32MP135 MPU's Hardware User's Manual.

Important Note:

1. It is strongly recommended to use the pin function same as selected in the OSM BGA for iWave's BSP reusability and to have compatible OSM modules in future for upgradability.

2. Signals highlighted are the default function selected.

Table 4: STM32MP135 SoC IOMUX for OSM BGA interfaces

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
ETH1	T16	U3		MCO2		TIM8_BKIN							SAI2_MCLK_B	ETH1_MDC		DCMIPP_D1				ETH1_MDC
	T15	R5		TIM2_CH3	TIM5_CH3	LPTIM4_OUT	TIM15_CH1			USART2_TX				ETH1_MDIO					ADC1_INP1, ADC2_INP1	ETH1_MDIO
	R15	R3	RCC_MCO_1			USART2_CK	I2C2_SCL	I2C3_SDA				SPDIFRX_IN0	ETH1_REF_CLK/ETH1_RX_CLK	QUADSPI_BK1_IO2	FMC_NE1					ETH1_RX_CLK
	M15	R6		TIM1_CH1N	TIM3_CH2	TIM8_CH1N	SAI2_D1	I2S1_CK/SPI1_SCK		USART1_CTS/USART1_NSS		TIM14_CH1		ETH1_CRS_DV/ETH1_RX_CTL/ETH1_RX_DV	SAI2_SD_A				ADC1_INP16	ETH1_RX_CTL
	K15	K9			TIM3_ETR	DFSDM1_CKIN2	SAI1_D3	I2S1_MCK			UART5_DE/UART5_RTS	SPDIFRX_IN2		ETH1_RXD0	SAI2_D3				ADC1_INP4, ADC2_INP4	ETH1_RXD0
	L15	P8				DFSDM1_DATIN2	SAI2_D4	I2S_CKIN	SAI1_D4	USART2_CTS/USART2_NSS		SPDIFRX_IN3		ETH1_RXD1					ADC1_INP10, ADC2_INP10	ETH1_RXD1
	N15	M8	DEBUG_DBTRGI	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	USART1_RX	I2S1_MCK	SAI2_FS_A	USART1_CK	UART4_CTS		SAI2_D2	ETH1_RXD2					ADC1_INP9, ADC1_INN5, ADC2_INP9, ADC2_INN5	ETH1_RXD2
	P15	N8		TIM1_CH3N	TIM3_CH4	TIM8_CH3N		I2S1_CK/SPI1_SCK	DFSDM1_DATIN1	UART4_RX				ETH1_RXD3					ADC1_INP5, ADC2_INP5	ETH1_RXD3

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
	J15	R7				DFSDM1_DATIN0			SAI1_D3				ETH1_CRS_DV/ETH1_RX_DV	ETH1_GTX_CLK					ADC2_INP2	ETH1_GTX_CLK
	K16	M6		TIM2_CH4		LPTIM1_OUT	I2C5_SMBA			USART3_RX				ETH1_TX_CTL/ETH1_TX_EN						ETH1_TX_CTL
	H15	R9		LPTIM1_OUT						USART6_CTS/USART6_NSS				ETH1_TXD0					ADC2_INP6, ADC2_INN2	ETH1_TXD0
	G15	T8		LPTIM1_ETR					SAI2_D1	USART6_TX			SAI2_SD_A	ETH1_TXD1						ETH1_TXD1
	H16	U8		SPI5_NSS				I2S1_WS/SPI1_NSS	SAI2_MCLK_A	USART1_DE/USART1_RTS			SAI2_CK1	ETH1_TXD2					ADC1_INP15	ETH1_TXD2
	G16	L9			SAI2_SCK_B	TIM8_CH3	TIM15_CH1				UART4_RX		ETH1_TXD3		FMC_NE1					ETH1_TXD3
ETH2	C6	H1		TIM17_CH1									ETH2_MDC	LTDC_G4	FMC_A15	DCMIPP_VSYNC	DCMIPP_D3			ETH2_MDC
	C7	K3		RTC_OUT2	SAI1_D1			I2S_CKIN	SAI1_SD_A		UART4_RX	QUADSPI_BK1_NCS		ETH2_MDIO	FMC_A6		LTDC_B4		TAMP_IN7	ETH2_MDIO
	P1	H7		SPI5_NSS	TIM5_CH2	SAI2_SD_A		I2S2_WS/SPI2_NSS	I2C4_SCL	USART6_RX		QUADSPI_BK2_IO0		ETH2_REF_CLK/ETH2_RX_CLK	FMC_A12		LTDC_G6			ETH2_RX_CLK
	L1	L6		LPTIM1_IN1			SAI2_SCK_A		SAI2_CK2	USART6_DE/USART6_RTS	USART3_CTS		ETH2_PHY_INTN	ETH1_PHY_INTN	ETH2_CRS_DV/ETH2_RX_CTL/ETH2_RX_DV					ETH2_RX_CTL
	J1	P3				USART2_RX								ETH2_RXD0	FMC_A4	DCMIPP_D4	LTDC_B6			ETH2_RXD0
	K1	N5		TIM1_CH4			I2C5_SCL	I2S2_WS/SPI2_NSS		USART1_CTS/USART1_NSS			ETH2_RXD1	ETH1_CLK		ETH2_CLK				ETH2_RXD1
	M1	J6			TIM12_CH1	USART2_CK	I2C5_SDA	I2S2_CK/SPI2_SCK				QUADSPI_BK1_IO2	ETH1_PHY_INTN	ETH1_RX_ER	ETH2_RXD2	QUADSPI_BK1_NCS				ETH2_RXD2
	N1	J8	RCC_MCO_1		SAI2_MCLK_A	TIM8_BKIN2	I2C4_SDA	SPI5_MISO	SAI2_CK1	USART1_CK	I2S2_SDO/SPI2_MOSI		USB_OTG_HS_SOF	ETH2_RXD3	FMC_A21		LTDC_B7			ETH2_RXD3

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
	H1	U2				TIM8_BKIN2	I2C2_SDA		SAI2_SD_B			FDCAN2_RX	ETH2_GTX_CLK	ETH1_MDIO	FMC_A13	DCMIPP_D15	DCMIPP_D12			ETH2_GTX_CLK
	J2	L1		TIM16_CH1				SPI5_NSS		UART7_RX		QUADSPI_BK1_IO2		ETH2_TX_CTL/ETH2_TX_EN		LTDC_R7	LTDC_G4			ETH2_TX_CTL
	G1	J7		TIM17_CH1						UART7_TX	UART4_CTS		ETH1_CLK125	ETH2_TXD0	FMC_A18		LTDC_G2			ETH2_TXD0
	F1	R1					SAI2_D3	I2S2_MCK		USART3_TX	UART4_TX		ETH2_TXD1		FMC_A24	DCMIPP_D14	LTDC_B2			ETH2_TXD1
	G2	P4		LPTIM1_ETR	TIM4_ETR	SAI2_FS_A	I2C2_SMBA	I2S2_SDI/SPI2_MISO	SAI2_D2			FDCAN2_TX	ETH2_TXD2		FMC_NBL0		LTDC_G7			ETH2_TXD2
	F2	R2	RCC_MCO_2	TIM1_BKIN2	SAI2_SCK_B		TIM15_CH2	I2C3_SMBA	SAI1_SCK_B		UART4_DE/UART4_RTS			ETH2_TXD3	FMC_A22	DCMIPP_D7	LTDC_G3			ETH2_TXD3
USB_A	AB13	U9																	USBH_HS_DM2 (boot), OTG_HS_DM	USB_DM2
	AC14	T9																	USBH_HS_DP2 (boot), OTG_HS_DP	USB_DP2
	AB14	J12		TIM1_CH3															OTG_HS_ID	USB_OTG_HS_ID
	AB16	U13																	OTG_HS_VBUS	USB_OTG_HS_VBUS
USB_B	AB23	U12																	USBH_HS_DM1	USB_DM1
	AC22	T12																	USBH_HS_DP1	USB_DP1
SAI	W18	K1		SPI5_MISO	SAI1_D2	DFSDM1_DATIN3	TIM15_CH1N	I2S_CKIN	SAI1_FS_A	UART7_DE/UART7_RTS	UART8_TX	QUADSPI_BK2_NCS	FMC_NCE2		FMC_A25	DCMIPP_D3	LTDC_G7			SAI1_FS_A
	V18	E1			SAI1_MCLK_A				SAI1_CK1			FDCAN1_RX			FMC_D2/FMC_DA2	DCMIPP_D1				SAI1_MCLK_A
	W20	G7		USART2_TX	TIM5_CH3	DFSDM1_CKIN1	I2C3_SCL	SPI5_MOSI	SAI1_SCK_A			QUADSPI_BK2_IO2	SAI1_CK2	ETH1_CRS	FMC_A6	DCMIPP_D3				SAI1_SCK_A
	W21	M7		TIM2_CH1/TIM2_ETR	USART2_CK	TIM8_CH1N	SAI1_D1	I2S1_WS/SPI1_NSS	SAI1_SD_A				ETH1_PPS_OUT	ETH2_PPS_OUT					ADC1_INP2	SAI1_SD_A
	V21	H2						SPI5_SCK	SAI1_SD_B		UART8_CTS	FDCAN1_TX	QUADSPI_BK2_IO1		FMC_NE3	DCMIPP_D2				SAI1_SD_B

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
SPI	U16	P7			SAI1_CK1	DFSDM1_CKOUT		I2S1_SDI/SPI1_MISO	I2S1_CK/SPI1_SCK		UART5_CTS		SAI1_MCLK_A	ETH1_TX_CLK	ETH2_TX_CLK				ADC1_INP13, ADC1_INN12, TAMP_IN5	SPI1_SCK
	U15	R8		TIM1_BKIN	TIM3_CH1	TIM8_BKIN	SAI2_CK2	I2S1_SDI/SPI1_MISO		USART1_CK	UART4_DE/UART4_RTS	TIM13_CH1			SAI2_SCK_A				ADC1_INP17, ADC1_INN16, TAMP_IN2	SPI1_MISO
	V15	T4			SAI1_SCK_A		SAI1_CK2	I2S1_MCK	I2S1_SDO/SPI1_MOSI	USART1_TX									ADC1_INP0, ADC1_INN1, ADC2_INP0, ADC2_INN1, TAMP_IN3	SPI1_MOSI
	Y15	J9						I2S1_WS/SPI1_NSS	SAI1_SD_A		UART4_TX		ETH1_TX_ER	ETH1_CLK125					ADC1_INP6, ADC1_INN2	SPI1_NSS
	Y21	B1		TIM1_CH3N				I2S4_CK/SPI4_SCK			UART8_DE/UART8_RTS	LTDC_VSYNC		LTDC_G4	FMC_D9/FMC_DA9	DCMIPP_D11	LTDC_G6	HDP_HDP4		SPI4_SCK
	Y22	C1		TIM1_CH3			I2C5_SDA	I2S4_SDI/SPI4_MISO						LTDC_B1	FMC_D10/FMC_DA10	DCMIPP_D4	LTDC_R6			SPI4_MISO
	Y23	C2					I2C5_SCL	I2S4_SDO/SPI4_MOSI			UART4_TX	QUADSPI_BK1_NCS		LTDC_B6	FMC_D3/FMC_DA3	DCMIPP_D13	LTDC_G2			SPI4_MOSI
	AA23	D3	RTC_REFIN				I2C5_SMBA	I2S4_WS/SPI4_NSS		USART3_CK		LTDC_G5		LTDC_B7	FMC_D15/FMC_DA15	DCMIPP_VSYNC	LTDC_B2		RTC_REFIN	SPI4_NSS
DATA UART	A14	G1				LPTIM2_IN2	I2C4_SMBA			USART3_CTS/USART3_NSS	SPDIFRX_IN0	QUADSPI_BK1_IO2	ETH2_CLK125	LTDC_R7	FMC_A16/FMC_CLE	UART7_RX	DCMIPP_D4			UART7_RX
	B13	F8		TIM1_CH1N		DFSDM1_CKIN2		I2C1_SDA		UART7_TX					FMC_D5/FMC_DA5					UART7_TX
	C14	G8								USART6_CTS/USART6_NSS	UART7_CTS	QUADSPI_BK1_IO1	ETH2_PHY_INTN	LTDC_B4		DCMIPP_D10	LTDC_B3			UART7_CTS
	C13	K2		TIM16_BKIN	SAI1_D3	TIM8_BKIN		SPI5_NSS		USART6_DE/USART6_RTS	UART7_DE/UART7_RTS	QUADSPI_CLK				DCMIPP_HSYNC	LTDC_B5		TAMP_IN1	UART7_RTS
	D14	B3							DCMIPP_D12		UART8_RX	FDCAN2_RX		LTDC_B1	FMC_A11	DCMIPP_D1	LTDC_B5			UART8_RX

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
	D13	C3		LPTIM1_IN2							UART8_TX	LTDC_HSYNC		LTDC_R4	FMC_NBL1	DCMIPP_D3	DCMIPP_D12			UART8_TX
	D16	F7			TIM4_CH3		I2C3_SDA			USART1_RX	UART8_CTS				FMC_D0/FMC_DA0	DCMIPP_D8	LTDC_R4			UART8_CTS
	D15	E2		TIM1_BKIN			SAI1_D4				UART8_DE/UART8_RTS	QUADSPI_BK1_NCS	QUADSPI_BK2_IO2		FMC_D11/FMC_DA11	DCMIPP_D7	LTDC_G0		TAMP_IN6	UART8_RTS
	A22	T3		TIM2_CH1/TIM2_ETR	SAI1_MCLK_B				DFSDM1_DATIN3	USART2_TX	UART5_RX								ADC1_INP11, ADC1_INN10, ADC2_INP11, ADC2_INN10	UART5_RX
	B23	C4		TIM1_ETR			LPTIM2_IN1				UART5_TX				FMC_D4/FMC_DA4	LTDC_B3	LTDC_R5			UART5_TX
	C22	N1		LPTIM2_ETR	TIM4_CH2	TIM8_CH2	SAI1_CK1		SAI1_MCLK_A	USART1_RX		QUADSPI_BK1_IO3		QUADSPI_BK2_IO2(131 &135)	FMC_A18		LTDC_G4			USART1_RX
	C23	D2		TIM1_CH2			I2C3_SMBA		DFSDM1_DATIN0	USART1_TX	UART4_TX		FMC_NWAIT			DCMIPP_D0	LTDC_R6			USART1_TX
UART CONSOLE	D22	B2				USART2_TX		I2S4_WS		USART3_TX	UART4_RX					DCMIPP_D9	DCMIPP_D3			UART4_RX
	D23	G9		TIM16_CH1N	SAI1_D1				SAI1_SD_A		UART4_TX					DCMIPP_D4	DCMIPP_D0			UART4_TX
CAN INTERFACE	AC17	G5	DEBUG_DBTRGO				I2C2_SDA			USART6_RX	SPDIFRX_IN3	FDCAN1_RX	FMC_NE2		FMC_NCE	DCMIPP_VSYNC				FDCAN1_RX
	AB17	C7		TIM1_CH2N						UART7_RX		FDCAN1_TX			FMC_D7/FMC_DA7					FDCAN1_TX
	AB19	F9	DEBUG_TRACED4	TIM17_BKIN	TIM3_CH2			I2S2_SDI/ SPI2_MISO	I2C4_SMBA		SDMMC1_CKIN	FDCAN2_RX		UART5_RX		LTDC_B6	LTDC_DE			FDCAN2_TX
	AC19	B10	DEBUG_TRACECLK	TIM1_CH1N			LPTIM2_OUT	I2S2_WS/ SPI2_NSS	I2C4_SCL		SDMMC1_D123DIR	FDCAN2_TX		UART5_TX		LTDC_CLK				FDCAN2_RX
SDIO	F21	B13	DEBUG_TRACECLK								UART7_TX		SAI2_SD_B		SDMMC1_CK		LTDC_DE			SDMMC1_CK
	E20	G11	DEBUG_TRACED4		TIM3_ETR		I2C1_SMBA	I2S3_WS/ SPI3_NSS	SAI2_D1	USART3_RX					SDMMC1_CMD					SDMMC1_CMD
	G20	C13	DEBUG_TRACED0		TIM3_CH3	TIM8_CH3		I2S3_SDI/ SPI3_MISO		USART6_CK	USART3_CTS		SAI2_FS_B	UART5_DE/ UART5_RTS	SDMMC1_D0		LTDC_G7			SDMMC1_D0

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
	G21	G12	DEBUG_TRACED1		TIM3_CH4	TIM8_CH4				USART3_RTS	UART5_CTS	FDCAN1_TX			SDMMC1_D1		LTDC_B4			SDMMC1_D1
	H20	F11	DEBUG_TRACED2					I2C1_SCL	I2S3_CK/SPI3_SCK	USART3_TX			SAI2_MCLK_B		SDMMC1_D2					SDMMC1_D2
	H21	C12	DEBUG_TRACED3				I2C1_SDA		I2S3_SDO/SPI3_MOSI	USART3_CK	UART5_RX		SAI2_SCK_B		SDMMC1_D3					SDMMC1_D3
ADC	M18	L7		TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN		SAI1_SD_B		UART5_TX			ETH1_CRS	ETH2_CRS				ADC1_INP7,ADC1_INN3,ADC2_INP7,ADC2_INN3	ADC2_INP7
	N18	L8		USART2_TX	SAI1_D2	DFSDM1_CKIN3			SAI1_FS_A						ETH2_RX_ER				ADC1_INP8,ADC1_INN4,ADC2_INP8,ADC2_INN4	ADC2_INP8
I2C	AA15	G4	TIM16_CH1	TIM4_CH3		I2C1_SCL	I2C3_SCL	DFSDM1_DATIN1		UART4_RX		SAI1_D1		FMC_D13/FMC_DA13	DCMIPP_D6					I2C3_SCL
	AA16	B6			DFSDM1_DATIN2	I2C3_SDA		DCMIPP_D8		UART4_RX			LTDC_B4		DCMIPP_D2	DCMIPP_PIXCLK				I2C3_SDA
	AA20	D7		LPTIM1_IN1	TIM4_CH1			I2C1_SCL		USART3_DE/USART3_RTS					FMC_A17/FMC_ALE	DCMIPP_D6				I2C1_SCL
	AA21	G6			TIM2_CH1/TIM2_ETR	USART2_CTS/USART2_NSS	DFSDM1_CKOUT	I2C1_SDA	SAI1_D3						FMC_CLK	DCMIPP_D5				I2C1_SDA
PWM	E18	H9		TIM17_CH1N	TIM1_CH1	DFSDM1_CKIN3			SAI1_D4	UART7_CTS	UART8_RX	TIM14_CH1	QUADSPI_BK1_IO1	QUADSPI_BK2_IO3	FMC_A9		LTDC_B6			TIM1_CH1
JTAG	N17	U4																	DEBUG_JTCK-SWCLK	DEBUG_JTCK-SWCLK
	N19	L10																	DEBUG_JTMS-SWDIO	DEBUG_JTMS-SWDIO
	P17	T13																	DEBUG_JTDI	DEBUG_JTDI
	R17	L12																	DEBUG_JTDO-SWO	DEBUG_JTDO-SWO
	R19	R10																	DEBUG_JTRST	DEBUG_JTRST
RGB	Y7	C8	DEBUG_TRACED8	TIM1_ETR				I2S3_SDI/SPI3_MISO			UART7_CTS		SDMMC2_CKIN	LTDC_R1		LTDC_R5	LTDC_R2			LTDC_R2
	AA6	A7	DEBUG_TRACED10				I2C2_SMBA		DFSDM1_DATIN1	UART7_DE/UART7_RTS				UART5_RX	SDMMC1_D5	LTDC_R3	LTDC_VSYNC			LTDC_R3

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
	Y6	A2				USART2_DE/USART2_RTS		I2S3_SDI/SPI3_MISO	DFSDM1_CKIN0			QUADSPI_CLK		LTDC_R1	FMC_NOE	LTDC_R4	LTDC_R6			LTDC_R4
	AA5	D1	DEBUG_TRACED12				DFSDM1_CKIN0	I2C1_SMBA				LTDC_G0			FMC_A5	DCMIPP_D11	LTDC_R5			LTDC_R5
	Y5	F1	DEBUG_TRACED9		TIM5_ETR	USART2_RX	I2C3_SDA							LTDC_R6	FMC_A8	DCMIPP_HSYNC	LTDC_R2	HDP_HDP2		LTDC_R6
	Y4	A3		TIM1_CH1								QUADSPI_BK1_IO1		LTDC_HSYNC	FMC_D6/FMC_DA6	DCMIPP_D7	LTDC_R7	HDP_HDP3		LTDC_R7
	W4	E9	DEBUG_TRACED15		USART2_CK	TIM8_CH1N	I2C5_SCL		I2S3_CK/SPI3_SCK		UART4_TX					LTDC_G3	LTDC_G2			LTDC_G2
	V3	B9				LPTIM2_IN2	I2C5_SDA	I2S4_SDI/SPI4_MISO	I2S3_WS/SPI3_NSS						FMC_A3		LTDC_G3			LTDC_G3
	V4	B4										QUADSPI_BK1_IO0			FMC_NWE	LTDC_B0	LTDC_G4			LTDC_G4
	U3	A4										FDCAN2_TX			FMC_A10	DCMIPP_PIXCLK	LTDC_G5			LTDC_G5
	T3	F2		TIM1_ETR	SAI2_MCLK_A					USART1_DE/USART1_RTS				ETH2_CRS_DV/ETH2_RX_CTL/ETH2_RX_DV	FMC_A7	DCMIPP_D1	LTDC_G6			LTDC_G6
	T4	E7	DEBUG_TRACED5	TIM2_CH1/TIM2_ETR				I2S4_MCK		UART4_DE/UART4_RTS	UART4_RX	LTDC_R0		LTDC_G7	FMC_A9	DCMIPP_D14	DCMIPP_D5	HDP_HDP5		LTDC_G7
	R4	L3			SAI2_FS_B			I2C3_SDA	SPI5_SCK			QUADSPI_BK2_IO3	ETH2_TX_CLK	ETH1_TX_CLK		QUADSPI_BK1_IO3	LTDC_B2			LTDC_B2
	R3	B7	DEBUG_TRACED1				I2C2_SCL		DFSDM1_CKIN1	USART6_CK		SDMMC2_D0DIR		SDMMC1_D0DIR	FMC_A2	LTDC_G4	LTDC_B3			LTDC_B3
	P3	T2					I2C3_SCL	SPI5_MOSI				QUADSPI_BK2_IO1	ETH1_COL	LTDC_R5	ETH2_COL	QUADSPI_BK1_IO0	LTDC_B4			LTDC_B4
	N3	A5		USART2_RX	TIM4_CH4	DFSDM1_DATIN2						QUADSPI_BK1_IO3			FMC_D1/FMC_DA1		LTDC_B5			LTDC_B5
	N4	G3	DEBUG_TRACED6	TIM16_CH1N	TIM4_CH1	TIM8_CH1	USART1_TX		SAI1_CK2	LTDC_B6		QUADSPI_BK1_NCS		ETH2_MDIO	FMC_NE3	DCMIPP_D5	LTDC_B7	HDP_HDP6		LTDC_B6

Interface	OSM Pin Number	STM32MP135 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Alternate Function	Default
	M3	A8	DEBUG_TRACED7				I2C2_SDA	I2S3_SDO/SPI3_MOSI							FMC_A1	LTDC_B7	LTDC_G1	HDP_HDP7		LTDC_B7
	J4	D9		TIM1_CH4	TIM12_CH2			I2S4_CK/SPI4_SCK	DCMIPP_D13			LTDC_B5		LTDC_DE	FMC_A20	DCMIPP_D9	DCMIPP_D8			LTDC_DE
	M4	B5	DEBUG_TRACECLK			DFSDM1_DATIN3							SDMMC2_CDIR	LTDC_B5	FMC_D14/FMC_DA14	LTDC_CLK	LTDC_B0			LTDC_CLK
	K3	C11	DEBUG_TRACED0		TIM5_CH1	SAI2_D3	DFSDM1_DATIN2	I2S3_MCK	I2S2_SDO/SPI2_MOSI	USART3_CTS/USART3_NSS	SDMMC1_D4					LTDC_HSYNC	LTDC_R2	HDP_HDP0		LTDC_HSYNC
	L3	C9	DEBUG_TRACED1	TIM1_BKIN2			DFSDM1_CKIN3				USART3_RX		SDMMC2_D123DIR	LTDC_VSYNC	FMC_A14	DCMIPP_D8	DCMIPP_D13	HDP_HDP1		LTDC_VSYNC
GPIOs	G17	H8										SPDIFRX_IN3			ETH1_RX_ER					GPIO
	D17	G10			TIM2_CH3		LPTIM2_IN1	I2C5_SMBA	I2S4_WS/SPI4_NSS	I2S2_CK/SPI2_SCK								LTDC_R3		GPIO
	F17	G2			LPTIM1_IN2					DCMIPP_D9	LTDC_G1	UART7_TX	QUADSPI_BK2_IO0	ETH2_CRS	ETH1_CRS	FMC_NE4	ETH2_CLK125	LTDC_B0		GPIO
	J17	K7		DEBUG_DBTRGO	DEBUG_DBTRGI	RCC_MCO_1						UART4_TX								GPIO
	H17	R11		DEBUG_DBTRGO	DEBUG_DBTRGI	RCC_MCO_2								USB_OTG_HS_SOF						GPIO
	K17	N4										SPDIFRX_IN1								GPIO
	E17	E4	TIM1_CH2		TIM1_CH2	USART2_CTS/USART2_NSS		SAI1_D2	I2S4_SDO/SPI4_MOSI	SAI1_FS_A	USART6_CK		LTDC_R0	ETH2_TX_ER	ETH1_TX_ER	FMC_D8/FMC_DA8	DCMIPP_D10	LTDC_R5		GPIO
BOOT & CONTROL	U19	N11																		PI5-BOOT1
	R18	M11																		PI6-BOOT2
	U17	K10																		NRST

3. TECHNICAL SPECIFICATION

This section provides detailed information about the STM32MP135 OSM LGA Module technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the single VCC_IN_5V in Size-S Module and returned through the numerous GND pins on the LGA/BGA.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of STM32MP135 OSM LGA Module.

Table 5: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_IN_5V [1]	4.75	5V	5.25	-
2	VDD_RTC [2]	-	3V	-	-

[1] STM32MP135 OSM LGA Module is designed to work with VCC_IN_5V input power rail from OSM Base Board.

[2]STM32MP135 OSM LGA Module use this voltage as backup power source for storing RTC contents when VCC_IN_5V is OFF.

3.1.2 Power Consumption

TBD

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of STM32MP135 OSM LGA Module.

Table 6: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS Compliance

iWave's STM32MP135 OSM LGA Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's STM32MP135 OSM LGA Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the Module except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 STM32MP135 OSM LGA Module Mechanical Dimensions

STM32MP135 OSM LGA Module PCB size is 30 mm x 30 mm. Module mechanical dimensions are shown below. (All dimensions are shown in mm).

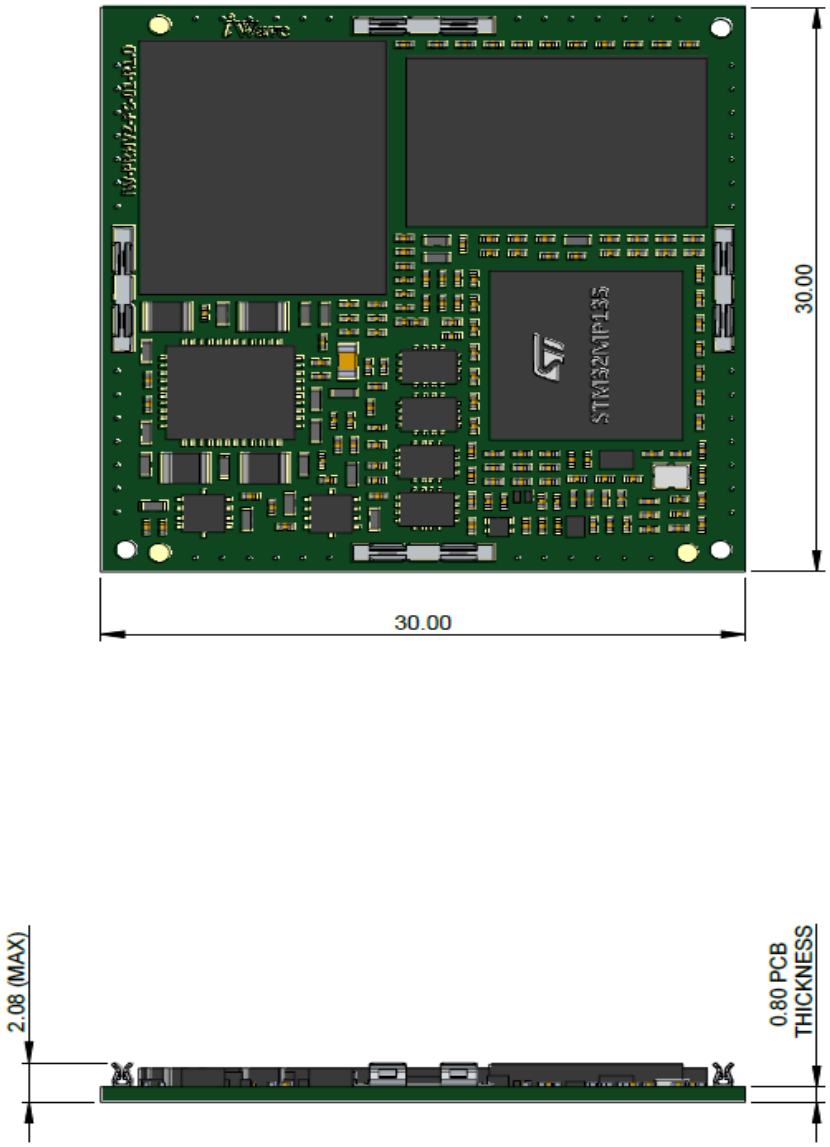

Figure 4: Mechanical dimension of STM32MP135 OSM LGA Module – Top & Side1

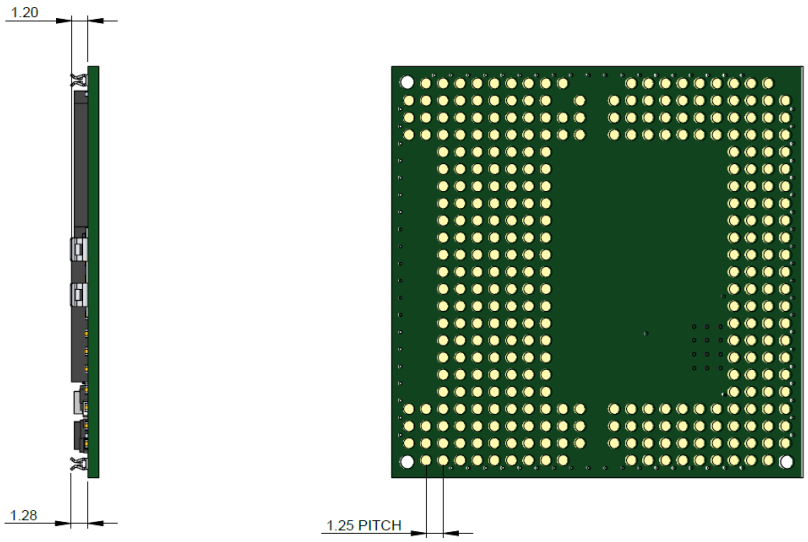

Figure 5: Mechanical dimension of STM32MP135 OSM LGA Module – Side2 & Bottom

The STM32MP135 OSM LGA Module PCB thickness is 0.9mm±0.1mm, top side maximum height component is 1.28mm (RFI Shield Clip). In bottom side, there are no components available.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different STM32MP135 OSM LGA Module variants. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size Module configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 7: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G54M – STM32MP135 OSM		
iW-G54M-OS35-3D512M-E004G-BIA-PP	STM32MP135 Security CPU, 512MB DDR3L, 4GB eMMC, based OSM	-40°C to 85°C

Note:

** Some Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.*

** For Module identification purpose, Product Part Number and Module Unique Serial Number are pasted as Label with QR Code on Module.*

** Please contact iWave for other RAM and eMMC Configurations.*

5. APPENDIX

5.1 STM32MP135 based Single Board Computer

iWave Systems supports iW-RainboW-G54S-STM32MP135 Single Board Computer which is targeted for quick validation of STM32MP135 MPU based OSM and its features. Being a SBC of compact form factor of 85mm x 56mm size, the SBC is highly useful for testing all the necessary interfaces & also has on-board connectors to validate complete OSM supported features.