iW-RainboW-G35V
Zynq Ultrascale+ MPSoC (ZU19/17/11EG)
3U-VPX Plug-in Module
Datasheet

iWave
Embedding Intelligence

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Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the Hardware Datasheet for the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module and provides detailed information on the overall design & usage from a Hardware Systems perspective. This 3U-VPX Plug-in Module consist of iWave's ZU19/17/11EG MPSoC based System On Module (SOM) and 3U-VPX carrier board.

The details about the Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM hardware is explained in another document "iW-RainboW-G35M-Zynq-Ultrascale+MPSoC (ZU11/17/19EG)-SOM-HardwareUserGuide".

1.2 Overview

iWave's Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module is fully compliant with OpenVPX System Standard ANSI/VITA 65.0-2019. Also, its optical interconnect is fully compliant with ANSI/VITA 66.4 Half Width MT Variant (within the VITA 66 family of blind mate Fiber Optic interconnects).

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
B2B	Board to Board
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor
CPutp	Control Plane Ultra-Thin Pipe
DP	Display Port
DPutp	Data Plane Ultra-Thin Pipe
FPGA	Field Programmable Gate Array
GA	Geographical Address
GAP	Geographical Address Parity
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
LED	Light-emitting Diode
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signal
Mbps	Megabits per sec

Acronyms	Abbreviations
MHz	Mega Hertz
NC	No Connect
NVMe	Non-volatile Memory Express
NVMRO	Non-Volatile Memory Read Only
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RX	Receiver
SOM	System On Module
SYS_CON	System Controller
SYSRESET	System Reset
TX	Transmitter
TXVR	Transceiver
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
VPX	Virtual Path Cross-Connect

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- ANSI/VITA 65.0 Specification
- ANSI/VITA 66.0 Specification
- ANSI/VITA 66.4 Specification
- Zynq Ultrascale+ MPSoC Datasheet & Reference Manual
- Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM Hardware User Guide

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module features with high level block diagram and detailed information about each block.

The 3U-VPX Plug-in module conforms to below mentioned Module Profile & Slot Profile defined in OpenVPX System Standard ANSI/VITA 65.0-2019.

- Module Profile : MOD3-SWH-4F1U7U1J-16.8.7-n
- Slot Profile : SLT3-SWH-4F1U7U1J-14.8.7-n
- Slot Pitch : 1 inch Conduction Cooled

Also this 3U-VPX Plug-in module is compatible with more Slot Profiles which are listed in the **APPENDIX** section of this document.

2.1 3U-VPX Plug-in Module Block Diagram

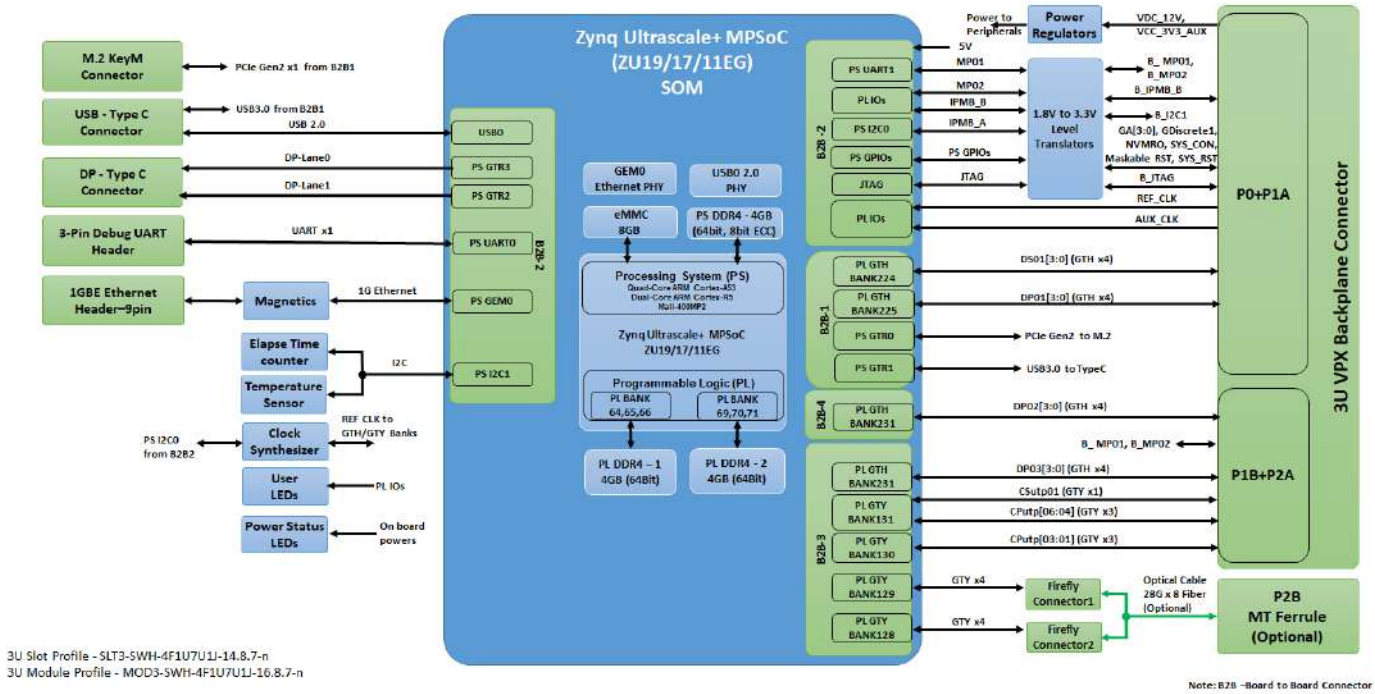

Figure 1: 3U-VPX Plug-in Module Block Diagram

2.2 3U-VPX Plug-in Module Features

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports the following features.

SoC

- Xilinx Zynq Ultrascale+ MPSoC (FFVC1760 Package) – ZU19EG, ZU17EG, ZU11EG
  - Programming Logic (PL) with up to 1.1M Logic cells
  - Processing System (PS) with integrated
    - Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.5GHz),
    - Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 600MHz) and
    - Mali™-400 MP2 Graphics Processor.

Memory

- 4GB DDR4 SDRAM (64bit) with ECC for PS (Expandable)
- 4GB DDR4 SDRAM1 (64bit) for PL (Expandable)
- 4GB DDR4 SDRAM2 (64bit) for PL (Expandable)
- 8GB eMMC Flash (Expandable)

3U VPX Backplane Features

- **3U VPX Connector - P0+P1A**
  - Data Plane Port
    - DP01[3:0] - 1G/2.5G/10G Ethernet or PCIe Gen3 (using PL GTH Transceivers @ Upto 16Gbps/lane)
  - Data Switch Port
    - DS01[3:0] - 1G/2.5G/10G Ethernet or PCIe Gen3 (using PL GTH Transceivers @ Upto 16Gbps/lane)
  - Utility Plane
    - System Control Signals (SYSRESET, NVMRO, SYS_CON, SM Bus, Geographic Address Field, JTAG)
    - System Reference Clocks (REF_CLK, AUX_CLK)
    - Bussed GPIO (GDiscrete1)
    - Power Input (12V VDC, 3.3V_AUX, VBAT)

- **3U VPX Connector - P1B+P2A**
  - Data Plane Port
    - DP02[3:0] - 1G/2.5G/10G Ethernet (using GTH Transceivers @ Upto 16Gbps/lane)
    - DP03[3:0] - 1G/2.5G/10G Ethernet (using GTH Transceivers @ Upto 16Gbps/lane)
  - Control Plane Port
    - CPutp[6:0] - 1G/2.5G/10G/25G Ethernet (using GTY Transceivers @ Upto 25Gbps/lane)
    - CSutp01 - 1G/2.5G/10G/25G Ethernet (using GTY Transceivers @ Upto 25Gbps/lane)
  - Utility Plane
    - System Control Signals (Maskable Reset)
  - Maintenance Port
    - MP01 and MP02
- **MT Ferrule Optical Interconnect - P2B**
  - 8 Fiber Optical Transceiver using two Firefly Connector (using GTY Transceivers @ Upto 28.125Gbps)

3U VPX Front Panel Features

- USB3.0 & USB 2.0 through USB Type-C Connector x 1
- Display Port through USB Type-C Connector x 1
- 10/100/1000Mbps Ethernet through 9 Pin Header x 1
- 3 Pin Debug UART Header x 1

Other On-Board Features

- PCIe Gen2 x 1 through M.2(Key-M) Connector x 1
- Temperature Sensor
- Elapse Time Counter
- Quad User LEDs
- Reset Switch
- Clock Synthesizer and Clock Buffers for GTY, GTH, and GTR Transceiver Reference clocks

General Specification

- Power Supply : +12VDC +/- 5% input from VPX Connector
- Form Factor : 3U- VPX (160mm X 100mm)

2.3 Zynq Ultrascale+ MPSoC

The Zynq Ultrascale+ MPSoC (ZU11/17/19EG) 3U-VPX Plug-in Module is based on Xilinx Zynq Ultrascale+ MPSoC (ZU11/17/19EG) with FFVC1760 package. Zynq Ultrascale+ MPSoC family integrates Processing system (PS) and Xilinx programmable logic (PL) in a single device. MPSoC's Processing system includes feature-rich Quad-core ARM Cortex-A53 MPCore up to 1.5 GHz of Application processor, Dual-core ARM Cortex-R5 MPCore up to 600MHz and Mali™-400 MP2 of Graphics Processor. The Block Diagram of Zynq Ultrascale+ MPSoC from Xilinx website is shown below for reference.

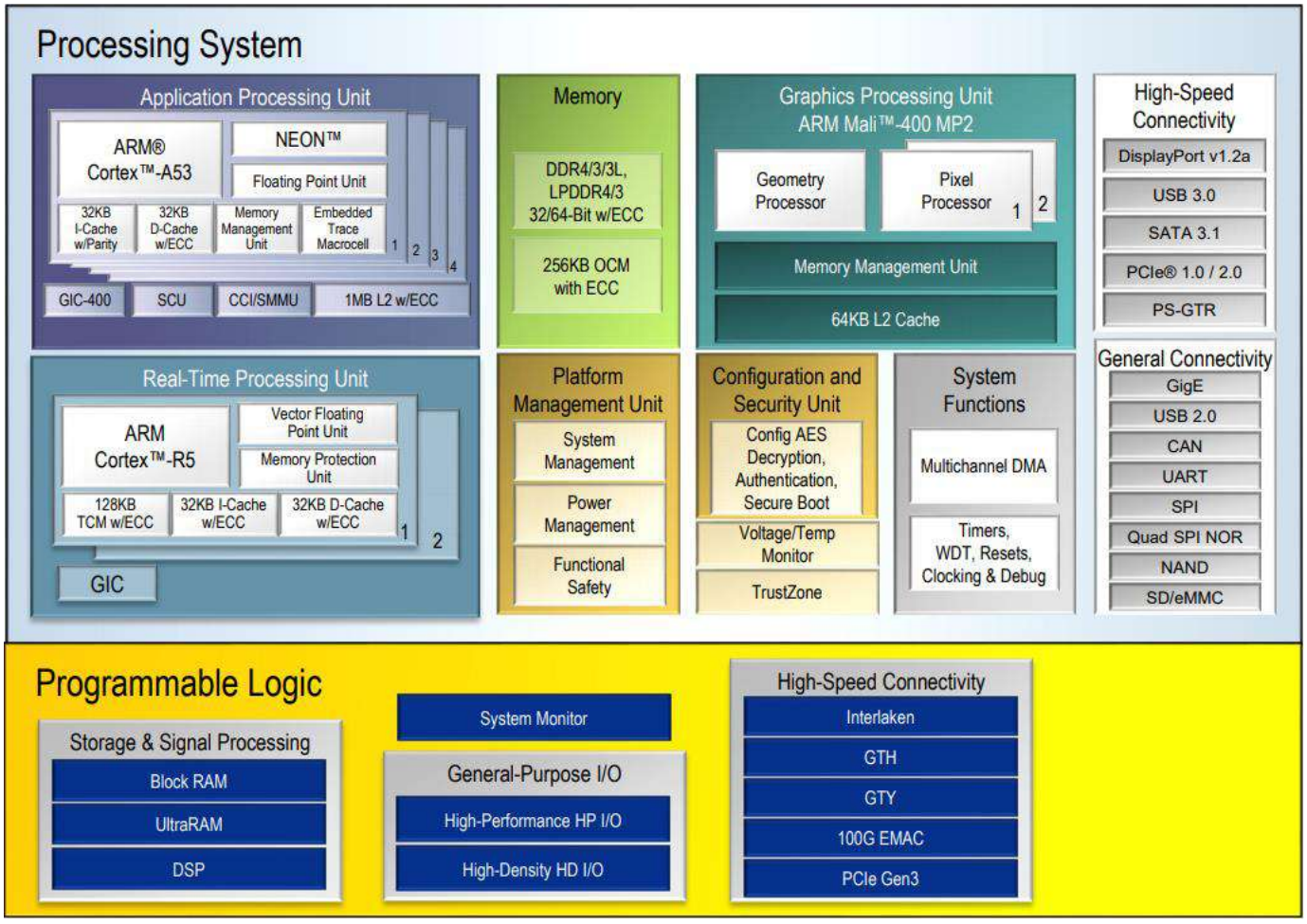

Figure 2: Zynq Ultrascale+ MPSoC CPU Simplified Block Diagram

Note: Please refer the latest Zynq Ultrascale+ MPSoC Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Zynq Ultrascale+ MPSoC SOM is compatible to ZU11EG, ZU17EG and ZU19EG MPSoC devices and feature comparison between these devices are shown below.

	ZU11EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache		
Real-Time Processing Unit	Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM		
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3;External Quad-SPI; NAND; eMMC		
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters		
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII		
Graphic Processing Unit	Arm Mali™-400 MP2; 64KB L2 Cache		
System Logic Cells	6,53,100	9,26,194	11,43,450
CLB Flip-Flops	5,97,120	8,46,806	10,45,440
CLB LUTs	2,98,560	4,23,403	5,22,720
Distributed RAM (Mb)	9.1	8	9.8
Block RAM Blocks	600	796	984
Block RAM (Mb)	21.1	28	34.6
UltraRAM Blocks	80	102	128
UltraRAM (Mb)	22.5	28.7	36
DSP Slices	2,928	1,590	1,968
CMTs	8	11	11
Max. HP I/O	416	416	416
Max. HD I/O	96	96	96
System Monitor	2	2	2
GTH Transceiver 16.3Gb/s	32	32	32
GTY Transceiver 28Gb/s	16	16	16
Transceiver Fractional PLLs	24	36	36
PCIe Gen3 x16	4	4	5
150G Interlaken	1	2	4
100G Ethernet w/ RS-FEC	2	2	4

Figure 3: Zynq Ultrascale+ MPSoC Devices Comparison

2.4 Memory

2.4.1 DDR4 SDRAM with ECC for PS

The 3U VPX Plug-In Module supports 64bit, 4GB DDR4 RAM memory for MPSoC's PS. Four 16 bit, 1GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. Also it supports 8bit ECC for RAM memory. These DDR4 devices operates at 2400Mbps data rate. DDR4 memory is connected to the hard memory controller of the MPSoC PS. The RAM size can be expandable up to maximum of 8GB based on the availability of higher density 16bit DDR4 device.

2.4.2 DDR4 SDRAM1 for PL

The 3U VPX Plug-In Module supports 64bit, 4GB DDR4 RAM memory through MPSoC's PL HP Bank64, 65 & 66. Four 16 bit, 1GB DDR4 SDRAM IC is used to support RAM memory of 4GB for PL. These DDR4 devices operates at 2666Mbps data rate. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The 3U VPX Plug-In Module supports 300MHz LVDS Oscillator on board for PL DDR4 reference clock and connected to Bank64 AT21 & AT22 dedicated clock input pins through AC Coupling capacitors.

Note: Zynq Ultrascale+ MPSoC SOM with -1 speed grade MPSoC can support upto 2400Mbps datarate for PL DDR4.

2.4.3 DDR4 SDRAM2 for PL

The 3U VPX Plug-In Module supports 64bit, 4GB DDR4 RAM memory through MPSoC's PL HP Bank69, 70 & 71. Four 16 bit, 1GB DDR4 SDRAM IC is used to support RAM memory of 4GB for PL. These DDR4 devices operates at 2666Mbps datarate. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The 3U VPX Plug-In Module supports 300MHz LVDS Oscillator on board for PL DDR4 reference clock and connected to Bank69 D32 & E32 dedicated clock input pins through AC Coupling capacitors.

Note: Zynq Ultrascale+ MPSoC SOM with -1 speed grade MPSoC can support upto 2400Mbps datarate for PL DDR4.

2.4.4 eMMC Flash

The 3U VPX Plug-In Module supports 8GB eMMC Flash memory for Boot & Storage of Zynq Ultrascale+ MPSoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the MPSOC's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC4.51 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

2.5 3U-VPX Backplane Connectors

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module conforms to below mentioned Module Profile & Slot Profile defined in OpenVPX System Standard ANSI/VITA 65.0-2019.

- Module Profile : MOD3-SWH-4F1U7U1J-16.8.7-n
- Slot Profile : SLT3-SWH-4F1U7U1J-14.8.7-n
- Slot Pitch : 1 inch Conduction Cooled

*Note: This 3U-VPX Plug-In module also compatible with more slot profiles and the complete compatible list is provided in section **5.1.5.1Compatible VPX Slot Profiles.** Even though this 3U-VPX Plug-In module is compatible with many slot profiles, this document explains interfaces with respect to only 'SLT3-SWH-4F1U7U1J-14.8.7-n' slot profile.*

This 3U-VPX Plug-in Module supports two VPX Backplane connectors P0+P1A (J5) and P1B+P2A (J8) to support standard ANSI/VITA 65.0. Also it support P2B (J11) MT Ferrule mechnical optical interconnect to support standard ANSI/VITA 66.4.

P0+P1A Connector Part Number : 2313237-1 from TE Connectivity
P1B+P2A Connector Part Number : 2302785-1 from TE Connectivity
P2B Connector Part Number : 2226881-1 from TE Connectivity
Right Angle Keyed Guide : 2000713-5 from TE Connectivity

The features which are supported on these 3U-VPX connectors are explained in the following section.

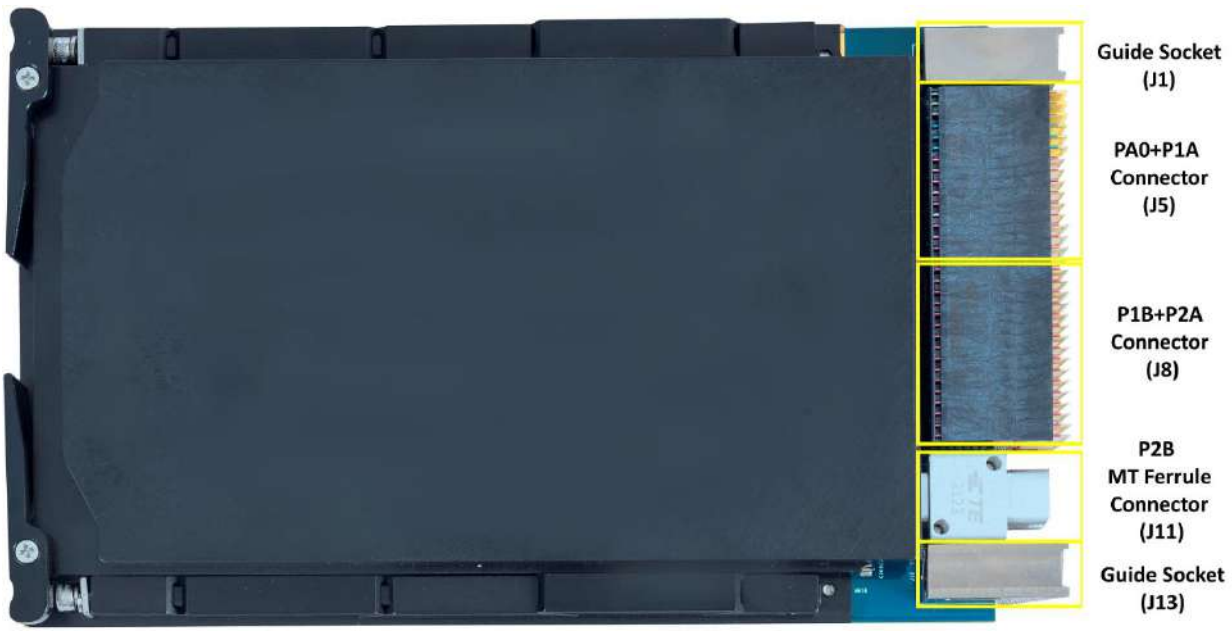

Figure 4: 3U-VPX Backplane Connectors

2.5.1 3U VPX Connector (P0+P1A)

The VPX P0+P1A Connector (J5) supports the below mentioned interface from Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module.

- Data Plane Port
  - DP01[3:0] - 1G/2.5G/10G Ethernet or PCIe Gen3 (using PL GTH Transceivers Bank225)
- Data Switch Port
  - DS01[3:0] - 1G/2.5G/10G Ethernet or PCIe Gen3 (using PL GTH Transceivers Bank224)
- Utility Plane
  - System Reference Clocks (REF_CLK, AUX_CLK)
  - System Control Signals (SYSRESET, NVMRO, SYS_CON, SM Bus, Geographic Address Field, JTAG)
  - Bussed GPIO (GDiscrete1)
  - Power Input (12V VDC, 3.3V_AUX, VBAT)

This 112Pin VPX connector P0+P1A (J5) is shown below.

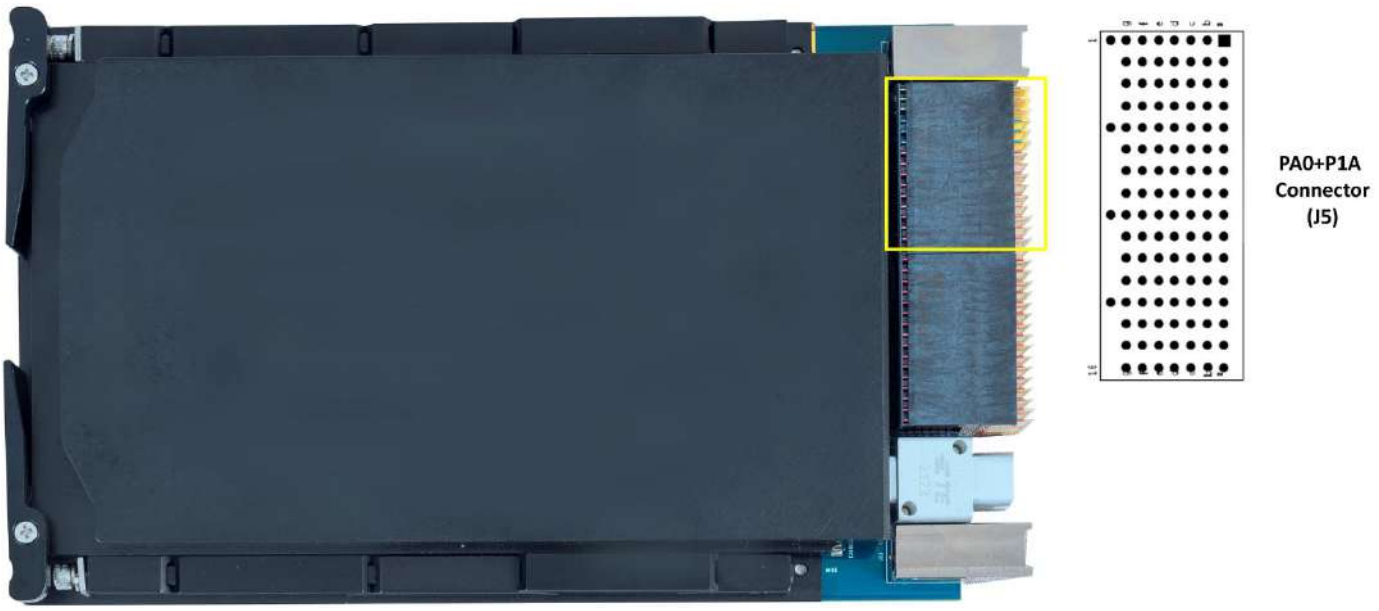

Figure 5 VPX Connector P0+P1A

This 112Pin VPX connector's P0+P1A (J5) pin mapping is shown below.

	G	F	E	D	C	B	A
P0							
1	+12VDC	+12VDC	+12VDC	No Pad	No Pad	No Pad	No Pad
2	+12VDC	+12VDC	+12VDC	No Pad	No Pad	No Pad	No Pad
3	No Pad	No Pad	No Pad	No Pad	No Pad	No Pad	No Pad
4	IPMB_B_SCL	IPMB_B_SDA	DGND	No Pad	DGND	SYSRESET_F	NVMRO
5	GAP	GA4	DGND	+3.3V_AUX	DGND	IPMB_A_SCL	IPMB_A_SD A
6	GA3	GA2	DGND	No Pad	DGND	GA1	GA0
7	TCK	DGND	TDO	TDI	DGND	TMS	TRST
8	DGND	REF_CLK-	REF_CLK+	DGND	AUX_CLK-	AUX_CLK+	DGND
P1A							
1	GDiscrete1	DGND	DS01-TD0-	DS01-TD0+	DGND	DS01-RD0-	DS01-RD0+
2	DGND	DS01-TD1-	DS01-TD1+	DGND	DS01-RD1-	DS01-RD1+	DGND
3	P1-VBAT	DGND	DS01-TD2-	DS01-TD2+	DGND	DS01-RD2-	DS01-RD2+
4	DGND	DS01-TD3-	DS01-TD3+	DGND	DS01-RD3-	DS01-RD3+	DGND
5	SYS_CON	DGND	DP01-TD0-	DP01-TD0+	DGND	DP01-RD0-	DP01-RD0+
6	DGND	DP01-TD1-	DP01-TD1+	DGND	DP01-RD1-	DP01-RD1+	DGND
7	Reserved	DGND	DP01-TD2-	DP01-TD2+	DGND	DP01-RD2-	DP01-RD2+
8	DGND	DP01-TD3-	DP01-TD3+	DGND	DP01-RD3-	DP01-RD3+	DGND

Figure 6 VPX Connector P0+P1A Pin Mapping

2.5.1.1 Data Plane Port

The following section explains about the features supported from the Data Plane of P0+P1A VPX Connector in Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

2.5.1.1.1 DP01[3:0]

The DP01 or Data Plane 01, is a dedicated interface responsible for handling application and external data traffic such as the 10GigE switch fabric. In compliance with the Vita 65.0 Specification, the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module utilizes the Data Plane to enable high-speed data communication with support for 1GBase-KX/10Gbase-KR protocols.

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) VPX Plug-in Module supports 4 GTH transceivers from Bank225 for DP01 interface through VPX connector. The Transmitter lanes of PL GTH Bank225 are directly connected to VPX Connector P0+P1A (J5) and Receiver lanes are connected through 0.01uF AC caps to VPX Connector P0+P1A (J5).

For more details on DP01 pinouts on VPX Connector, refer the below table.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D13	DP01-TD0+	MGTHTXP0_225	225	AR6	O, DIFF	GTH Bank225 channel0 High speed differential transmitter positive.
E13	DP01-TD0-	MGTHTXN0_225	225	AR5	O, DIFF	GTH Bank225 channel0 High speed differential transmitter negative.
B13	DP01-RD0-	MGTHRXN0_225	225	AT3	I, DIFF	GTH Bank225 channel0 High speed differential receiver negative.
A13	DP01-RD0+	MGTHRXP0_225	225	AT4	I, DIFF	GTH Bank225 channel0 High speed differential receiver positive.
E14	DP01-TD1+	MGTHTXP1_225	225	AP8	O, DIFF	GTH Bank225 channel1 High speed differential transmitter positive.
F14	DP01-TD1-	MGTHTXN1_225	225	AP7	O, DIFF	GTH Bank225 channel1 High speed differential transmitter negative.
C14	DP01-RD1-	MGTHRXN1_225	225	AR1	I, DIFF	GTH Bank225 channel1 High speed differential receiver negative.
B14	DP01-RD1+	MGTHRXP1_225	225	AR2	I, DIFF	GTH Bank225 channel1 High speed differential receiver positive.
D15	DP01-TD2+	MGTHTXP2_225	225	AN6	O, DIFF	GTH Bank225 channel2 High speed differential transmitter positive.
E15	DP01-TD2-	MGTHTXN2_225	225	AN5	O, DIFF	GTH Bank225 channel2 High speed differential transmitter negative.
B15	DP01-RD2-	MGTHRXN2_225	225	AP3	I, DIFF	GTH Bank225 channel2 High speed differential receiver negative.
A15	DP01-RD2+	MGTHRXP2_225	225	AP4	I, DIFF	GTH Bank225 channel2 High speed differential receiver positive.
E16	DP01-TD3+	MGTHTXP3_225	225	AM8	O, DIFF	GTH Bank225 channel3 High speed differential transmitter positive.
F16	DP01-TD3-	MGTHTXN3_225	225	AM7	O, DIFF	GTH Bank225 channel3 High speed differential transmitter negative.
C16	DP01-RD3-	MGTHRXN3_225	225	AN1	I, DIFF	GTH Bank225 channel3 High speed differential receiver negative.
B16	DP01-RD3+	MGTHRXP3_225	225	AN2	I, DIFF	GTH Bank225 channel3 High speed differential receiver positive.

2.5.1.2 Data Switch Port

The following section explains about the features supported from the Data Switch Port of P0+P1A VPX Connector in Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

2.5.1.2.1 DS01[3:0]

The DS01 refers to Data Switch Ports, the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module's DS01 or Switch Profile 0 slot is designed to accommodate a switch module that provides advanced interconnection capabilities with the VPX System. It facilitates high-speed data communication to enable high-speed data communication with support for 1GBase-KX/10Gbase-KR protocols.

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports 4 GTH transceivers from Bank224 for DS01 interface through VPX connector. The Transmitter lanes of PL GTH Bank224 are directly connected to VPX Connector P0+P1A (J5) and Receiver lanes are connected through 0.01uF AC caps to VPX Connector P0+P1A (J5).

For more details on DS01 pinouts on VPX Connector, refer the below table.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D9	DS01-TD0+	MGTHTXP0_224	224	AY4	O, DIFF	GTH Bank224 channel0 High speed differential transmitter positive.
E9	DS01-TD0-	MGTHTXN0_224	224	AY3	O, DIFF	GTH Bank224 channel0 High speed differential transmitter negative.
B9	DS01-RD0-	MGTHRXN0_224	224	BA1	I, DIFF	GTH Bank224 channel0 High speed differential receiver negative.
A9	DS01-RD0+	MGTHRXP0_224	224	BA2	I, DIFF	GTH Bank224 channel0 High speed differential receiver positive.
E10	DS01-TD1+	MGTHTXP1_224	224	AW6	O, DIFF	GTH Bank224 channel1 High speed differential transmitter positive.
F10	DS01-TD1-	MGTHTXN1_224	224	AW5	O, DIFF	GTH Bank224 channel1 High speed differential transmitter negative.
C10	DS01-RD1-	MGTHRXN1_224	224	AW1	I, DIFF	GTH Bank224 channel1 High speed differential receiver negative.
B10	DS01-RD1+	MGTHRXP1_224	224	AW2	I, DIFF	GTH Bank224 channel1 High speed differential receiver positive.
D11	DS01-TD2+	MGTHTXP2_224	224	AU6	O, DIFF	GTH Bank224 channel2 High speed differential transmitter positive.
E11	DS01-TD2-	MGTHTXN2_224	224	AU5	O, DIFF	GTH Bank224 channel2 High speed differential transmitter negative.
B11	DS01-RD2-	MGTHRXN2_224	224	AV3	I, DIFF	GTH Bank224 channel2 High speed differential receiver negative.
A11	DS01-RD2+	MGTHRXP2_224	224	AV4	I, DIFF	GTH Bank224 channel2 High speed differential receiver positive.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
E12	DS01-TD3+	MGTHTXP3_224	224	AT8	O, DIFF	GTH Bank224 channel3 High speed differential transmitter positive.
F12	DS01-TD3-	MGTHTXN3_224	224	AT7	O, DIFF	GTH Bank224 channel3 High speed differential transmitter negative.
C12	DS01-RD3-	MGTHRXN3_224	224	AU1	I, DIFF	GTH Bank224 channel3 High speed differential receiver negative.
B12	DS01-RD3+	MGTHRXP3_224	224	AU2	I, DIFF	GTH Bank224 channel3 High speed differential receiver positive.

2.5.1.3 Utility Plane Port

The following section explains about the features supported from the Utility Plane of P0+P1A VPX Connector of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

2.5.1.3.1 System Reference Clocks

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports two LVDS clocks - Reference clock input and Auxiliary clock input. These two clocks are connected from VPX connector (J5) to PL Bank GC pins through 0.1uF AC cap.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
REF CLK						
E8	REF_CLK+	IO_L11P_T1U_N8_GC_68	68	G17	I, LVDS	PL Bank68 IO11 differential Global Clock positive. *Note: This clock is optionally connected to Clock Synthesizer (U7) IN1 pin through resistor and by default not populated.*
F8	REF_CLK-	IO_L11N_T1U_N9_GC_68	68	F17	I, LVDS	PL Bank68 IO11 differential Global Clock negative. *Note: This clock is optionally connected to Clock Synthesizer (U7) IN1 pin through resistor and by default not populated.*
AUX CLK						
B8	AUX_CLK+	IO_L13P_T2L_N0_GC_QBC_68	68	F14	I, LVDS	PL Bank68 IO13 differential Global Clock positive.
C8	AUX_CLK-	IO_L13N_T2L_N1_GC_QBC_68	68	E14	I, LVDS	PL Bank68 IO13 differential Global Clock negative.

2.5.1.3.2 System Control Signals

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports four control signals to VPX connector(J5). These Control signals are connected Zynq US+ MPSoC PS. These signals are connected from PS GPIOs to VPX connector through Level translator (U2).

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A4	NVMRO	PS_MIO45_501	501	T29	IO, 3V3 LVCMOS	Non-Volatile Memory Read Only.
B4	SYSRESET	NA	NA	NA	I, 3V3 LVCMOS	System Reset.
G9	GDiscrete1	PS_MIO43_501	501	R30	IO,3V3 LVCMOS/100K PU	General Purpose Input/ Output.
G13	SYS_CON	PS_MIO3_500	500	AM30	IO,3V3 LVCMOS	System Controller.

2.5.1.3.3 System Management Bus

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports two I2C interfaces on the VPX connector (J5) for IPMB (Intelligent Platform Management Bus). One I2C interface is from the PS, and one I2C interface from the PL is supported. Dedicated hardware supervision and management of hardware resources are expanded from the 3U-VPX Plug-in Module to the Backplane. The PS I2C is connected to the VPX connector as well as the on-board peripherals.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
IPMB_A						
B5	IPMB_A_SCL	PS_MIO10_500	500	AK30	O, 3V3 LVCMOS	I2C0 Clock.
A5	IPMB_A_SDA	PS_MIO11_500	500	AK32	IO, 3V3 LVCMOS	I2C0 Data.
IPMB_B						
G4	IPMB_B_SCL	IO_L17P_T2U_N8_AD10P_68	68	A14	O, 3V3 LVCMOS	I2C0 Clock.
F4	IPMB_B_SDA	IO_L17N_T2U_N9_AD10N_68	68	A13	IO, 3V3 LVCMOS	I2C0 Data.

2.5.1.3.4 JTAG

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports JTAG signals from Zynq Ultrascale+ MPSoC to VPX connector(J5). JTAG signals from MPSoC is directly connected to VPX Connector (J8) through Level translator(U1). JTAG-HS2/ JTAG-HS3 programming cable can be used for programming and debugging purpose.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B7	TMS	PS_JTAG_TMS	503	AD26	I, 3V3 LVCMOS	JTAG test mode select.
D7	TDI	PS_JTAG_TDI	503	AD25	I, 3V3 LVCMOS	JTAG test data input.
E7	TDO	PS_JTAG_TDO	503	AD27	O, 3V3 LVCMOS	JTAG test data output
G7	TCK	PS_JTAG_TCK	503	AC26	I, 3V3 LVCMOS	JTAG test Clock.

2.5.1.3.5 Geographical Address Field and Parity

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports five Geographical address signals and one parity signal to VPX connector(J5). These Geographical address and parity signals are connected Zynq US+ MPSoC PS. These signals are connected from Zynq Ultrascale+ MPSoC PS to VPX connector through Level translator(U4).

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A6	GA0	PS_MIO51_501	501	W30	I, 3V3 LVCMOS/ 10K PU	Geographical Address 0.
B6	GA1	PS_MIO50_501	501	V29	I, 3V3 LVCMOS/ 10K PU	Geographical Address 1.
F6	GA2	PS_MIO46_501	501	U28	I, 3V3 LVCMOS/ 10K PU	Geographical Address 2.
G6	GA3	PS_MIO47_501	501	T28	I, 3V3 LVCMOS/ 10K PU	Geographical Address 3.
F5	GA4	PS_MIO48_501	501	V30	I, 3V3 LVCMOS/ 10K PU	Geographical Address 4.
G5	GAP	PS_MIO49_501	501	U29	I, 3V3 LVCMOS/ 10K PU	Geographical Address Parity.

2.5.1.3.6 Power

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module works with 12 power input (VCC) from VPX Connector and generates all other required powers internally On-3U-VPX Plug-in Module itself. Also 3.3V AUX is input to the 3U-VPX Plug-in Module through VPX connector(J5).

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
E1, E2, F1, F2 G1, G2	+12VDC	NA	NA	NA	I, 12V Power	Input Supply Voltage.
D5	+3.3V_AUX	NA	NA	NA	I,3.3V Power	AUX Supply Voltage.

2.5.2 3U VPX Connector (P1B+P2A)

The VPX-P1B+P2A Connector (J8) supports the below mentioned interfaces from Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module.

- Data Plane Port
  - DP02[3:0] - 1G/2.5G/10G Ethernet (using GTH Transceivers @ Upto 16Gbps/lane)
  - DP03[3:0] - 1G/2.5G/10G Ethernet (using GTH Transceivers @ Upto 16Gbps/lane)
- Control Plane Port
  - CPutp[6:0] - 1G/2.5G/10G/25G Ethernet (using GTY Transceivers @ Upto 25Gbps/lane)
  - CSutp01 - 1G/2.5G/10G/25G Ethernet (using GTY Transceivers @ Upto 25Gbps/lane)
- Utility Plane
  - System Control Signals (Maskable Reset)
- Maintenance Port
  - MP01 and MP02

This 112Pin VPX connector P1B+P2A is shown below.

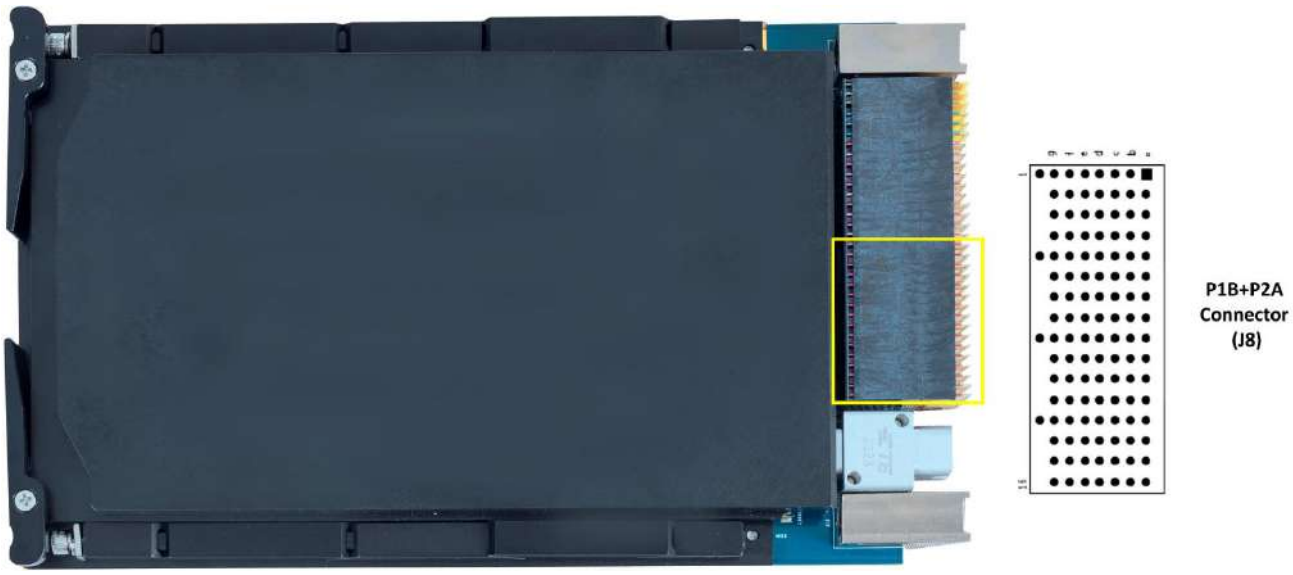

Figure 7 VPX Connector P1B+P2A

This 112Pin VPX connector's P1B+P2A (J8) pin mapping is shown below.

P1B							
1	MP01-TD	DGND	DP02-TD0-	DP02-TD0+	DGND	DP02-RD0-	DP02-RD0+
2	DGND	DP02-TD1-	DP02-TD1+	DGND	DP02-RD1-	DP02-RD1+	DGND
3	MP01-RD	DGND	DP02-TD2-	DP02-TD2+	DGND	DP02-RD2-	DP02-RD2+
4	DGND	DP02-TD3-	DP02-TD3+	DGND	DP02-RD3-	DP02-RD3+	DGND
5	Reserved	DGND	DP03-TD0-	DP03-TD0+	DGND	DP03-RD0-	DP03-RD0+
6	DGND	DP03-TD1-	DP03-TD1+	DGND	DP03-RD1-	DP03-RD1+	DGND
7	MaskableReset	DGND	DP03-TD2-	DP03-TD2+	DGND	DP03-RD2-	DP03-RD2+
8	DGND	DP03-TD3-	DP03-TD3+	DGND	DP03-RD3-	DP03-RD3+	DGND
P2A							
9	DGND	DGND	DGND	DGND	DGND	DGND	DGND
10	DGND	CPutp06-TD-	CPutp06-TD+	DGND	CPutp06-RD-	CPutp06-RD+	DGND
11	MP02-TD	DGND	CPutp05-TD-	CPutp05-TD+	DGND	CPutp05-RD-	CPutp05-RD+
12	DGND	CPutp04-TD-	CPutp04-TD+	DGND	CPutp04-RD-	CPutp04-RD+	DGND
13	MP02-RD	DGND	CPutp03-TD-	CPutp03-TD+	DGND	CPutp03-RD-	CPutp03-RD+
14	DGND	CPutp02-TD-	CPutp02-TD+	DGND	CPutp02-RD-	CPutp02-RD+	DGND
15	Reserved	DGND	CPutp01-TD-	CPutp01-TD+	DGND	CPutp01-RD-	CPutp01-RD+
16	DGND	CSutp01-TD-	CSutp01-TD+	DGND	CSutp01-RD-	CSutp01-RD+	DGND

Figure 8: VPX Connector P1B+P2A Pin Mapping

2.5.2.1 Data Plane Port

The following section explains about the features supported from Data Plane of P1B+P2A VPX Connector in Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

2.5.2.1.1 DP02[3:0]

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports 4 GTH transceivers from Bank230 for DP02 (Data Plane) through VPX connector which supports 1GBase-KX/10GBase-KR. The Transmitter lanes of PL GTH Bank230 is directly connected to VPX Connector(J8) and Receiver lanes are connected through 0.01uF AC caps to VPX Connector(J8) as recommended.

For more details on DP02 pinouts on VPX connector, refer the below table.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D1	DP02-TD0+	MGTHTXP0_230	230	R6	O, DIFF	GTH Bank230 channel0 High speed differential transmitter positive.
E1	DP02-TD0-	MGTHTXN0_230	230	R5	O, DIFF	GTH Bank230 channel0 High speed differential transmitter negative.
A1	DP02-RD0+	MGTHRXP0_230	230	T4	I, DIFF	GTH Bank230 channel0 High speed differential receiver positive.
B1	DP02-RD0-	MGTHRXN0_230	230	T3	I, DIFF	GTH Bank230 channel0 High speed differential receiver negative.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
E2	DP02-TD1+	MGTHTXP1_230	230	P8	O, DIFF	GTH Bank230 channel1 High speed differential transmitter positive.
F2	DP02-TD1-	MGTHTXN1_230	230	P7	O, DIFF	GTH Bank230 channel1 High speed differential transmitter negative.
B2	DP02-RD1+	MGTHRXP1_230	230	R2	I, DIFF	GTH Bank230 channel1 High speed differential receiver positive.
C2	DP02-RD1-	MGTHRXN1_230	230	R1	I, DIFF	GTH Bank230 channel1 High speed differential receiver negative.
D3	DP02-TD2+	MGTHTXP2_230	230	N6	O, DIFF	GTH Bank230 channel2 High speed differential transmitter positive.
E3	DP02-TD2-	MGTHTXN2_230	230	N5	O, DIFF	GTH Bank230 channel2 High speed differential transmitter negative.
A3	DP02-RD2+	MGTHRXP2_230	230	P4	I, DIFF	GTH Bank230 channel2 High speed differential receiver positive.
B3	DP02-RD2-	MGTHRXN2_230	230	P3	I, DIFF	GTH Bank230 channel2 High speed differential receiver negative.
E4	DP02-TD3+	MGTHTXP3_230	230	M8	O, DIFF	GTH Bank230 channel3 High speed differential transmitter positive.
F4	DP02-TD3-	MGTHTXN3_230	230	M7	O, DIFF	GTH Bank230 channel3 High speed differential transmitter negative.
B4	DP02-RD3+	MGTHRXP3_230	230	N2	I, DIFF	GTH Bank230 channel3 High speed differential receiver positive.
C4	DP02-RD3-	MGTHRXN3_230	230	N1	I, DIFF	GTH Bank230 channel3 High speed differential receiver negative.

2.5.2.1.2 DP03[3:0]

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports 4 GTH transceivers from Bank231 for DP01 (Data Plane) through VPX connector to support 1GBase-KX/10GBase-KR. The Transmitter lanes of PL GTH Bank231 are directly connected to VPX Connector(J8) and Receiver lanes are connected through 0.01uF AC caps to VPX Connector(J8) as recommended.

For more details on DP03 pinouts on VPX connector, refer the below table.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D5	DP03-TD0+	MGTHTXP0_231	231	L6	O, DIFF	GTH Bank231 channel0 High speed differential transmitter positive.
E5	DP03-TD0-	MGTHTXN0_231	231	L5	O, DIFF	GTH Bank231 channel0 High speed differential transmitter negative.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A5	DP03-RD0+	MGTHRXP0_231	231	M4	I, DIFF	GTH Bank231 channel0 High speed differential receiver positive.
B5	DP03-RD0-	MGTHRXN0_231	231	M3	I, DIFF	GTH Bank231 channel0 High speed differential receiver negative.
E6	DP03-TD1+	MGTHTXP1_231	231	K4	O, DIFF	GTH Bank231 channel1 High speed differential transmitter positive.
F6	DP03-TD1-	MGTHTXN1_231	231	K3	O, DIFF	GTH Bank231 channel1 High speed differential transmitter negative.
B6	DP03-RD1+	MGTHRXP1_231	231	L2	I, DIFF	GTH Bank231 channel1 High speed differential receiver positive.
C6	DP03-RD1-	MGTHRXN1_231	231	L1	I, DIFF	GTH Bank231 channel1 High speed differential receiver negative.
D7	DP03-TD2+	MGTHTXP2_231	231	J6	O, DIFF	GTH Bank231 channel2 High speed differential transmitter positive.
E7	DP03-TD2-	MGTHTXN2_231	231	J5	O, DIFF	GTH Bank231 channel2 High speed differential transmitter negative.
A7	DP03-RD2+	MGTHRXP2_231	231	J2	I, DIFF	GTH Bank231 channel2 High speed differential receiver positive.
B7	DP03-RD2-	MGTHRXN2_231	231	J1	I, DIFF	GTH Bank231 channel2 High speed differential receiver negative.
E8	DP03-TD3+	MGTHTXP3_231	231	H4	O, DIFF	GTH Bank231 channel3 High speed differential transmitter positive.
F8	DP03-TD3-	MGTHTXN3_231	231	H3	O, DIFF	GTH Bank231 channel3 High speed differential transmitter negative.
B8	DP03-RD3+	MGTHRXP3_231	231	G2	I, DIFF	GTH Bank231 channel3 High speed differential receiver positive.
C8	DP03-RD3-	MGTHRXN3_231	231	G1	I, DIFF	GTH Bank231 channel3 High speed differential receiver negative.

2.5.2.2 Control Plane Port

The following section explains about the features supported from Control Plane of P1B+P2A VPX Connector in Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

2.5.2.2.1 CPutp[6:0]

The CPutp (Control Plane User Transfer Protocol) facilitates the exchange of control and management information between different modules or components within the system.

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports this CPutp interface using 6 GTY transceivers from Bank130 & 131 to establish a high-speed connection between the module and the backplane via the VPX connector. The Transmitter lanes of PL GTY Bank130 & 131 is directly connected to VPX Connector(J8) and Receiver lanes are connected through 0.01uF AC caps to VPX Connector(J8) as recommended.

For more details on CPutp pinouts on VPX connector, refer the below table.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D15	CPutp01-TD+	MGTYTXP0_130	130	M34	O, DIFF	GTY Bank130 channel0 High speed differential transmitter positive.
E15	CPutp01-TD-	MGTYTXN0_130	130	M35	O, DIFF	GTY Bank130 channel0 High speed differential transmitter negative.
A15	CPutp01-RD+	MGTYRXP0_130	130	L41	I, DIFF	GTY Bank130 channel0 High speed differential receiver positive.
B15	CPutp01-RD-	MGTYRXN0_130	130	L42	I, DIFF	GTY Bank130 channel0 High speed differential receiver negative.
E14	CPutp02-TD+	MGTYTXP1_130	130	L36	O, DIFF	GTY Bank130 channel1 High speed differential transmitter positive.
F14	CPutp02-TD-	MGTYTXN1_13	130	L37	O, DIFF	GTY Bank130 channel1 High speed differential transmitter negative.
B14	CPutp02-RD+	MGTYRXP1_130	130	K39	I, DIFF	GTY Bank130 channel1 High speed differential receiver positive.
C14	CPutp02-RD-	MGTYRXN1_130	130	K40	I, DIFF	GTY Bank130 channel1 High speed differential receiver negative.
D13	CPutp03-TD+	MGTYTXP2_130	130	K34	O, DIFF	GTY Bank130 channel2 High speed differential transmitter positive.
E13	CPutp03-TD-	MGTYTXN2_130	130	K35	O, DIFF	GTY Bank130 channel2 High speed differential transmitter negative.
A13	CPutp03-RD+	MGTYRXP2_130	130	J41	I, DIFF	GTY Bank130 channel2 High speed differential receiver positive.
B13	CPutp03-RD-	MGTYRXN2_130	130	J42	I, DIFF	GTY Bank130 channel2 High speed differential receiver negative.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
E12	CPutp04-TD+	MGTYTXP0_131	131	H34	O, DIFF	GTY Bank131 channel0 High speed differential transmitter positive.
F12	CPutp04-TD	MGTYTXN0_131	131	H35	O, DIFF	GTY Bank131 channel0 High speed differential transmitter negative.
B12	CPutp04-RD+	MGTYRXP0_131	131	G41	I, DIFF	GTY Bank131 channel0 High speed differential receiver positive.
C12	CPutp04-RD-	MGTYRXN0_131	131	G42	I, DIFF	GTY Bank131 channel0 High speed differential receiver negative.
D11	CPutp05-TD+	MGTYTXP1_131	131	G36	O, DIFF	GTY Bank131 channel1 High speed differential transmitter positive.
E11	CPutp05-TD-	MGTYTXN1_131	131	G37	O, DIFF	GTY Bank131 channel1 High speed differential transmitter negative.
A11	CPutp05-RD+	MGTYRXP1_131	131	F39	I, DIFF	GTY Bank131 channel1 High speed differential receiver positive.
B11	CPutp05-RD-	MGTYRXN1_131	131	F40	I, DIFF	GTY Bank131 channel1 High speed differential receiver negative.
E10	CPutp06-TD+	MGTYTXP2_131	131	F34	O, DIFF	GTY Bank131 channel2 High speed differential transmitter positive.
F10	CPutp06-TD-	MGTYTXN2_131	131	F35	O, DIFF	GTY Bank131 channel2 High speed differential transmitter negative.
B10	CPutp06-RD+	MGTYRXP2_131	131	E41	I, DIFF	GTY Bank131 channel2 High speed differential receiver positive.
C10	CPutp06-RD-	MGTYRXN2_131	131	E42	I, DIFF	GTY Bank131 channel2 High speed differential receiver negative.

2.5.2.2.2 CSutp01

CSutp01 interface allows the module to efficiently transfer control and status data, contributing to improved system performance and streamlined communication between various components.

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module utilizes one GTY transceiver from Bank131 to establish a high-speed connection for the CSutp interface via the VPX connector. The Transmitter lanes of PL GTY Bank131 is directly connected to VPX Connector(J8) and Receiver lanes are connected through 0.01uF AC caps to VPX Connector(J8) as recommended.

For more details on CSutp pinout on VPX Connector, refer the below table.

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
E16	CSutp01-TD+	MGTYTXP3_131	131	E36	O, DIFF	GTY Bank131 channel3 High speed differential transmitter positive.
F16	CSutp01-TD-	MGTYTXN3_131	131	E37	O, DIFF	GTY Bank131 channel3 High speed differential transmitter negative.
B16	CSutp01-RD+	MGTYRXP3_131	131	D39	I, DIFF	GTY Bank131 channel3 High speed differential receiver positive.
C16	CSutp01-RD-	MGTYRXN3_131	131	D40	I, DIFF	GTY Bank131 channel3 High speed differential receiver negative.

2.5.2.3 Utility Plane Port

The following section explains about the features supported from Utility Plane of P1B+P2A VPX Connector in Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

2.5.2.3.1 System Control Signals

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports one Maskable Reset control signal to VPX connector(J8). This control signal is conneted from Zynq US+ MPSoC PS. This signal is connected from MPSoC to VPX connector through Level translator(U2).

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
G7	Maskable Reset	PS_MIO44_501	501	R29	I, 3V3 LVCMOS/4.7 PU	Maskable Reset

2.5.2.4 Maintenance Port

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports two MP01 and MP02 signals to VPX connector(J8). MP01 Signals are connected from Zynq US+ MPSoC PS and MP02 signals are connected Zynq US+ MPSoC PL. These signals are connected from MPSoC to VPX connector through Level translator(U1).

VPX Pin No	VPX Connector Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
G1	MP01-TD	PS_MIO08_500	500	AK33	O, 3V3 LVCMOS	Maintenance Port1 transmit data.
G3	MP01-RD	PS_MIO09_500	500	AK34	I, 3V3 LVCMOS	Maintenance Port1 receive data.
G11	MP02-TD	IO_L24P_T3U_N10_68	68	B18	O, 3V3 LVCMOS	Maintenance Port2 transmit data
G13	MP02-RD	IO_L24N_T3U_N11_68	68	A18	I, 3V3 LVCMOS	Maintenance Port2 Receive data.

2.5.3 MT Ferrule Optical Interconnect (P2B)

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports VITA66.4 MT Ferrule Optical Interconnect in the P2B Position. This MT Ferrule Optical Interconnect (J11) is physically located at the top of the board as shown below.

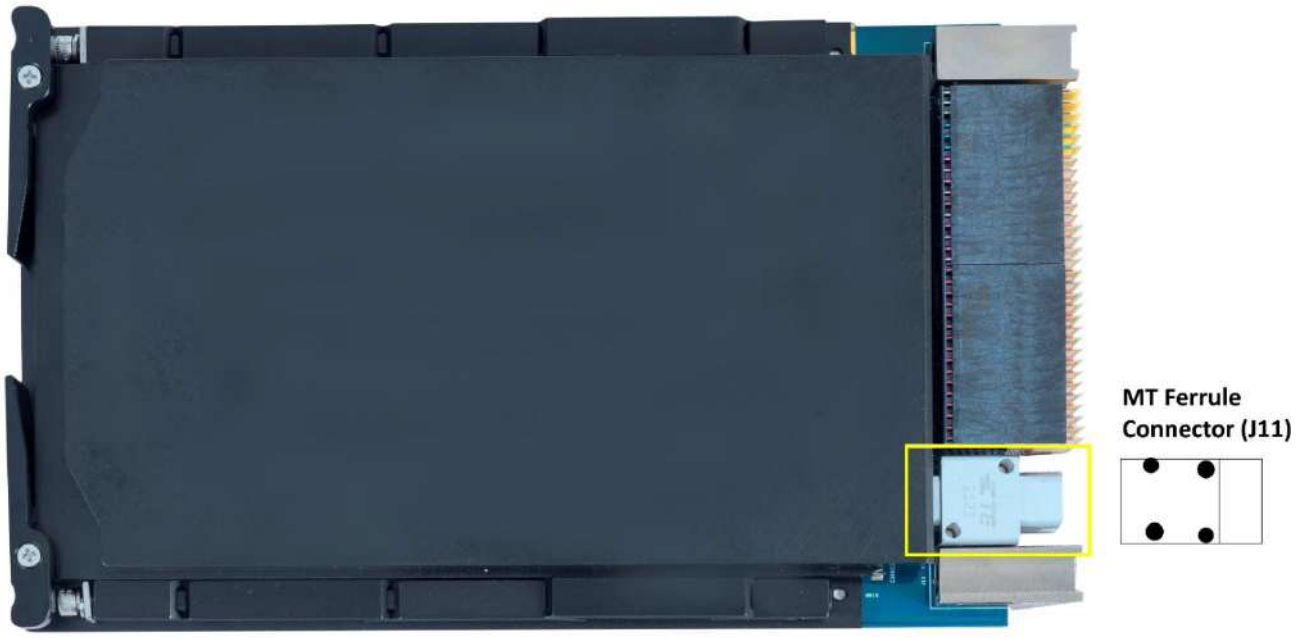

Figure 9: MT Ferrule Connector

This 3U-VPX Plug-in Module can support 8 or 16 optical fiber configuration with upto 28Gbps data rate on MT Ferrule Optical Interconnect. While using 8 optical fiber configuration (4 TX & 4 RX), single Firefly activte optical cable is used from Firefly Connector1 to MT Ferrule Optical Interconnect. And while using 16 optical fiber configuration (8 TX & 8 RX), Dual Firefly activate optical cable is used from Firefly connector 1 & 2 to MT Ferrule Optical Interconnect.

For more details on Firefly Connectors 1 & 2 pinout, refer Appendix section **5.3** & **5.4**.

Single Firefly Optical Cable:

Optical Fiber Number on MT Ferrule	Function
1	Receive Data 1
2	Receive Data 2
3	Receive Data 3
4	Receive Data 4
5	-
6	-
7	-
8	-
9	Transmit Data 1
10	Transmit Data 2
11	Transmit Data 3
12	Transmit Data 4

Figure 10: Single Firefly Optical Cable & Pinout On MT Ferrule

Note: For Dual Firefly configuration pinout, contact iWave.

2.6 3U-VPX Front Panel Features

Features which are supported from the front panel of the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module are explained in the following section.

2.6.1 USB Type-C Connector

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports one Super Speed USB3.0 host through USB Type-C connector. The PS-GTR Lane1 of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) PS is used for USB3.0 interface.

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports “FUSB302” USB Type-C controller for port detection & cable orientation and controlled through I2C0 interface of MPSoC PS. To support double-way plug in on USB Type-C connector, PS-GTR Lane2 is connected to “FUSB340” 2:1 data Switch and then connected to USB TypeC connector. The lane selection to Type-C connector (top or bottom port) is controlled through PL Bank IO “PL_C15_LVDS68_L18P”. Also USB2.0 Host interface of MPSoC PS is connected to USB Type-C connector for backward compatible USB2.0 support.

The USB3.0 port can be used as full functional host functionality which supports USB3.0 host and USB2.0 device based on Type-C . The VBUS power of this USB Type-C connector is connected through current limit power switch which can be used to switch On/Off the power based on the Host and also limits the current above 900mA in host mode. The USB PHY transceiver in SOM detects the USB functionality through USB ID pin and controls the power using the USB_PWR_EN pin.This USB Type-C connector (J16) is physically located at the bottom of the board as shown below.

Figure 11: USB Type-C Connector

Table 3: USB Type-C Pin Assignment

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
A1	GND	GND	NA	NA	NA	Power	Ground.
A2	SSTXp1	PS_MGTRTXP1_505	PS_MGTRTXP1_505	505	AF39	O, DIFF	USB3.0 Super Speed Transmit Data Positive.
A3	SSTXn1	PS_MGTRTXN1_505	PS_MGTRTXN1_505	505	AF40	O, DIFF	USB3.0 Super Speed Transmit Data Negative.
A4	VBUS	VBUS_C	NA	NA	NA	Power	5V Power Supply.
A5	CC1	CC1	NA	NA	NA	O, 5V CMOS	Configuration Channel pin1.
A6	Dp1	USB_OTG_DP	NA	NA	NA	IO, DIFF	USB2.0 Transmit Data Positive.
A7	Dn1	USB_OTG_DM	NA	NA	NA	IO, DIFF	USB2.0 Transmit Data Negative.
A8	SBU1	NC	NA	NA	NA	NC	NC.
A9	VBUS	VBUS_C	NA	NA	NA	Power	5V Power Supply.
A10	SSRXn2	PS_MGTRRXN1_505	PS_MGTRRXN1_505	505	AE42	I, DIFF	USB3.0 Super Speed Receive Data Negative.
A11	SSRXp2	PS_MGTRRXP1_505	PS_MGTRRXP1_505	505	AE41	I, DIFF	USB3.0 Super Speed Receive Data Positive.
A12	GND	GND	NA	NA	NA	Power	Ground.
B1	GND	GND	NA	NA	NA	Power	Ground.
B2	SSTXp2	PS_MGTRTXP1_505	PS_MGTRTXP1_505	505	AF39	O, DIFF	USB3.0 Super Speed Transmit Data Positive.
B3	SSTXn2	PS_MGTRTXN1_505	PS_MGTRTXN1_505	505	AF40	O, DIFF	USB3.0 Super Speed Transmit Data Negative.
B4	VBUS	VBUS_C	NA	NA	NA	Power	5V Power Supply.
B5	CC2	CC2	NA	NA	NA	O, 5V CMOS	Configuration Channel pin2.
B6	Dp1	USB_OTG_DP	NA	NA	NA	IO, DIFF	USB2.0 Transmit Data Positive.
B7	Dn1	USB_OTG_DM	NA	NA	NA	IO, DIFF	USB2.0 Transmit Data Negative.
B8	SBU2	NC	NA	NA	NA	NC	NC.
B9	VBUS	VBUS_C	NA	NA	NA	Power	5V Power Supply.
B10	SSRXn1	PS_MGTRRXN1_505	PS_MGTRRXN1_505	505	AE42	I, DIFF	USB3.0 Super Speed Receive Data Negative.
B11	SSRXp1	PS_MGTRRXP1_505	PS_MGTRRXP1_505	505	AE41	I, DIFF	USB3.0 Super Speed Receive Data Positive.
B12	GND	GND	NA	NA	NA	Power	Mechanical Pin.

2.6.2 Display Port Type-C Connector

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports one Display port connector through PS-GTR Lanes of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) PS. PS-GTR Lane3 & Lane2 is connected to Display port type-C connector to support single or dual lane display port.

The Display port type-C connector supports AUX+ & AUX- signals from the PL Bank IOs. Also, it supports Hot plug detect signal and connected to PL Bank IO. This Display Port type-C connector (J18) is physically located at the bottom of the board as shown below.

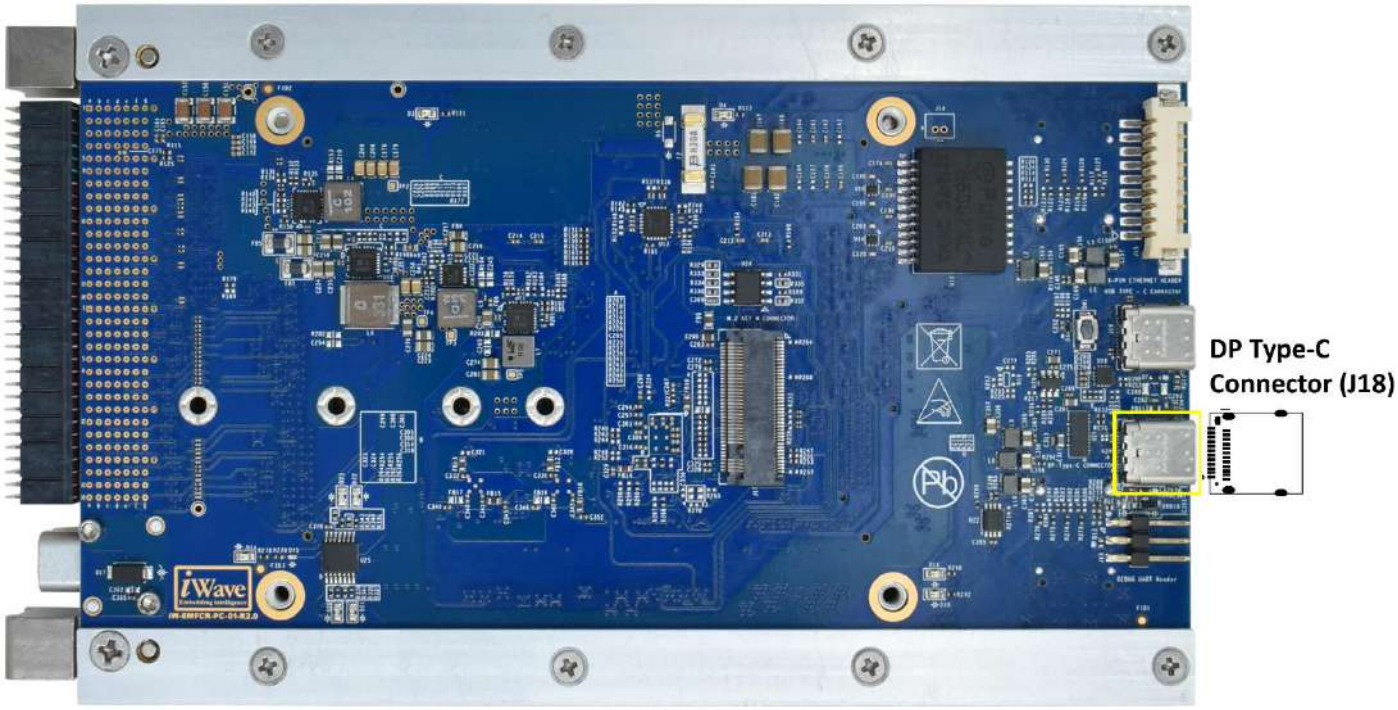

Figure 12: Display Port Type-C Connector

Table 4: USB Type-C Pin Assignment

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
A1	GND	GND	NA	NA	NA	Power	Ground.
A2	SSTXp1	NC	NA	NA	NA	NC	NC
A3	SSTXn1	NC	NA	NA	NA	NC	NC
A4	VBUS	VBUS_DP	NA	NA	NA	Power	3.3V Power Supply.
A5	CC1	PL_A3_LVDS94_L10N	IO_L10N_AD10N_94	94	A3	O, 3.3V CMOS	Hot Plug Detect.
A6	Dp1	NC	NA	NA	NA	NC	NC
A7	Dn1	NC	NA	NA	NA	NC	NC
A8	SBU1	PL_J18_LVDS68_L9P	IO_L9P_T1L_N4_AD12P_68	68	J18	IO, 1.8V LVDS	Auxiliary channel Positive.
A9	VBUS	VBUS_DP	NA	NA	NA	Power	3.3V Power Supply.

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
A10	SSRXn2	PS_MGTRTXN3_505	PS_MGTRTXN3_505	505	AB40	I, DIFF	Display Port Transmit Lane0 Negative.
A11	SSRXp2	PS_MGTRTXP3_505	PS_MGTRTXP3_505	505	AB39	I, DIFF	Display Port Transmit Lane0 Positive.
A12	GND	GND	NA	NA	NA	Power	Ground.
B1	GND	GND	NA	NA	NA	Power	Ground.
B2	SSTXp2	PS_MGTRTXP2_505	PS_MGTRTXP2_505	505	AD39	I, DIFF	Display Port Transmit Lane1 Positive.
B3	SSTXn2	PS_MGTRTXN2_505	PS_MGTRTXN2_505	505	AD40	I, DIFF	Display Port Transmit Lane1 Negative
B4	VBUS	VBUS_DP	NA	NA	NA	Power	3.3V Power Supply.
B5	CC2	NC	NA	NA	NA	NC	NC
B6	Dp2	NC	NA	NA	NA	NC	NC
B7	Dn2	NC	NA	NA	NA	NC	NC
B8	SBU2	PL_H18_LVDS68_L9N	IO_L9N_T1L_N5_AD12N_68	68	H18	IO, 1.8V LVDS	Auxiliary channel Negative.
B9	VBUS	VBUS_DP	NA	NA	NA	Power	3.3V Power Supply.
B10	SSRXn1	NC	NA	NA	NA	NC	NC
B11	SSRXp1	NC	NA	NA	NA	NC	NC
B12	GND	GND	NA	NA	NA	Power	Mechanical Pin.

2.6.3 9-Pin Ethernet Header

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports 10/100/1000Mbps Ethernet ports. This Ethernet port is supported through GEM0 interface of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) PS. Ethernet PHY output signals is directly connected to 9-Pin Ethernet Header (J15) through H5007NL transformer. This 9-pin Ethernet Header(J15) is physically located at the bottom of the board as shown below.

Figure 13: 9-Pin Ethernet Header

Table 5: 9-Pin Ethernet Header Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	ATXRXP	GPHY_ATXRXM	IO, DIFF	Gigabit Ethernet differential pair 1 negative.
2	ATXRXM	GPHY_ATXRXP	IO, DIFF	Gigabit Ethernet differential pair 1 positive.
3	BTXRXP	GPHY_BTXRXM	IO, DIFF	Gigabit Ethernet differential pair 2 negative.
4	BTXRXM	GPHY_BTXRXP	IO, DIFF	Gigabit Ethernet differential pair 2 positive.
5	CTXRXP	GPHY_CTXRXM	IO, DIFF	Gigabit Ethernet differential pair 3 negative.
6	CTXRXM	GPHY_CTXRXP	IO, DIFF	Gigabit Ethernet differential pair 3 positive.
7	DTXRXP	GPHY_DTXRXM	IO, DIFF	Gigabit Ethernet differential pair 3 negative.
8	DTXRXM	GPHY_DTXRXP	IO, DIFF	Gigabit Ethernet differential pair 3 positive.
9	GND	GND	Power	Ground.

2.6.4 3-Pin Debug UART Header

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports debug interface through UART0 interface of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) PS. This UART0 signals are connected connected to 3-Pin Header (J19). This Header can be used for Debug purpose which is is physically located at the bottom of the board as shown below.

Figure 14: 3-Pin Debug UART Header

Table 6: 3-Pin Debug UART Header Pin Assignment

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
1	TX	UART0_TX(PS_MIO07_500)	PS_MIO7_500	500	AL30	O, 1.8V LVCMOS	Transmit Data Line.
2	RX	UART0_RX(PS_MIO06_500)	PS_MIO6_500	500	AL31	I, 1.8V LVCMOS	Receive Data Line.
3	GND	GND	NA	NA	NA	Power	Ground.

2.7 Other On-Module Features

Other features which are supported from PS and PL of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module are explained in the following section.

2.7.1 M.2 PCIe Connector

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports one PCIe interface through M.2 (Key M) PCIe Connector. PS-GTR0 Lane of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) PS is used for PCIe interface. MPSoC's PCIe supports the Specification with Gen1(2.5Gbps) & Gen2(5Gbps) datarates. The VPX Card board provides 100MHz reference clock to M.2 connector from on board LVDS Clock Buffer1. On Board LVDS Clock Buffer1 input clock is fed from the clock synthesizer (OUT2). This M.2 PCIe connector (J17) is physically located at the bottom of the board as shown below.

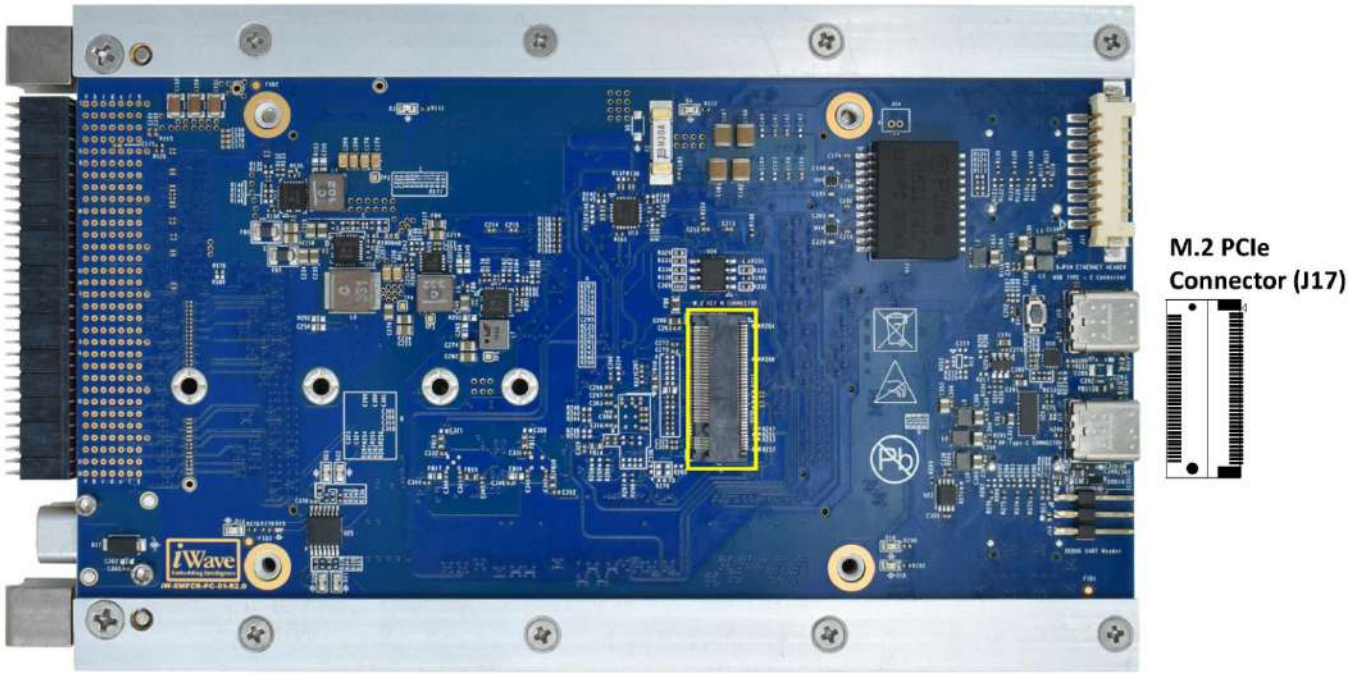

Figure 15: M.2 PCIe Connector (Key M)

Table 7: M.2 PCIe Connector Pin Assignment

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
1	CONFIG_3	NA	NA	NA	NA	NA	NC
2	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
3	GND	GND	NA	NA	NA	Power	Ground.
4	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
5	PERn3	NA	NA	NA	NA	NA	NC.

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
6	N/A1	NA	NA	NA	NA	NA	NC.
7	PERp3	NA	NA	NA	NA	NA	NC.
8	N/A2	NA	NA	NA	NA	NA	NC.
9	GND	GND	NA	NA	NA	Power	Ground.
10	DAS/DSS	DAS	NA	NA	NA	IO, 3.3V CMOS	Connected to LED D15 for the activity indication
11	PETn3	NA	NA	NA	NA	NA	NC.
12	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
13	PETp3	NA	NA	NA	NA	NA	NC.
14	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
15	GND	GND	NA	NA	NA	Power	Ground.
16	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
17	PERn2	NA	NA	NA	NA	NA	NC.
18	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
19	PERp2	NA	NA	NA	NA	NA	NC.
20	N/A3	NA	NA	NA	NA	NA	NC.
21	CONFIG_0	NA	NA	NA	NA	NA	NC
22	N/A4	NA	NA	NA	NA	NA	NC.
23	PETn2	NA	NA	NA	NA	NA	NC.
24	N/A5	NA	NA	NA	NA	NA	NC.
25	PETp2	NA	NA	NA	NA	NA	NC.
26	N/A6	NA	NA	NA	NA	NA	NC.
27	GND	GND	NA	NA	NA	Power	Ground.
28	N/A7	NA	NA	NA	NA	NA	NC.
29	PERn1	NA	NA	NA	NA	NA	NC.
30	N/A8	NA	NA	NA	NA	NA	NC.
31	PERp1	NA	NA	NA	NA	NA	NC.
32	N/A9	NA	NA	NA	NA	NA	NC.
33	GND	GND	NA	NA	NA	Power	Ground.
34	N/A10	NA	NA	NA	NA	NA	NC.
35	PETn1	NA	NA	NA	NA	NA	NC.
36	N/A11	NA	NA	NA	NA	NA	NC.
37	PETp1	NA	NA	NA	NA	NA	NC.
38	DEVSLP	NA	NA	NA	NA	NA	NC.
39	GND	GND	NA	NA	NA	Power	Ground.
40	SMB_CLK	NA	NA	NA	NA	NA	NC.

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
41	SATA-B+/PERn0	PS_MGTRRXN0_505	PS_MGTRRXN0_505	505	AG42	I, DIFF	PCIe Receive pair negative.
42	SMB_DATA	NA	NA	NA	NA	NA	NC.
43	SATA-B-/PERp0	PS_MGTRRXP0_505	PS_MGTRRXP0_505	505	AG41	I, DIFF	PCIe Receive pair positive.
44	SMB_ALERT	NA	NA	NA	NA	NA	NC.
45	GND	GND	NA	NA	NA	Power	Ground.
46	N/A15	NA	NA	NA	NA	NA	NC.
47	SATA-A-/PETn0	PS_MGTRTXN0_505	PS_MGTRTXN0_505	505	AH40	O, DIFF	PCIe Transmit pair negative.
48	N/A16	NA	NA	NA	NA	NA	NC.
49	SATA-A+/PETp0	PS_MGTRTXP0_505	PS_MGTRTXP0_505	505	AH39	O, DIFF	PCIe Transmit pair positive.
50	PERST#	PL_H9_LVDS93_L3N	IO_L3N_AD9N_93	93	H9	O, 3.3V CMOS 10K PU	PL Bank93 IO3 Single Ended. This pin is connected from H9 pin of PL HD Bank 93.
51	GND	GND	NA	NA	NA	Power	Ground.
52	CLKREQ#	PL_F9_LVDS93_L4P	IO_L4P_AD8P_93	93	F9	IO, 3.3V CMOS 10K PU	PL Bank93 IO4 Single Ended. This pin is connected from F9 pin of PL HD Bank 93.
53	REFCLKN	M2_PCIe_REFCLKN	NA	NA	NA	O, DIFF	PCIe reference clock pair negative. This pin is connected from 2nd (Q1b) pin of LVDS Clock Buffer1.
54	PEWAKE#	PL_E9_LVDS93_L4N	IO_L4N_AD8N_93	93	E9	O, 3.3V CMOS 10K PU	PL Bank93 IO4 Single Ended. This pin is connected from E9 pin of PL HD Bank 93
55	REFCLKP	M2_PCIe_REFCLKP	NA	NA	NA	O, DIFF	PCIe reference clock pair positive. This pin is connected from 3rd (Q1) pin of LVDS Clock Buffer1.

Pin No	Pin Name	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Signal Type / Termination	Description
56	MFG1	NA	NA	NA	NA	NA	NC.
57	GND	GND	NA	NA	NA	Power	Ground.
58	MFG2	NA	NA	NA	NA	NA	NC.
59	M1	NA	NA	NA	NA	NA	NC.
60	M2	NA	NA	NA	NA	NA	NC.
61	M3	NA	NA	NA	NA	NA	NC.
62	M4	NA	NA	NA	NA	NA	NC.
63	M5	NA	NA	NA	NA	NA	NC.
64	M6	NA	NA	NA	NA	NA	NC.
65	M7	NA	NA	NA	NA	NA	NC.
66	M8	NA	NA	NA	NA	NA	NC.
67	N/A17	NA	NA	NA	NA	NA	NC.
68	SUSCLK	NA	NA	NA	NA	NA	NC.
69	CONFIG_1	PL_C9_LVDS93_L12N	IO_L12N_AD0N_93	93	C9	O, CMOS 10K PU	PL HD Bank93 IO12 Single Ended. This pin is connected to VCC_3V3
70	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
71	GND	GND	NA	NA	NA	Power	Ground.
72	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
73	GND	GND	NA	NA	NA	Power	Ground.
74	3.3V	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
75	CONFIG_2	NA	NA	NA	NA	NA	NC

2.7.2 General Purpose LEDs

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports four configurable General Purpose LEDs (D20, D21, D22 & D23). This LEDs are connected to a Quadruple Bus Buffer Gate IC which is controlled by PL HD Bank IOs. The four User LEDs are physically located at the bottom of the board as shown below.

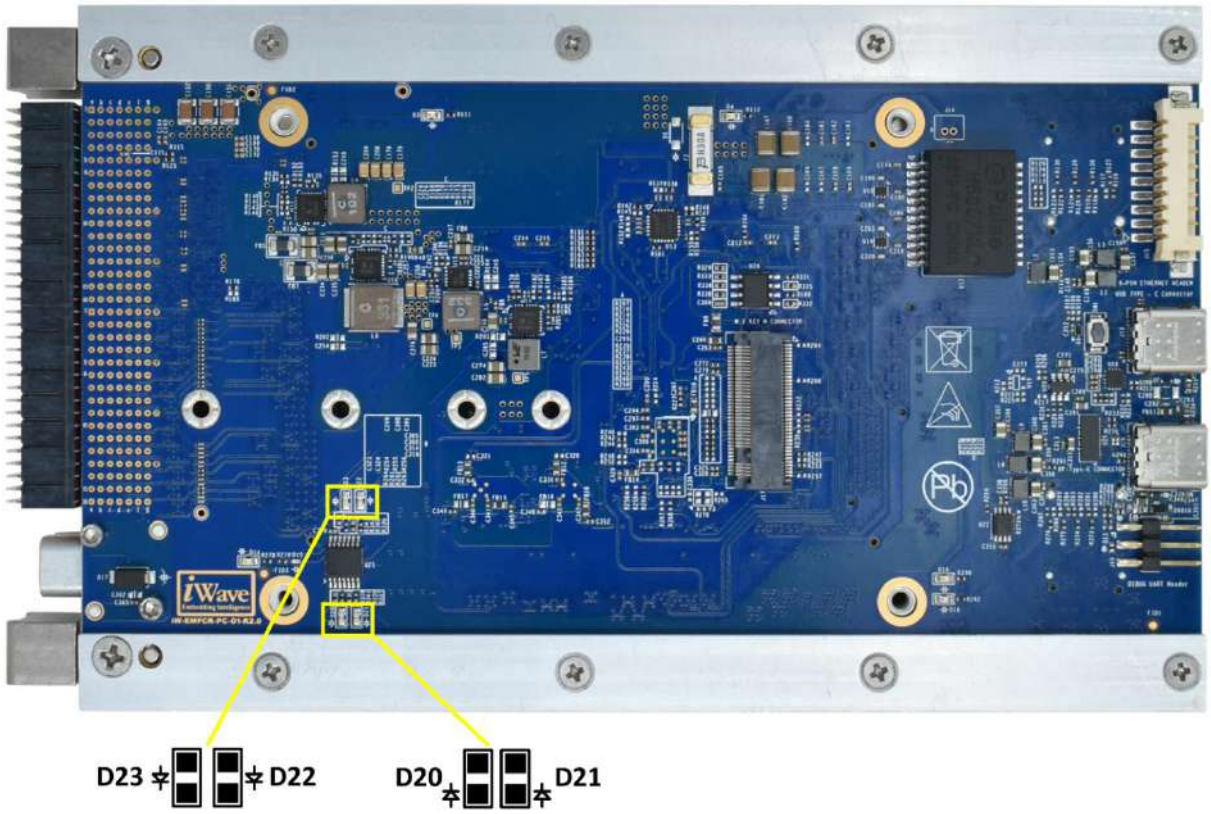

Figure 16: 2.8.3 General Purpose LEDs

Table 8: General Purpose LEDs Pin Assignment

B2B-1 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
82	PL_F8_LVDS93_L6N_HDGC	IO_L6N_HDGC_AD6N_93	PL HD Bank 93	F8	O, 3.3V	Connected to User LED – D20. By default, high.
84	PL_G8_LVDS93_L6P_HDGC	IO_L6P_HDGC_AD6P_93	PL HD Bank 93	G8	O, 3.3V	Connected to User LED – D21. By default, high.
92	PL_E1_LVDS94_L4P	IO_L4P_AD12P_94	PL HD Bank 94	E1	O, 3.3V	Connected to User LED – D22. By default, high.
94	PL_D1_LVDS94_L4N	IO_L4N_AD12N_94	PL HD Bank 94	D1	O, 3.3V	Connected to User LED – D23. By default, high.

2.7.3 Temperature Sensor

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports and external Temperature Sensor IC which is communicated using I2C Bus from PS of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) SOM. Temperature ALERT pin of the Temperature Sensor IC is connected to PL HD Bank94 IO.

2.7.4 Elapse Time Counter

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports an Elapse Time Counter Interface which can be utilized for specific timing and synchronization requirements. The EVENT input and ALARM output of the Elapsed Time Counter IC are connected to the PL IOs of HD Bank 93. Additionally, ETC IC supports 16 bytes of user-programmable EEPROM Memory.

2.7.5 Reset Switch

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports Push button switch (SW1) to reset the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) CPU. Reset signal is directly connected from Reset Push button switch to PS_SRST_B pin of Zynq Ultrascale+ MPSoC. This Reset Push button switch (SW1) is physically located at the bottom of the board as shown below.

Figure 17: Reset Switch

2.8 Clock Tree

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports On-Board Oscisllators for PS & PL reference clocks. Also it supports one 10-output Clock Synthesizer “SI5341B-D-GM” and three LVDS Clock Buffers “SI53342-B-GM” for PS-GTR, PL-GTH and PL-GTY Transceiver Banks Reference Clock distribution. This Clock Generator’s outputs are connected to MPSoC through 0.01uF AC coupling capacitors. An external 100MHz Oscillator is connected to this Clock Synthesizer for reference. This Clock Synthesizer supports from 100 Hz to 1028 MHz clock output and configurable through PS I2C0.

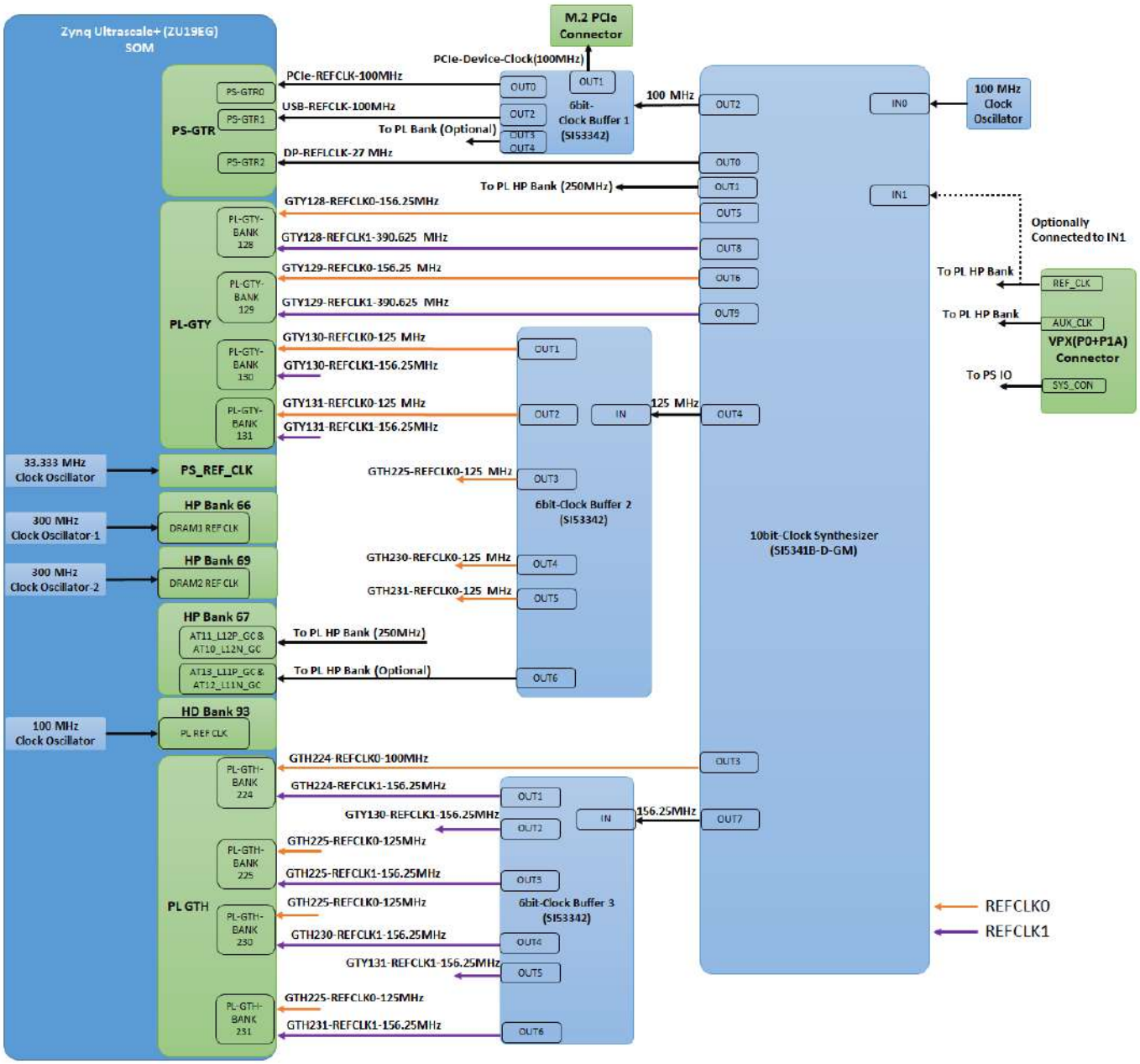

Figure 18: Clock Tree

Table 9: On -Board Oscillators

Sl. No	On-Board Oscillator Frequency	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	33.33MHz	PS_REF_CLK	503	AC27	1.8V, LVCMOS	33.33Mhz single ended reference clock for PS.
2	100MHz[1]	IO_L5P_HDGC_AD7P_93	93	G7	1.8V[2], LVCMOS	100Mhz single ended reference clock for PL. This is connected to PL Bank93 HDGC Global clock pin.
3	300MHz	IO_L13N_T2L_N1_GC_QBC_64	64	AT21	1.8V, LVDS	LVDS reference clock for PL DDR4 SDRAM1. This is connected to PL Bank64 Global clock pins.
		IO_L13P_T2L_N0_GC_QBC_64		AT22		
4	300MHz	IO_L13N_T2L_N1_GC_QBC_69	69	D32	1.8V, LVDS	LVDS reference clock for PL DDR4 SDRAM2. This is connected to PL Bank69 Global clock pins.
		IO_L13P_T2L_N0_GC_QBC_69		E32		

[1] Important Note: I/O voltage of PL Bank93 is software configurable. Since this oscillator supports 1.8V to 3.3V VCC only, this reference clock can be used only if the I/O voltage of PL Bank93 is set between 1.8V to 3.3V.

[2] Mentioned voltage level is based on after uboot bootup I/O voltage set to PL Bank93.

Table 10: Clock Synthesizer Output Clocks

Clock Synthesizer Pin No	Clock Synthesizer Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Programmed Frequency	Connected To
24	OUT0	PS_MGTREFCLK2P_505	505	AC37	27 MHz	PS GTR Lane3 Reference Clock
23	OUT0b	PS_MGTREFCLK2N_505		AC38		
28	OUT1	IO_L13P_T2L_N0_GC_QBC_67	67	AR13	250 MHz	PL HP Bank 67 Global Clock Differential Input
27	OUT1b	IO_L13N_T2L_N1_GC_QBC_67		AR12		
31	OUT2	NA	NA	NA	100 MHz	LVDS Clock Buffer – 1 Input (CLK0/CLK0B)
30	OUT2b	NA		NA		
35	OUT3	MGTREFCLK0P_224	224	AK12	100 MHz	PL GTH Bank 224 Transceiver Reference Clock 0
34	OUT3b	MGTREFCLK0N_224		AK11		
38	OUT4	NA	NA	NA	125 MHz	LVDS Clock Buffer – 2 Input (CLK0/CLK0B)
37	OUT4b	NA		NA		
42	OUT5	MGTREFCLK0P_128	128	AB34	156.25 MHz	PL GTY Bank 128 Transceiver Reference Clock 0
41	OUT5b	MGTREFCLK0N_128		AB35		
45	OUT6	MGTREFCLK0P_129	129	W32	156.25 MHz	PL GTY Bank 129 Transceiver Reference Clock 0
44	OUT6b	MGTREFCLK0N_129		W33		
51	OUT7	NA	NA	NA	156.25 MHz	LVDS Clock Buffer – 3 Input (CLK0/CLK0B)
50	OUT7b	NA		NA		
54	OUT8	MGTREFCLK1P_128	128	AA32	390.625 MHz	PL GTY Bank 128 Transceiver Reference Clock 1
53	OUT8b	MGTREFCLK1N_128		AA33		
59	OUT9	MGTREFCLK1P_129	129	U32	390.625 MHz	PL GTY Bank 129 Transceiver Reference Clock 1
58	OUT9b	MGTREFCLK1N_129		U33		

Table 11: LVDS Clock Buffer1 Output Clocks

Clock Buffer Pin No	Clock Buffer Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Programmed Frequency	Connected To
5	Q0	PS_MGTREFCLK0P_505	505	AG37	100 MHz	PS GTR Lane0 Reference Clock.
4	Q0B	PS_MGTREFCLK0N_505		AG38		
3	Q1	NA	NA	NA	100 MHz	M.2 PCIe Device Reference clock.
2	Q1B	NA		NA		
23	Q2	PS_MGTREFCLK1P_505	505	AE37	100 MHz	PS GTR Lane1 Reference Clock
22	Q2B	PS_MGTREFCLK1N_505		AE38		
21	Q3	IO_L12P_T1U_N10_GC_67	67	AT11	100 MHz	PL HP Bank 67 Global Clock Differential Input
20	Q3B	IO_L12N_T1U_N11_GC_67		AT10		
17	Q4	IO_L8P_HDGC_AD4P_93	93	D8	100 MHz	PL HD Bank 93 Global Clock Differential Input
16	Q4B	IO_L8N_HDGC_AD4N_93		C8		

Table 12: LVDS Clock Buffer2 Output Clocks

Clock Buffer Pin No	Clock Buffer Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Programmed Frequency	Connected To
5	Q0	MGTREFCLK0P_130	130	R32	125 MHz	PL GTY Bank 130 Transceiver Reference Clock 0
4	Q0B	MGTREFCLK0N_130		R33		
3	Q1	MGTREFCLK0P_131	131	L32	125 MHz	PL GTY Bank 131 Transceiver Reference Clock 0
2	Q1B	MGTREFCLK0N_131		L33		
23	Q2	MGTREFCLK0P_225	225	AH12	125 MHz	PL GTY Bank 225 Transceiver Reference Clock 0
22	Q2B	MGTREFCLK0N_225		AH11		
21	Q3	MGTREFCLK0P_230	230	V12	125 MHz	PL GTY Bank 230 Transceiver Reference Clock 0
20	Q3B	MGTREFCLK0N_230		V11		
17	Q4	MGTREFCLK0P_231	231	T12	125 MHz	PL GTY Bank 231 Transceiver Reference Clock 0
16	Q4B	MGTREFCLK0N_231		T11		
15	Q5	IO_L11P_T1U_N8_GC_67	67	AT13	125 MHz	PL HP Bank 67 Global Clock Differential Input
14	Q5B	IO_L11N_T1U_N9_GC_67		AT12		

Table 13: LVDS Clock Buffer3 Output Clocks

Clock Buffer Pin No	Clock Buffer Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No.	Programmed Frequency	Connected To
5	Q0	MGTREFCLK1P_224	224	AJ10	156.25 MHz	PL GTY Bank 224 Transceiver Reference Clock 1
4	Q0B	MGTREFCLK1N_224		AJ9		
3	Q1	MGTREFCLK1P_130	130	N32	156.25 MHz	PL GTY Bank 130 Transceiver Reference Clock 1
2	Q1B	MGTREFCLK1N_130		N33		
23	Q2	MGTREFCLK1P_225	225	AG10	156.25 MHz	PL GTY Bank 225 Transceiver Reference Clock 1
22	Q2B	MGTREFCLK1N_225		AG9		
21	Q3	MGTREFCLK1P_230	230	U10	156.25 MHz	PL GTY Bank 230 Transceiver Reference Clock 1
20	Q3B	MGTREFCLK1N_230		U9		
17	Q4	MGTREFCLK1P_131	131	J32	156.25 MHz	PL GTY Bank 131 Transceiver Reference Clock 1
16	Q4B	MGTREFCLK1N_131		J33		
15	Q5	MGTREFCLK1P_231	231	R10	156.25 MHz	PL GTY Bank 231 Transceiver Reference Clock 1
14	Q5B	MGTREFCLK1N_231		R9		

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module's Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The Zynq Ultrasclae+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module is designed to work with 12V & 3.3V external power through VPX Connector J5 (P0) and uses on board voltage regulators for internal power management.

The below table provides the Power Input Requirement Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

Table 14: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.4V	12V	12.6V	±50mV
2	VCC_3V3_AUX	3.25	3.3V	3.45V	±50mV
3	VBAT-P1[1]	0	3V	3.15V	±20mV

[1] The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module uses this voltage as backup power source to On-SOM PMIC RTC controller when VCC is off.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module.

Table 15: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	+85°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.2.2 RoHS Compliance

iWave's Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 3U-VPX Plug-in Module Mechanical Dimensions

The 3U-VPX Plug-in Module PCB form factor is 160mm x 100mm and Module mechanical dimension is shown below.

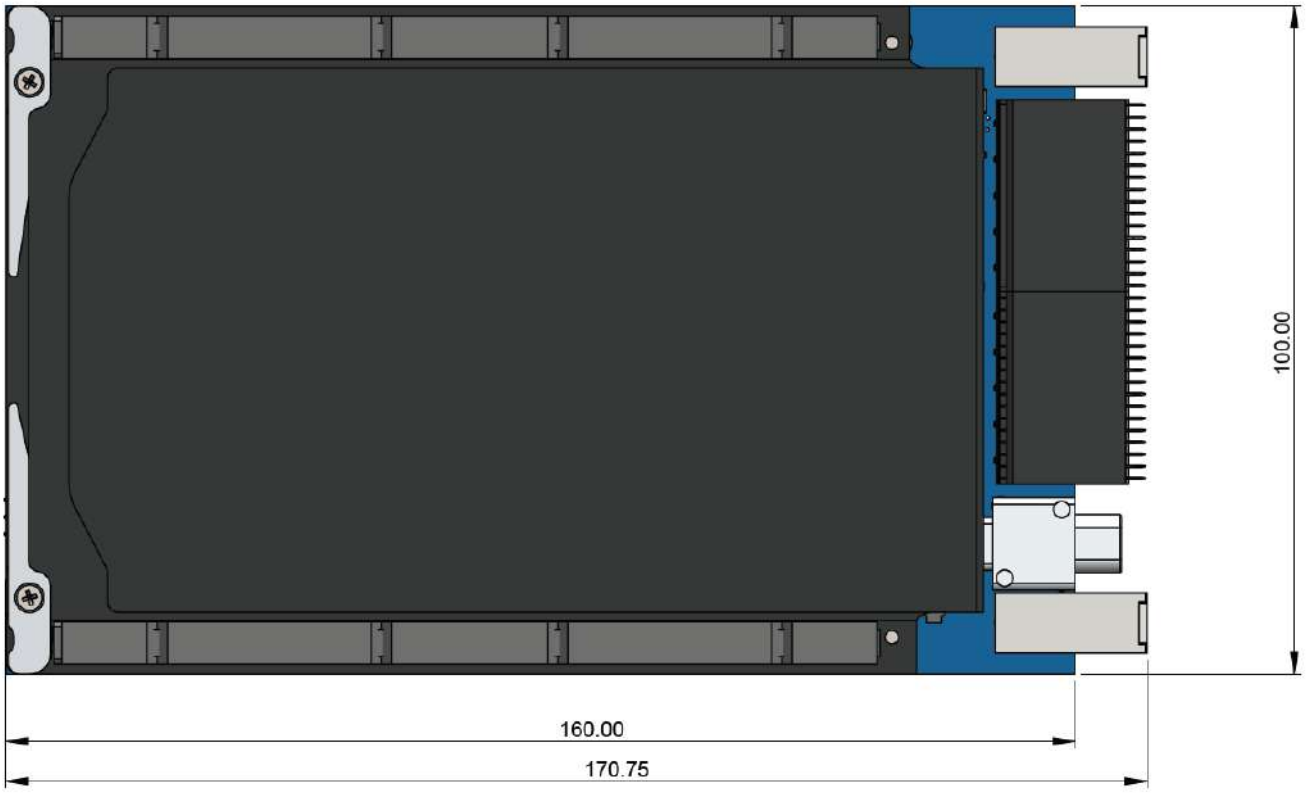

Figure 19: 3U-VPX Plug-in Module Mechanical dimension – Top View

The 3U-VPX Card board PCB thickness is 1.6mm±0.1mm, top side maximum height component is the Heat-Spreader (16.76mm) followed by MT Ferrule Connector (14.70mm) and bottom side maximum height component is 9-pin Ethernet Header (5.60mm) and 1000Base-T Magnetics Module (5.40mm) followed by M.2 PCIe connector(4.20mm). Please refer the below figure for height details of the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Card.

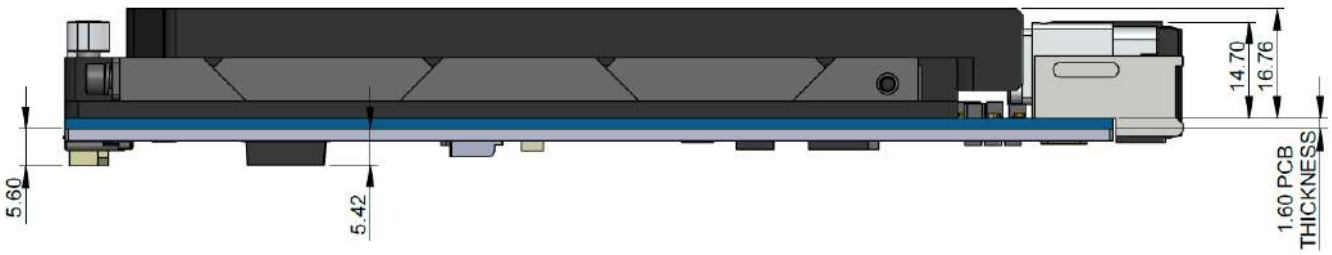

Figure 20: 3U-VPX Plug-in Module Mechanical dimension – Side View

Note: Height of the some of the parts in the bottom side is beyond the specification. Contact iWave to remove those features.

3.3.2 Alignment and Keying

Zynq Ultrascale+ MPSoC (ZU19/17/11EG) VPX Plug-in Module has an alignment keying of 315° with an on-board guide socket, which matches the backplane's alignment pin also set at 315°. For keying information of the Zynq Ultrascale+ MPSoC (ZU19/17/11EG) VPX Plug-in Module, please refer to the figure below.

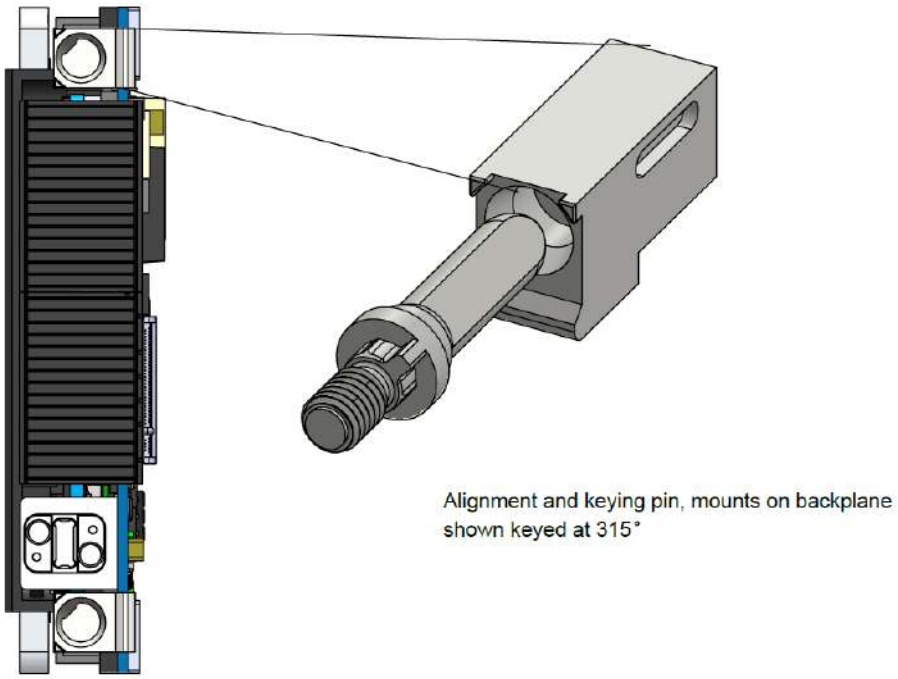

Figure 21: 3U-VPX Module Alignment Keying

3.3.3 Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module Expanded View

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) Plug-in Module's Expanded view is provided below.

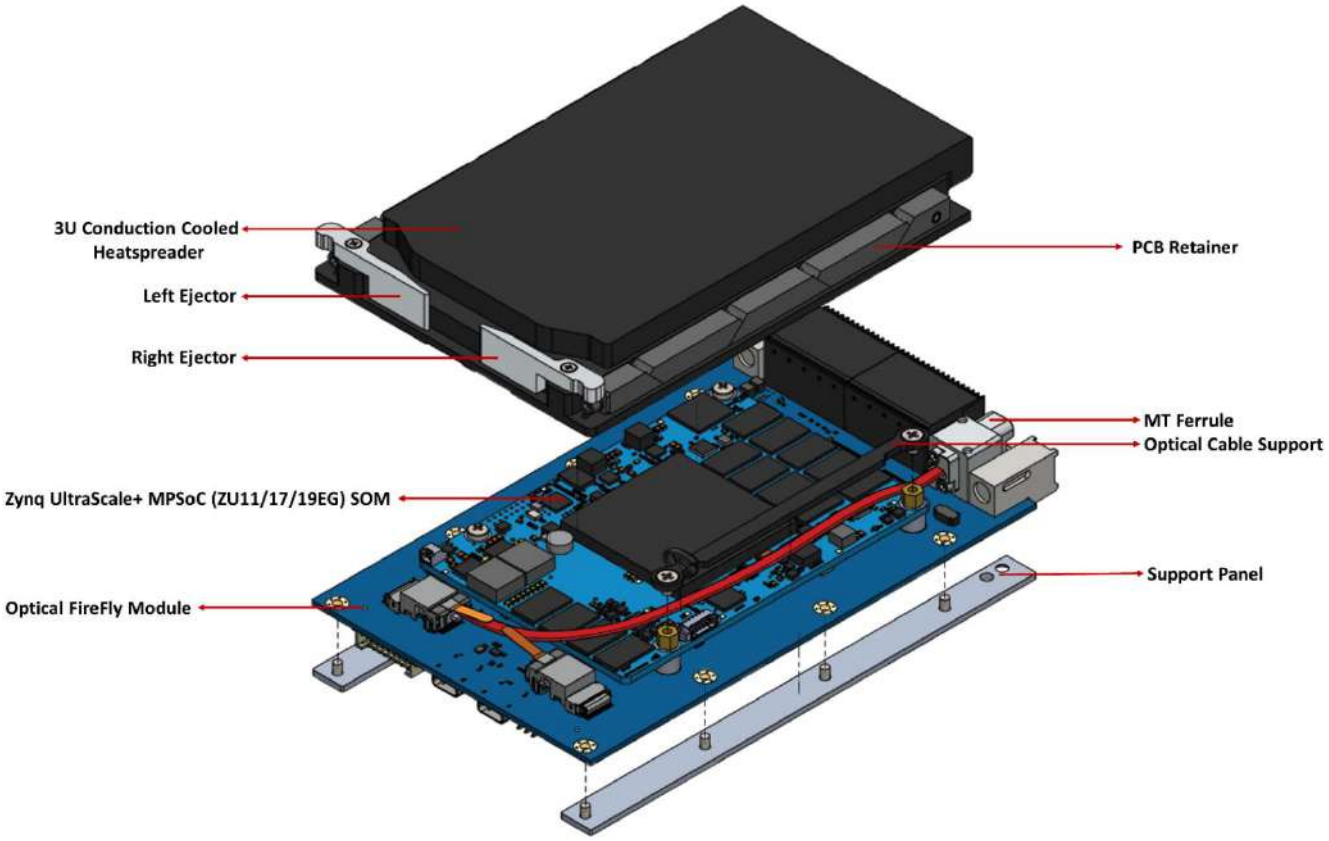

Figure 22: 3U-VPX Module Expanded View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 16: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G35V-19EG-4E004G-E008G-BIA	ZU19EG (-2) MPSoC (XCZU19EG-2FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4, 8GB eMMC, 3U VPX Backplane connectors, 3U VPX Heatspreader with Wedgelocks & Ejector and without MT Ferrule (no Optical)	Industrial
iW-G35V-19EG-4E004G-E008G-BIB	ZU19EG (-2) MPSoC (XCZU19EG-2FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4, 8GB EMMC, 3U VPX Backplane connectors, MT Ferrule with Single Firefly (8 Optical – 4 TX & 4 RX), 3U VPX Heatspreader with Wedgelocks & Ejector	Industrial

5. APPENDIX

5.1 Compatible VPX Slot Profiles

Below provided VPX Slot Profiles are compatible with iWave's Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U VPX Plug-in Module.

Table 17: Compatible Slot Profiles

SL No.	VPX Slot Profile
1	**SLT3-SWH-4F1U7U1J-14.8.7-n**
2	SLT3-SWH-4F8U1J-14.8.5-n
3	SLT3-PER-2F-14.3.1-n
4	SLT3-PER-1F-14.3.2-n
5	SLT3-SWH-2F8U-14.4.5-n
6	SLT3-SWH-4F-14.4.4-n
7	SLT3-SWH-10U7T1J-14.8.1-n
8	SLT3-SWH-10U7T1E-14.8.1-0
9	SLT3-SWH-6F1J-14.8.3-n
10	SLT3-SWH-6F1E-14.8.4-0
11	SLT3-PAY-1F1F2U1E-14.6.1-0
12	SLT3-PAY-4F1E-14.6.2-0
13	SLT3-PAY-2F1F2U1J-14.6.5-n
14	SLT3-PAY-2F1F2U1E-14.6.6-0
15	SLT3-PAY-2F2U1J-14.6.9-n
16	SLT3-PAY-2F2U1E-14.6.10-0

5.2 VPX Connector Pinout

Table 18: VPX Connector Pin Assignment(P0+P1A)

SL No	VPX Connector Pin No	VPX Connector Pin Name	SOM Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/Termination	Description
1	A1	No Pad1	NA	NA	NA	NA	NA	NC.
2	A2	No Pad2	NA	NA	NA	NA	NA	NC.
3	A3	No Pad3	NA	NA	NA	NA	NA	NC.
4	A4	NVMRO	PS_MIO45_501	PS_MIO45_501	501	T29	O, 3V3 LVCMOS	Non-Volatile Memory Read Only. This signal is connected to VPX Connector through Level translator (U2).
5	A5	IPMB_A_SDA	I2C0_SDA(PS_MIO11_500)	PS_MIO11_500	500	AK32	IO, 3V3 LVCMOS	I2C0 Data. This signal is connected to VPX Connector through Level translator (U3).
6	A6	GA0	PS_MIO51_501	PS_MIO51_501	501	W30	I, 3V3 LVCMOS/10K PU	Geographical Address 0. This signal is connected to VPX Connector through Level translator (U4).
7	A7	TRST	NA	NA	NA	NA	NA	Optional support provided at Board-to-Board Connector
8	A8	DGND1	GND	NA	NA	NA	Power	Ground.
9	A9	DS01-RD0+	GTHRXP0_224	MGTHRXP0_224	224	BA2	I, DIFF	GTH Bank224 channel0 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap.
10	A10	DGND2	GND	NA	NA	NA	Power	Ground.
11	A11	DS01-RD2+	GTHRXP2_224	MGTHRXP2_224	224	AV4	I, DIFF	GTH Bank224 channel2 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
12	A12	DGND3	GND	NA	NA	NA	Power	Ground.
13	A13	DP01-RD0+	GTHRXP0_225	MGTHRXP0_225	225	AT4	I, DIFF	GTH Bank225 channel0 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap.
14	A14	DGND4	GND	NA	NA	NA	Power	Ground.
15	A15	DP01-RD2+	GTHRXP2_225	MGTHRXP2_225	225	AP4	I, DIFF	GTH Bank225 channel2 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
16	A16	DGND5	GND	NA	NA	NA	Power	Ground.
17	B1	No Pad1	NA	NA	NA	NA	NA	NC.
18	B2	No Pad2	NA	NA	NA	NA	NA	NC.
19	B3	No Pad3	NA	NA	NA	NA	NA	NC.
20	B4	SYSRESET_F	PS_MIO5_500	PS_MIO5_500	500	AL32	I, 3V3 LVCMOS	System Reset. This signal is connected to VPX Connector through Level translator (U2).
21	B5	IPMB_A_SCL	I2C0_SCL(PS_MIO10_500)	PS_MIO10_500	500	AK30	O, 3V3 LVCMOS	I2C0 Clock. This signal is connected to VPX Connector through Level translator (U3).
22	B6	GA1	PS_MIO50_501	PS_MIO50_501	501	V29	I, 3V3 LVCMOS/10K PU	Geographical Address 1. This signal is connected to VPX Connector through Level translator (U4).

SL No	VPX Connector Pin No	VPX Connector Pin Name	SOM Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/Termination	Description
23	**B7**	TMS	PS_JTAG_TMS	PS_JTAG_TMS	503	AD26	I, 3V3 LVCMOS	JTAG test mode select. This signal is connected to VPX Connector through Level translator(U1).
24	**B8**	AUX_CLK+	PL_F14_LVDS68_L13P_GC	IO_L13P_T2L_N0_GC_QBC_68	68	F14	I, 1.8V LVDS	PL Bank68 IO13 differential Global Clock positive. This signal is connected to Board-to-Board connector through 0.1uF AC Cap
25	**B9**	DS01-RD0-	GTHRXN0_224	MGTHRXN0_224	224	BA1	I, DIFF	GTH Bank224 channel0 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
26	**B10**	DS01-RD1+	GTHRXP1_224	MGTHRXP1_224	224	AW2	I, DIFF	GTH Bank224 channel1 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
27	**B11**	DS01-RD2-	GTHRXN2_224	MGTHRXN2_224	224	AV3	I, DIFF	GTH Bank224 channel2 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
28	**B12**	DS01-RD3+	GTHRXP3_224	MGTHRXP3_224	224	AU2	I, DIFF	GTH Bank224 channel3 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
29	**B13**	DP01-RD0-	GTHRXN0_225	MGTHRXN0_225	225	AT3	I, DIFF	GTH Bank225 channel0 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
30	**B14**	DP01-RD1+	GTHRXP1_225	MGTHRXP1_225	225	AR2	I, DIFF	GTH Bank225 channel1 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
31	**B15**	DP01-RD2-	GTHRXN2_225	MGTHRXN2_225	225	AP3	I, DIFF	GTH Bank225 channel2 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
32	**B16**	DP01-RD3+	GTHRXP3_225	MGTHRXP3_225	225	AN2	I, DIFF	GTH Bank225 channel3 High speed differential receiver positive. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
33	**C1**	No Pad1	NA	NA	NA	NA	NA	NC.
34	**C2**	No Pad2	NA	NA	NA	NA	NA	NC.
35	**C3**	No Pad3	NA	NA	NA	NA	NA	NC.
36	**C4**	DGND1	GND	NA	NA	NA	Power	Ground.
37	**C5**	DGND2	GND	NA	NA	NA	Power	Ground.
38	**C6**	DGND3	GND	NA	NA	NA	Power	Ground.
39	**C7**	DGND4	GND	NA	NA	NA	Power	Ground.
40	**C8**	AUX_CLK-	PL_E14_LVDS68_L13N_GC	IO_L13N_T2L_N1_GC_QBC_68	68	E14	I, 1.8V LVDS	PL Bank68 IO13 differential Global Clock negative. This signal is connected to Board-to-Board connector through 0.1uF AC Cap
41	**C9**	DGND5	GND	NA	NA	NA	Power	Ground.
42	**C10**	DS01-RD1-	GTHRXN1_224	MGTHRXN1_224	224	AW1	I, DIFF	GTH Bank224 channel1 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap

SL No	VPX Connector Pin No	VPX Connector Pin Name	SOM Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/Termination	Description
43	**C11**	DGND6	GND	NA	NA	NA	Power	Ground.
44	**C12**	DS01-RD3-	GTHRXN3_224	MGTHRXN3_224	224	AU1	I, DIFF	GTH Bank224 channel3 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
45	**C13**	DGND7	GND	NA	NA	NA	Power	Ground.
46	**C14**	DP01-RD1-	GTHRXN1_225	MGTHRXN1_225	225	AR1	I, DIFF	GTH Bank225 channel1 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
47	**C15**	DGND8	GND	NA	NA	NA	Power	Ground.
48	**C16**	DP01-RD3-	GTHRXN3_225	MGTHRXN3_225	225	AN1	I, DIFF	GTH Bank225 channel3 High speed differential receiver negative. This signal is connected to Board-to-Board connector through 0.01uF AC Cap
49	**D1**	No Pad1	NA	NA	NA	NA	NA	NC.
50	**D2**	No Pad2	NA	NA	NA	NA	NA	NC.
51	**D3**	No Pad3	NA	NA	NA	NA	NA	NC.
52	**D4**	No Pad4	NA	NA	NA	NA	NA	NC.
53	**D5**	+3.3V_AUX	VCC_3V3_AUX	NA	NA	NA	I, 3.3V Power	Module Supply Voltage.
54	**D6**	No Pad5	NA	NA	NA	NA	NA	NC.
55	**D7**	TDI	PS_JTAG_TDI	PS_JTAG_TDI	503	AD25	I, 3V3 LVCMOS	JTAG test data input. This signal is connected to VPX Connector through Level translator(U1).
56	**D8**	DGND1	GND	NA	NA	NA	Power	Ground.
57	**D9**	DS01-TD0+	GTHTXP0_224	MGTHTXP0_224	224	AY4	O, DIFF	GTH Bank224 channel0 High speed differential transmitter positive.
58	**D10**	DGND2	GND	NA	NA	NA	Power	Ground.
59	**D11**	DS01-TD2+	GTHTXP2_224	MGTHTXP2_224	224	AU6	O, DIFF	GTH Bank224 channel2 High speed differential transmitter positive.
60	**D12**	DGND3	GND	NA	NA	NA	Power	Ground.
61	**D13**	DP01-TD0+	GTHTXP0_225	MGTHTXP0_225	225	AR6	O, DIFF	GTH Bank225 channel0 High speed differential transmitter positive
62	**D14**	DGND4	GND	NA	NA	NA	Power	Ground.
63	**D15**	DP01-TD2+	GTHTXP2_225	MGTHTXP2_225	225	AN6	O, DIFF	GTH Bank225 channel2 High speed differential transmitter positive.
64	**D16**	DGND5	GND	NA	NA	NA	Power	Ground.
65	**E1**	+12VDC1	VDC_12V	NA	NA	NA	I, 12V Power	Module Board Main Input Supply Voltage.
66	**E2**	+12VDC2	VDC_12V	NA	NA	NA	I, 12V Power	Module Board Main Input Supply Voltage.
67	**E3**	No Pad	NA	NA	NA	NA	NA	NC.
68	**E4**	DGND1	GND	NA	NA	NA	Power	Ground.
69	**E5**	DGND2	GND	NA	NA	NA	Power	Ground.
70	**E6**	DGND3	GND	NA	NA	NA	Power	Ground.

SL No	VPX Connector Pin No	VPX Connector Pin Name	SOM Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/Termination	Description
71	**E7**	TDO	PS_JTAG_TDO	PS_JTAG_TDO	503	AD27	O, 3V3 LVCMOS	JTAG test data output. This signal is connected to VPX Connector through Level translator(U1).
72	**E8**	REF_CLK+	PL_G17_LVDS68_L11P_GC	IO_L11P_T1U_N8_GC_68	68	G17	I, 1.8V LVDS	PL Bank68 IO11 differential Global Clock positive. This signal is connected to Board-to-Board connector through 0.1uF AC Cap
73	**E9**	DS01-TD0-	GTHTXN0_224	MGTHTXN0_224	224	AY3	O, DIFF	GTH Bank224 channel0 High speed differential transmitter negative.
74	**E10**	DS01-TD1+	GTHTXP1_224	MGTHTXP1_224	224	AW6	O, DIFF	GTH Bank224 channel1 High speed differential transmitter positive.
75	**E11**	DS01-TD2-	GTHTXN2_224	MGTHTXN2_224	224	AU5	O, DIFF	GTH Bank224 channel2 High speed differential transmitter negative.
76	**E12**	DS01-TD3+	GTHTXP3_224	MGTHTXP3_224	224	AT8	O, DIFF	GTH Bank224 channel3 High speed differential transmitter positive.
77	**E13**	DP01-TD0-	GTHTXN0_225	MGTHTXN0_225	225	AR5	O, DIFF	GTH Bank225 channel0 High speed differential transmitter negative.
78	**E14**	DP01-TD1+	GTHTXP1_225	MGTHTXP1_225	225	AP8	O, DIFF	GTH Bank225 channel1 High speed differential transmitter positive.
79	**E15**	DP01-TD2-	GTHTXN2_225	MGTHTXN2_225	225	AN5	O, DIFF	GTH Bank225 channel2 High speed differential transmitter negative.
80	**E16**	DP01-TD3+	GTHTXP3_225	MGTHTXP3_225	225	AM8	O, DIFF	GTH Bank225 channel3 High speed differential transmitter positive
81	**F1**	+12VDC1	VDC_12V	NA	NA	NA	I, 12V Power	VPX Module Main Input Supply Voltage.
82	**F2**	+12VDC2	VDC_12V	NA	NA	NA	I, 12V Power	VPX Module Board Main Input Supply Voltage.
83	**F3**	No Pad	NA	NA	NA	NA	NA	NC.
84	**F4**	IPMB_B_SDA	PL_A13_LVDS68_L17N	IO_L17N_T2U_N9_AD10N_68	68	A13	IO, 3.3V LCVMOS	PL Bank68 IO17 Single Ended. This signal is connected to VPX Connector through Level translator(U3).
85	**F5**	GA4	PS_MIO48_501	PS_MIO48_501	501	V30	I, 3V3 LVCMOS/10K PU	Geographical Address 4. This signal is connected to VPX Connector through Level translator (U4).
86	**F6**	GA2	PS_MIO46_501	PS_MIO46_501	501	U28	I, 3V3 LVCMOS/10K PU	Geographical Address 2. This signal is connected to VPX Connector through Level translator (U4).
87	**F7**	DGND1	GND	NA	NA	NA	Power	Ground.
88	**F8**	REF_CLK-	PL_F17_LVDS68_L11N_GC	IO_L11N_T1U_N9_GC_68	68	F17	I, 1.8V LVDS	PL Bank68 IO11 differential Global Clock negative. This signal is connected to Board-to-Board connector through 0.1uF AC Cap
89	**F9**	DGND2	GND	NA	NA	NA	Power	Ground.
90	**F10**	DS01-TD1-	GTHTXN1_224	MGTHTXN1_224	224	AW5	O, DIFF	GTH Bank224 channel1 High speed differential transmitter negative.
91	**F11**	DGND3	GND	NA	NA	NA	Power	Ground.
92	**F12**	DS01-TD3-	GTHTXN3_224	MGTHTXN3_224	224	AT7	O, DIFF	GTH Bank224 channel3 High speed differential transmitter negative.
93	**F13**	DGND4	GND	NA	NA	NA	Power	Ground.

SL No	VPX Connector Pin No	VPX Connector Pin Name	SOM Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/Termination	Description
94	**F14**	DP01-TD1-	GTHTXN1_225	MGTHTXN1_225	225	AP7	O, DIFF	GTH Bank225 channel1 High speed differential transmitter negative.
95	**F15**	DGND5	GND	NA	NA	NA	Power	Ground.
96	**F16**	DP01-TD3-	GTHTXN3_225	MGTHTXN3_225	225	AM7	O, DIFF	GTH Bank225 channel3 High speed differential transmitter negative.
97	**G1**	+12VDC1	VDC_12V	NA	NA	NA	I, 12V Power	VPX Module Board Main Input Supply Voltage.
98	**G2**	+12VDC2	VDC_12V	NA	NA	NA	I, 12V Power	VPX Module Main Input Supply Voltage.
99	**G3**	No Pad	NA	NA	NA	NA	NA	NC.
100	**G4**	IPMB_B_SCL	PL_A14_LVDS68_L17P	IO_L17P_T2U_N8_AD10P_68	68	A14	O, 3.3V LCVMOS	PL Bank68 IO17 Single Ended. This signal is connected to VPX Connector through Level translator(U3).
101	**G5**	GAP	PS_MIO49_501	PS_MIO49_501	501	U29	I, 3V3 LVCMOS/10K PU	Geographical Address Parity. This signal is connected to VPX Connector through Level translator (U4).
102	**G6**	GA3	PS_MIO47_501	PS_MIO47_501	501	T28	I, 3V3 LVCMOS/10K PU	Geographical Address 3. This signal is connected to VPX Connector through Level translator (U4).
103	**G7**	TCK	PS_JTAG_TCK	PS_JTAG_TCK	503	AC26	I, 3V3 LVCMOS	JTAG test Clock. This signal is connected to VPX Connector through Level translator(U1).
104	**G8**	DGND1	GND	NA	NA	NA	Power	Ground.
105	**G9**	GDiscrete1	PS_MIO43_501	PS_MIO43_501	501	R30	IO, 3V3 LVCMOS/	General Purpose Input/Output. This signal is connected to VPX Connector through Level translator (U2).
106	**G10**	DGND2	GND	NA	NA	NA	Power	Ground.
107	**G11**	P1-VBAT	VBAT-P1	NA	NA	NA	Power	3V backup coin cell input for RTC.
108	**G12**	DGND3	GND	NA	NA	NA	Power	Ground.
109	**G13**	SYS_CON	PS_MIO3_500	PS_MIO3_500	500	AM30	IO, 3V3 LVCMOS/	System Controller. This signal is connected to VPX Connector through Level translator (U3).
110	**G14**	DGND4	GND	NA	NA	NA	Power	Ground.
111	**G15**	Reserved	NA	NA	NA	NA	NA	NC.
112	**G16**	DGND5	GND	NA	NA	NA	Power	Ground.

Table 19: VPX Connector Pin Assignment(P1B+P2A)

SL No	VPX Connector Pin No	VPX Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	**A1**	DP02-RD0+	Board to Board connector4	B17	GTHRXP0_230	230	T4	I, DIFF	GTH Bank230 channel0 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
2	**A2**	DGND1	NA	NA	GND	NA	NA	Power	Ground.
3	**A3**	DP02-RD2+	Board to Board connector4	B9	GTHRXP2_230	230	P4	I, DIFF	GTH Bank230 channel2 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
4	**A4**	DGND2	NA	NA	GND	NA	NA	Power	Ground.
5	**A5**	DP03-RD0+	Board to Board connector3	D51	GTHRXP0_231	231	M4	I, DIFF	GTH Bank231 channel0 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
6	**A6**	DGND3	NA	NA	GND	NA	NA	Power	Ground.
7	**A7**	DP03-RD2+	Board to Board connector3	C45	GTHRXP2_231	231	J2	I, DIFF	GTH Bank231 channel2 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
8	**A8**	DGND4	NA	NA	GND	NA	NA	Power	Ground.
9	**A9**	DGND5	NA	NA	GND	NA	NA	Power	Ground.
10	**A10**	DGND6	NA	NA	GND	NA	NA	Power	Ground.
11	**A11**	CPutp05-RD+	Board to Board connector3	A9	GTYRXP1_131	131	F39	I, DIFF	GTY Bank131 channel1 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
12	**A12**	DGND7	NA	NA	GND	NA	NA	Power	Ground.
13	**A13**	CPutp03-RD+	Board to Board connector3	C4	GTYRXP2_130	130	J41	I, DIFF	GTY Bank130 channel2 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
14	**A14**	DGND8	NA	NA	GND	NA	NA	Power	Ground.
15	**A15**	CPutp01-RD+	Board to Board connector3	C9	GTYRXP0_130	130	L41	I, DIFF	GTY Bank130 channel0 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.

SL No	VPX Connector Pin No	VPX Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
16	**A16**	DGND9	NA	NA	GND	NA	NA	Power	Ground.
17	**B1**	DP02-RD0-	Board to Board connector4	B16	GTHRXN0_230	230	T3	I, DIFF	GTH Bank230 channel0 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
18	**B2**	DP02-RD1+	Board to Board connector4	A3	GTHRXP1_230	230	R2	I, DIFF	GTH Bank230 channel1 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
19	**B3**	DP02-RD2-	Board to Board connector4	B8	GTHRXN2_230	230	P3	I, DIFF	GTH Bank230 channel2 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
20	**B4**	DP02-RD3+	Board to Board connector4	B5	GTHRXP3_230	230	N2	I, DIFF	GTH Bank230 channel3 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
21	**B5**	DP03-RD0-	Board to Board connector3	D50	GTHRXN0_231	231	M3	I, DIFF	GTH Bank231 channel0 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
22	**B6**	DP03-RD1+	Board to Board connector3	D43	GTHRXP1_231	231	L2	I, DIFF	GTH Bank231 channel1 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
23	**B7**	DP03-RD2-	Board to Board connector3	C44	GTHRXN2_231	231	J1	I, DIFF	GTH Bank231 channel2 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
24	**B8**	DP03-RD3+	Board to Board connector3	D47	GTHRXP3_231	231	G2	I, DIFF	GTH Bank231 channel3 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
25	**B9**	DGND	NA	NA	GND	NA	NA	Power	Ground.
26	**B10**	CPutp06-RD+	Board to Board connector3	B3	GTYRXP2_131	131	E41	I, DIFF	GTY Bank131 channel2 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.

SL No	VPX Connector Pin No	VPX Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
27	**B11**	CPutp05-RD-	Board to Board connector3	A8	GTYRXN1_131	131	F40	I, DIFF	GTY Bank131 channel1 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
28	**B12**	CPutp04-RD+	Board to Board connector3	A5	GTYRXP0_131	131	G41	I, DIFF	GTY Bank131 channel0 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
29	**B13**	CPutp03-RD-	Board to Board connector3	C5	GTYRXN2_130	130	J42	I, DIFF	GTY Bank130 channel2 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
30	**B14**	CPutp02-RD+	Board to Board connector3	C29	GTYRXP1_130	130	K39	I, DIFF	GTY Bank130 channel1 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
31	**B15**	CPutp01-RD-	Board to Board connector3	C8	GTYRXN0_130	130	L42	I, DIFF	GTY Bank130 channel0 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
32	**B16**	CSutp01-RD+	Board to Board connector3	B7	GTYRXP3_131	131	D39	I, DIFF	GTY Bank131 channel3 High speed differential receiver positive. This signal is connected to Board to Board connector through 0.01uF AC Cap.
33	**C1**	DGND	NA	NA	GND	NA	NA	Power	Ground.
34	**C2**	DP02-RD1-	Board to Board connector4	A2	GTHRXN1_230	230	R1	I, DIFF	GTH Bank230 channel1 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
35	**C3**	DGND	NA	NA	GND	NA	NA	Power	Ground.
36	**C4**	DP02-RD3-	Board to Board connector4	B4	GTHRXN3_230	230	N1	I, DIFF	GTH Bank230 channel3 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
37	**C5**	DGND	NA	NA	GND	NA	NA	Power	Ground.
38	**C6**	DP03-RD1-	Board to Board connector3	D42	GTHRXN1_231	231	L1	I, DIFF	GTH Bank231 channel1 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.

SL No	VPX Connector Pin No	VPX Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
39	**C7**	DGND	NA	NA	GND	NA	NA	Power	Ground.
40	**C8**	DP03-RD3-	Board to Board connector3	D46	GTHRXN3_231	231	G1	I, DIFF	GTH Bank231 channel3 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
41	**C9**	DGND	NA	NA	GND	NA	NA	Power	Ground.
42	**C10**	CPutp06-RD-	Board to Board connector3	B2	GTYRXN2_131	131	E42	I, DIFF	GTY Bank131 channel2 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
43	**C11**	DGND	NA	NA	GND	NA	NA	Power	Ground.
44	**C12**	CPutp04-RD-	Board to Board connector3	A4	GTYRXN0_131	131	G42	I, DIFF	GTY Bank131 channel0 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
45	**C13**	DGND	NA	NA	GND	NA	NA	Power	Ground.
46	**C14**	CPutp02-RD-	Board to Board connector3	C28	GTYRXN1_130	130	K40	I, DIFF	GTY Bank130 channel1 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
47	**C15**	DGND	NA	NA	GND	NA	NA	Power	Ground.
48	**C16**	CSutp01-RD-	Board to Board connector3	B6	GTYRXN3_131	131	D40	I, DIFF	GTY Bank131 channel3 High speed differential receiver negative. This signal is connected to Board to Board connector through 0.01uF AC Cap.
49	**D1**	DP02-TD0+	Board to Board connector4	A10	GTHTXP0_230	230	R6	O, DIFF	GTH Bank230 channel0 High speed differential transmitter positive.
50	**D2**	DGND	NA	NA	GND	NA	NA	Power	Ground.
51	**D3**	DP02-TD2+	Board to Board connector4	A18	GTHTXP2_230	230	N6	O, DIFF	GTH Bank230 channel2 High speed differential transmitter positive.
52	**D4**	DGND	NA	NA	GND	NA	NA	Power	Ground.
53	**D5**	DP03-TD0+	Board to Board connector3	C52	GTHTXP0_231	231	L6	O, DIFF	GTH Bank231 channel0 High speed differential transmitter positive.
54	**D6**	DGND	NA	NA	GND	NA	NA	Power	Ground.
55	**D7**	DP03-TD2+	Board to Board connector3	D54	GTHTXP2_231	231	J6	O, DIFF	GTH Bank231 channel2 High speed differential transmitter positive.
56	**D8**	DGND	NA	NA	GND	NA	NA	Power	Ground.
57	**D9**	DGND	NA	NA	GND	NA	NA	Power	Ground.
58	**D10**	DGND	NA	NA	GND	NA	NA	Power	Ground.

SL No	VPX Connector Pin No	VPX Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
59	**D11**	CPutp05-TD+	Board to Board connector3	B11	GTYTXP1_131	131	G36	O, DIFF	GTY Bank131 channel1 High speed differential transmitter positive.
60	**D12**	DGND	NA	NA	GND	NA	NA	Power	Ground.
61	**D13**	CPutp03-TD+	Board to Board connector3	C37	GTYTXP2_130	130	K34	O, DIFF	GTY Bank130 channel2 High speed differential transmitter positive.
62	**D14**	DGND	NA	NA	GND	NA	NA	Power	Ground.
63	**D15**	CPutp01-TD+	Board to Board connector3	C41	GTYTXP0_130	130	M34	O, DIFF	GTY Bank130 channel0 High speed differential transmitter positive.
64	**D16**	DGND	NA	NA	GND	NA	NA	Power	Ground.
65	**E1**	DP02-TD0-	Board to Board connector4	A11	GTHTXN0_230	230	R5	O, DIFF	GTH Bank230 channel0 High speed differential transmitter negative.
66	**E2**	DP02-TD1+	Board to Board connector4	A14	GTHTXP1_230	230	P8	O, DIFF	GTH Bank230 channel1 High speed differential transmitter positive.
67	**E3**	DP02-TD2-	Board to Board connector4	A19	GTHTXN2_230	230	N5	O, DIFF	GTH Bank230 channel2 High speed differential transmitter negative.
68	**E4**	DP02-TD3+	Board to Board connector4	B12	GTHTXP3_230	230	M8	O, DIFF	GTH Bank230 channel3 High speed differential transmitter positive.
69	**E5**	DP03-TD0-	Board to Board connector3	C53	GTHTXN0_231	231	L5	O, DIFF	GTH Bank231 channel0 High speed differential transmitter negative.
70	**E6**	DP03-TD1+	Board to Board connector3	C57	GTHTXP1_231	231	K4	O, DIFF	GTH Bank231 channel1 High speed differential transmitter positive.
71	**E7**	DP03-TD2-	Board to Board connector3	D55	GTHTXN2_231	231	J5	O, DIFF	GTH Bank231 channel2 High speed differential transmitter negative.
72	**E8**	DP03-TD3+	Board to Board connector3	D58	GTHTXP3_231	231	H4	O, DIFF	GTH Bank231 channel3 High speed differential transmitter positive.
73	**E9**	DGND	NA	NA	GND	NA	NA	Power	Ground.
74	**E10**	CPutp06-TD+	Board to Board connector3	A17	GTYTXP2_131	131	F34	O, DIFF	GTY Bank131 channel2 High speed differential transmitter positive.
75	**E11**	CPutp05-TD-	Board to Board connector3	B10	GTYTXN1_131	131	G37	O, DIFF	GTY Bank131 channel1 High speed differential transmitter negative.
76	**E12**	CPutp04-TD+	Board to Board connector3	B15	GTYTXP0_131	131	H34	O, DIFF	GTY Bank131 channel0 High speed differential transmitter positive.
77	**E13**	CPutp03-TD-	Board to Board connector3	C36	GTYTXN2_130	130	K35	O, DIFF	GTY Bank130 channel2 High speed differential transmitter negative.
78	**E14**	CPutp02-TD+	Board to Board connector3	C13	GTYTXP1_130	130	L36	O, DIFF	GTY Bank131 channel0 High speed differential transmitter positive.
79	**E15**	CPutp01-TD-	Board to Board connector3	C40	GTYTXN0_130	130	M35	O, DIFF	GTY Bank130 channel0 High speed differential transmitter negative.
80	**E16**	CSutp01-TD+	Board to Board connector3	A13	GTYTXP3_131	131	E36	O, DIFF	GTY Bank131 channel3 High speed differential transmitter positive.

SL No	VPX Connector Pin No	VPX Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
81	**F1**	DGND1	NA	NA	GND	NA	NA	Power	Ground.
82	**F2**	DP02-TD1-	Board to Board connector4	A15	GTHTXN1_230	230	P7	O, DIFF	GTH Bank230 channel1 High speed differential transmitter negative.
83	**F3**	DGND2	NA	NA	GND	NA	NA	Power	Ground.
84	**F4**	DP02-TD3-	Board to Board connector4	B13	GTHTXN3_230	230	M7	O, DIFF	GTH Bank230 channel3 High speed differential transmitter negative.
85	**F5**	DGND3	NA	NA	GND	NA	NA	Power	Ground.
86	**F6**	DP03-TD1-	Board to Board connector3	C56	GTHTXN1_231	231	K3	O, DIFF	GTH Bank231 channel1 High speed differential transmitter negative.
87	**F7**	DGND4	NA	NA	GND	NA	NA	Power	Ground.
88	**F8**	DP03-TD3-	Board to Board connector3	D59	GTHTXN3_231	231	H3	O, DIFF	GTH Bank231 channel3 High speed differential transmitter negative.
89	**F9**	DGND5	NA	NA	GND	NA	NA	Power	Ground.
90	**F10**	CPutp06-TD-	Board to Board connector3	A16	GTYTXN2_131	131	F35	O, DIFF	GTY Bank131 channel2 High speed differential transmitter negative.
91	**F11**	DGND6	NA	NA	GND	NA	NA	Power	Ground.
92	**F12**	CPutp04-TD-	Board to Board connector3	B14	GTYTXN0_131	131	H35	O, DIFF	GTY Bank131 channel0 High speed differential transmitter negative.
93	**F13**	DGND7	NA	NA	GND	NA	NA	Power	Ground.
94	**F14**	CPutp02-TD-	Board to Board connector3	C12	GTYTXN1_130	130	L37	O, DIFF	GTY Bank130 channel1 High speed differential transmitter negative.
95	**F15**	DGND8	NA	NA	GND	NA	NA	Power	Ground.
96	**F16**	CSutp01-TD-	Board to Board connector3	A12	GTYTXN3_131	131	E37	O, DIFF	GTY Bank131 channel3 High speed differential transmitter negative.
97	**G1**	MP01-TD	Board to Board connector2	50	UART1_TX(PS_MIO08_500)	500	AK33	O, 3V3 LVCMOS	Maintenance Port1 transmit data. This signal is connected to VPX Connector through Level translator(U1).
98	**G2**	DGND1	NA	NA	GND	NA	NA	Power	Ground.
99	**G3**	MP01-RD	Board to Board connector2	52	UART1_RX(PS_MIO09_500)	500	AK34	I, 3V3 LVCMOS	Maintenance Port1 receive data. This signal is connected to VPX Connector through Level translator(U1).
100	**G4**	DGND2	NA	NA	GND	NA	NA	Power	Ground.
101	**G5**	Reserved1	NA	NA	NA	NA	NA	NA	NC.
102	**G6**	DGND3	NA	NA	GND	NA	NA	Power	Ground.
103	**G7**	Maskable Reset	Board to Board connector2	40	PS_MIO44_501	501	R29	I, 3V3 LVCMOS/4.7PU	Maskable Reset This signal is connected to VPX Connector through Level translator (U2).
104	**G8**	DGND4	NA	NA	GND	NA	NA	Power	Ground.
105	**G9**	DGND5	NA	NA	GND	NA	NA	Power	Ground.

SL No	VPX Connector Pin No	VPX Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
106	**G10**	DGND6	NA	NA	GND	NA	NA	Power	Ground.
107	**G11**	MP02-TD	Board to Board connector2	81	PL_B18_LVDS68_L24 P	68	B18	O, 3V3 LVCMOS	Maintenance Port2 transmit data. This signal is connected to VPX Connector through Level translator(U1).
108	**G12**	DGND7	NA	NA	GND	NA	NA	Power	Ground.
109	**G13**	MP02-RD	Board to Board connector2	79	PL_A18_LVDS68_L24 N	68	A18	I, 3V3 LVCMOS	Maintenance Port2 Receive data. This signal is connected from VPX Connector through Level translator(U1).
110	**G14**	DGND8	NA	NA	GND	NA	NA	Power	Ground.
111	**G15**	Reserved2	NA	NA	NA	NA	NA	NA	NC.
112	**G16**	DGND9	NA	NA	GND	NA	NA	Power	Ground.

5.3 FireFly Connector1 Pinout

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports FireFly Connector1 through PL GTY transceiver Bank129 of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) PL. This GTY transceiver lanes are connected to FireFly data connector1 (J9) along with PS I2C0 & PL Bank IOs for configuration and control. And FireFly module power is supplied from FireFly power connector1 (J12).

Table 20 Firefly Data Connector1 (J9) Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
A1	GND_1	GND	Power	Ground.
A2	TX1N	GTYTXN0_129	O, DIFF	FireFly Transmit1 Data Negative
A3	TX1P	GTYTXP0_129	O, DIFF	FireFly Transmit1 Data Positive.
A4	GND_2	GND	Power	Ground.
A5	TX3N	GTYTXN2_129	O, DIFF	FireFly Transmit3 Data Negative
A6	TX3P	GTYTXP2_129	O, DIFF	FireFly Transmit3 Data Positive.
A7	GND_3	GND	Power	Ground.
A8	RSVD_1	NA	NA	NC
A9	RSVD_2	NA	NA	NC
A10	RSVD_3	NA	NA	NC
A11	RSVD_4	NA	NA	NC
A12	RSVD_5	NA	NA	NC
A13	GND_4	GND	Power	Ground.
A14	RX4P	GTYRXP3_129	I, DIFF	FireFly Receiver4 Data Positive
A15	RX4N	GTYRXN3_129	I, DIFF	FireFly Receiver4 Data Negative
A16	GND_5	GND	Power	Ground.
A17	RX2P	GTYRXP1_129	I, DIFF	FireFly Receiver2 Data Positive
A18	RX2N	GTYRXN1_129	I, DIFF	FireFly Receiver2 Data Negative
A19	GND_6	GND	Power	Ground.
B1	GND_7	GND	Power	Ground.
B2	TX2N	GTYTXN1_129	O, DIFF	FireFly Transmit2 Data Negative
B3	TX2P	GTYTXP1_129	O, DIFF	FireFly Transmit2 Data Positive.
B4	GND_8	GND	Power	Ground.
B5	TX4N	GTYTXN3_129	O, DIFF	FireFly Transmit4 Data Negative
B6	TX4P	GTYTXP3_129	O, DIFF	FireFly Transmit4 Data Positive.
B7	GND_9	GND	Power	Ground.
B8	RSVD_6	NA	NA	NC
B9	RSVD_7	NA	NA	NC
B10	RSVD_8	NA	NA	NC
B11	RSVD_9	NA	NA	NC
B12	RSVD_10	NA	NA	NC
B13	GND_10	GND	Power	Ground.
B14	RX3P	GTYRXP2_129	I, DIFF	FireFly Receiver3 Data Positive
B15	RX3N	GTYRXN2_129	I, DIFF	FireFly Receiver3 Data Negative
B16	GND_11	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
B17	RX1P	GTYRXP0_129	I, DIFF	FireFly Receiver1 Data Positive
B18	RX1N	GTYRXN0_129	I, DIFF	FireFly Receiver1 Data Negative
B19	GND_12	GND	Power	Ground.

Table 21 FireFly Power Connector1 (J12) Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC_TX	VCCTX_F_3V3	O, 3.3V Power	3.3V Transmit Supply Voltage
2	GND_14	GND	Power	Ground
3	MODPRS	PL_E5_LVDS94_L2P	I, 3.3V CMOS/ 4.7K PU	FireFly Module Present. This Pin is connected to E5 pin PL HD Bank 94 for software access if required.
4	MODSEL	PL_F5_LVDS94_L1P	O, 3.3V CMOS/ 4.7K PD	FireFly Module Select. This Pin is connected to F5 pin of pl HD Bank 94 for software access if required.
5	INTL	PL_F4_LVDS94_L1N	I, 3.3V CMOS/ 4.7K PU	FireFly Module Interrupt. This Pin is connected to F4 pin of PL HD Bank 94for software access if required.
6	RESETL	PL_A7_LVDS93_L10N	O, 3.3V CMOS/ 4.7K PU	FireFly Module Reset. This Pin is connected to A7 pin of PL HD Bank 93 for software access if required.
7	SDA	I2C0_SDA(PS_MIO11_500)	IO, 3.3V CMOS	I2C0 Data.
8	SCL	I2C0_SCL(PS_MIO10_500)	O, 3.3V CMOS	I2C0 Clock.
9	VCC_1.8V	VCC_F_1V8	O, 3.3V Power	1.8 V supply
10	VCC_RX	VCCRX_F_3V3	O, 3.3V Power	3.3V Receive Supply Voltage

5.4 FireFly Connector2 Pinout

The Zynq Ultrascale+ MPSoC (ZU19/17/11EG) 3U-VPX Plug-in Module supports FireFly Connector2 through PL GTY transceiver Bank128 of Zynq Ultrascale+ MPSoC (ZU19/17/11EG) PL. This GTY transceiver lanes are connected to FireFly data connector1 (J4) along with PS I2C0 & PL Bank IOs for configuration and control. And FireFly module power is supplied from FireFly power connector1 (J2).

Table 22 FireFly Data Connector2 (J4) Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
A1	GND_1	GND	Power	Ground.
A2	TX1N	GTYTXN0_128	O, DIFF	FireFly Transmit1 Data Negative
A3	TX1P	GTYTXP0_128	O, DIFF	FireFly Transmit1 Data Positive.
A4	GND_2	GND	Power	Ground.
A5	TX3N	GTYTXN2_128	O, DIFF	FireFly Transmit3 Data Negative
A6	TX3P	GTYTXP2_128	O, DIFF	FireFly Transmit3 Data Positive.
A7	GND_3	GND	Power	Ground.
A8	RSVD_1	NA	NA	NC
A9	RSVD_2	NA	NA	NC
A10	RSVD_3	NA	NA	NC
A11	RSVD_4	NA	NA	NC
A12	RSVD_5	NA	NA	NC
A13	GND_4	GND	Power	Ground.
A14	RX4P	GTYRXP3_128	I, DIFF	FireFly Receiver4 Data Positive
A15	RX4N	GTYRXN3_128	I, DIFF	FireFly Receiver4 Data Negative
A16	GND_5	GND	Power	Ground.
A17	RX2P	GTYRXP1_128	I, DIFF	FireFly Receiver2 Data Positive
A18	RX2N	GTYRXN1_128	I, DIFF	FireFly Receiver2 Data Negative
A19	GND_6	GND	Power	Ground.
B1	GND_7	GND	Power	Ground.
B2	TX2N	GTYTXN1_128	O, DIFF	FireFly Transmit2 Data Negative
B3	TX2P	GTYTXP1_128	O, DIFF	FireFly Transmit2 Data Positive.
B4	GND_8	GND	Power	Ground.
B5	TX4N	GTYTXN3_128	O, DIFF	FireFly Transmit4 Data Negative
B6	TX4P	GTYTXP3_128	O, DIFF	FireFly Transmit4 Data Positive.
B7	GND_9	GND	Power	Ground.
B8	RSVD_6	NA	NA	NC
B9	RSVD_7	NA	NA	NC
B10	RSVD_8	NA	NA	NC
B11	RSVD_9	NA	NA	NC
B12	RSVD_10	NA	NA	NC
B13	GND_10	GND	Power	Ground.
B14	RX3P	GTYRXP2_128	I, DIFF	FireFly Receiver3 Data Positive
B15	RX3N	GTYRXN2_128	I, DIFF	FireFly Receiver3 Data Negative
B16	GND_11	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
B17	RX1P	GTYRXP0_128	I, DIFF	FireFly Receiver1 Data Positive
B18	RX1N	GTYRXN0_128	I, DIFF	FireFly Receiver1 Data Negative
B19	GND_12	GND	Power	Ground.

Table 23 FireFly Power Connector2 (J2) Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC_TX	VCCTX_F1_3V3	O, 3.3V Power	3.3V Transmit Supply Voltage
2	GND_14	GND	Power	Ground
3	MODPRS	PL_J9_LVDS93_L3P	I, 3.3V CMOS/ 4.7K PU	FireFly Module Present. This Pin is connected to J9 pin of PL HD Bank 93 for software access if required.
4	MODSEL	PL_B8_LVDS93_L11P	O, 3.3V CMOS/ 4.7K PD	FireFly Module Select. This Pin is connected to B8 pin of PL HD Bank 93 for software access if required.
5	INTL	PL_A8_LVDS93_L11N	I, 3.3V CMOS/ 4.7K PU	FireFly Module Interrupt. This Pin is connected to A8 pin of PL HD bank 93 for software access if required.
6	RESETL	PL_E4_LVDS94_L2N	O, 3.3V CMOS/ 4.7K PU	FireFly Module Reset. This Pin is connected to E4 pin of PL HD Bank 94 for software access if required.
7	SDA	I2C1_SDA(PS_MIO25_500)	IO, 3.3V CMOS	I2C1 Data.
8	SCL	I2C1_SCL(PS_MIO24_500)	O, 3.3V CMOS	I2C1 Clock.
9	VCC_1.8V	VCC_F1_1V8	O, 3.3V Power	1.8 V supply
10	VCC_RX	VCCRX_F1_3V3	O, 3.3V Power	3.3V Receive Supply Voltage


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