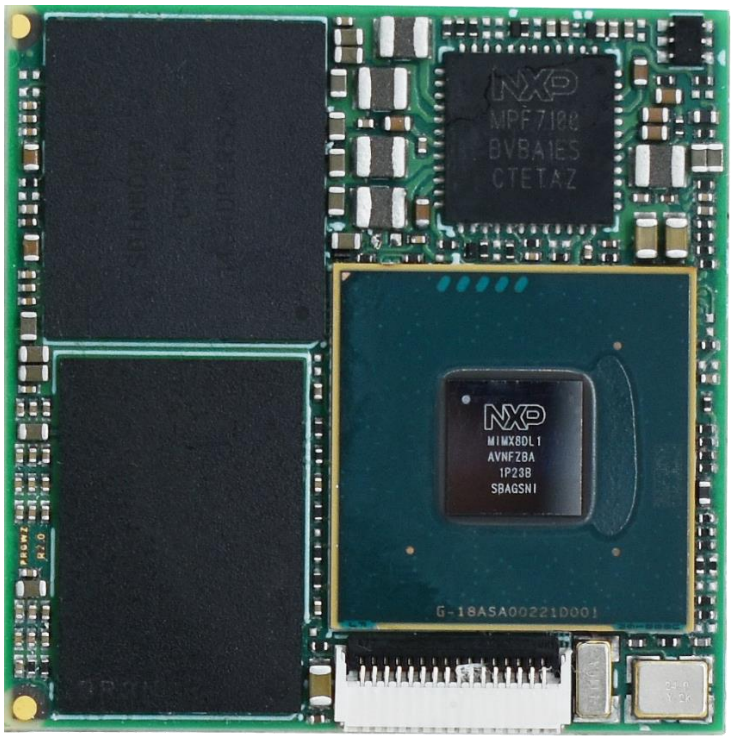
iW-RainboW-G46M
i.MX 8XLite Dual/Solo
OSM-Size SE LGA Module
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the NXP's i.MX 8XLite (Dual/Solo) Application processor based OSM v1.0 specification compatible LGA module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8XLite OSM Module from a Hardware Systems perspective.

1.2 OSM LGA Module Overview

The OSM V1.0 ("Open Standard Modules™") is a future proof and versatile standard for small size, low-cost embedded computer modules. Combining the following key characteristics like completely machine processible during soldering, assembly and testing, Pre-tinned LGA package for direct PCB soldering without connector.

The OSM Module definition targeting application that requires low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 8XLite SoC based OSM LGA Module is rich with i.MX 8XLite features along with on SOM LPDDR4, eMMC and comes in compact 30mm x 30mm form factor (Size S). The Module PCB has 332 contacts which can be mounted as LGA on OSM carrier card.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DP	Display Port
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface

Acronyms	Abbreviations
eMMC	Enhanced Multi Media Card
EMS	Electronics manufacturing services
ESAI	Enhanced Serial Audio Interface
FLEXCAN	Flexible Control Area Network
FlexSPI	Flexible Serial Peripheral Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
MLB	Media Local Bus
OSM	Open Standard Module
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SOM	System On Module
SPDIF	The Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPU	Video Processing Unit

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal

Terminology	Description
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
PCIe	PCIe differential pair signals
USB	Universal Serial Bus
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-OSM.

1.5 References

- IMX8DXLA1AEC_Revx.pdf
- iMX8DXL_RM_Rev_x.pdf
- OSM Specification V1.0

1.6 Important Note

In this document, wherever i.MX 8XLite SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET1_RGMII_TXC

  In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8XLite OSM LGA Module SOM and Hardware architecture with high level block diagram.

2.1 i.MX 8XLite OSM LGA Module Block Diagram

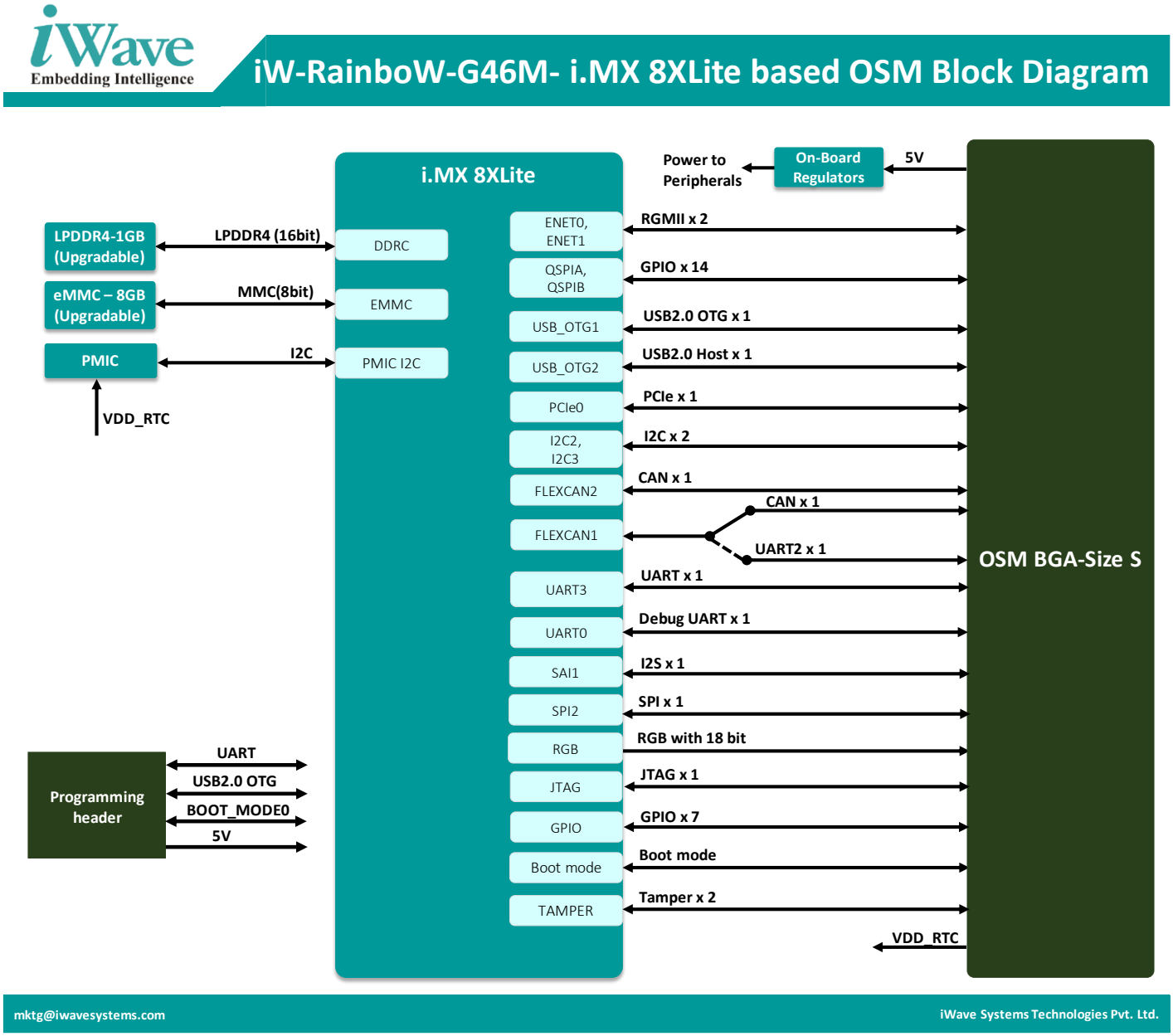

Figure 1: i.MX 8XLite OSM LGA MODULE Block Diagram

2.2 i.MX 8XLite SOM Features

i.MX 8XLite OSM LGA Module supports the following features.

SoC

- i.MX 8XLite Applications Processor
  - i.MX 8XLite Dual : 2 x Cortex-A35, 1 x Cortex-M4F
  - i.MX 8XLite Solo : 1 x Cortex-A35, 1 x Cortex-M4F

Power

- PF7100 PMIC

Memory

- LPDDR4 - 2GB (Expandable) [1]
- eMMC Flash - 8GB (Expandable)[1]

Other On-SOM Features

- Programming Header

OSM LGA Interfaces

- RGMII x 2
- USB 2.0 x 2
- PCIe 3.0 x 1
- SAI/I2S (Audio Interface) x 1
- SPI x 1
- Data UART (without CTS & RTS) x 2 [2]
- Debug UART x 1
- OSM GPIOs
- CAN-FD x 2
- I2C x 2
- Tamper x 2

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 30mm X 30mm (OSM V1.0 Specification)

1. *Memory Size will differ based on iWave's SOM Product Part Number.*
2. *By default, only 1 Data UART port is supported. 2nd UART is muxed with CAN.*

2.3 i.MX 8XLite SoC

iW-RainboW-G46M OSM LGA Module can support i.MX 8XLite SoCs from NXP. The i.MX 8XLite Family consists of two processors: i.MX 8XLite Dual & i.MX 8XLite Solo. The Major Difference between i.MX 8XLite SoCs are:

- i.MX 8XLite Dual : 2 x Cortex-A35, 1 x Cortex-M4F
- i.MX 8XLite Solo : 1 x Cortex-A35, 1 x Cortex-M4F

The i.MX 8XLite processors have advanced multicore processing with V2X acceleration supported by Arm cores. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1 and a wide range of peripheral I/Os such as PCIe 3.0 provide wide flexibility.

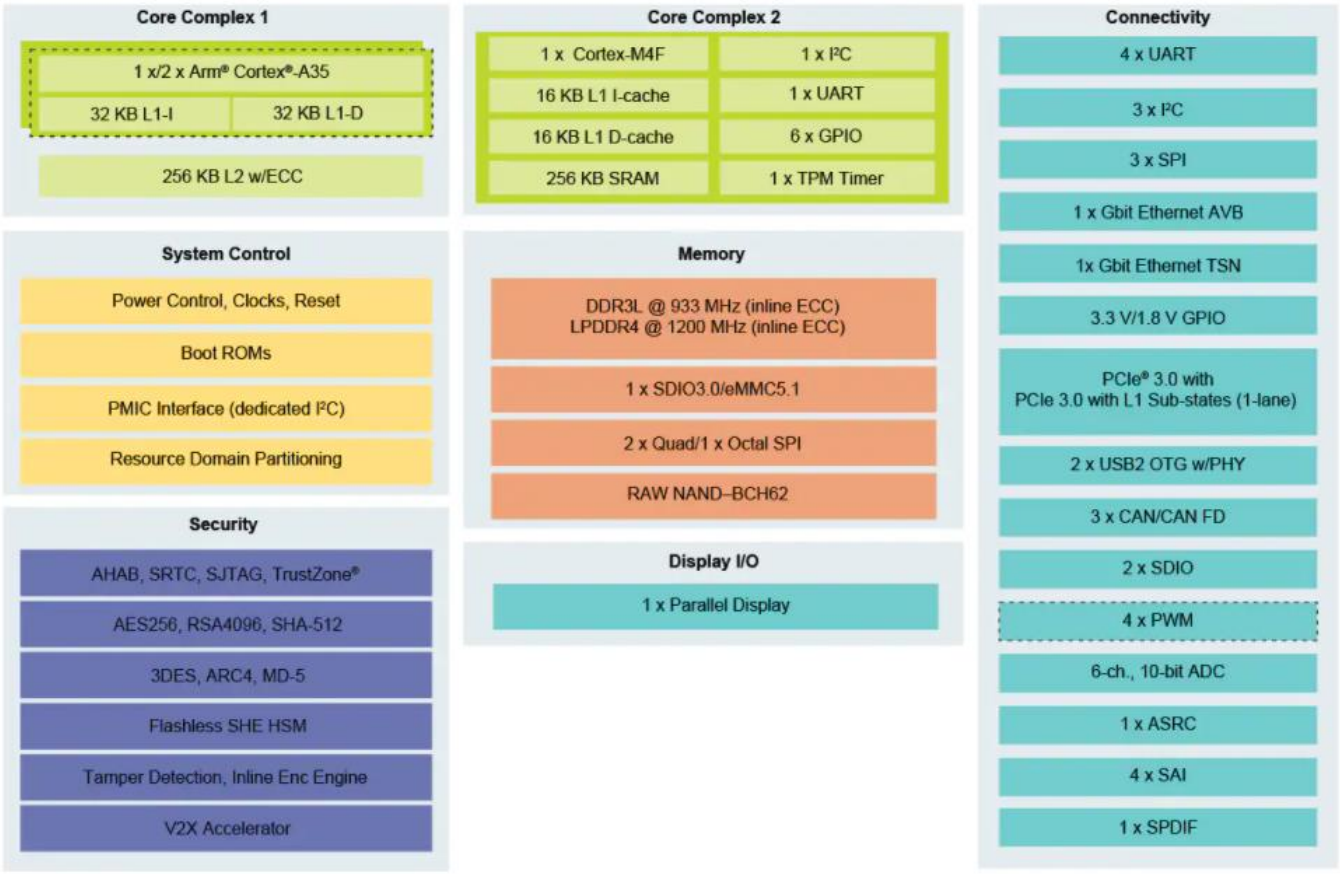

Figure 2: i.MX 8XLite Block Diagram

Note: The i.MX 8XLite processor offers numerous advanced features, please refer the latest i.MX 8XLite Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PF7100 PMIC

The i.MX 8XLite OSM LGA Module uses one PF7100 PMIC (U2) for module power management. The PF7100 features five high efficiency step-down regulators and two linear regulators. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PF7100 PMIC comes in 48pin 7x7 QFN Package and is placed on the Top side of the Module.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX 8XLite OSM LGA Module supports 2GB LPDDR4 RAM memory by default using 16bit DDR_CH0 channel of i.MX 8XLite SoC to support LPDDR4 up to 1.2GHz. LPDDR4 part U5 is placed on Top side of the Module. To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 8XLite OSM LGA Module supports 8GB eMMC as default boot and storage device. This is directly connected to eMMC controller of the i.MX 8XLite SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory (U3) is physically located on Top side of the Module. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.6 OSM LGA

OSM LGA has standard pinout as per OSM Specification V1.0 The interfaces which are available at 332 contacts are explained in the following sections.

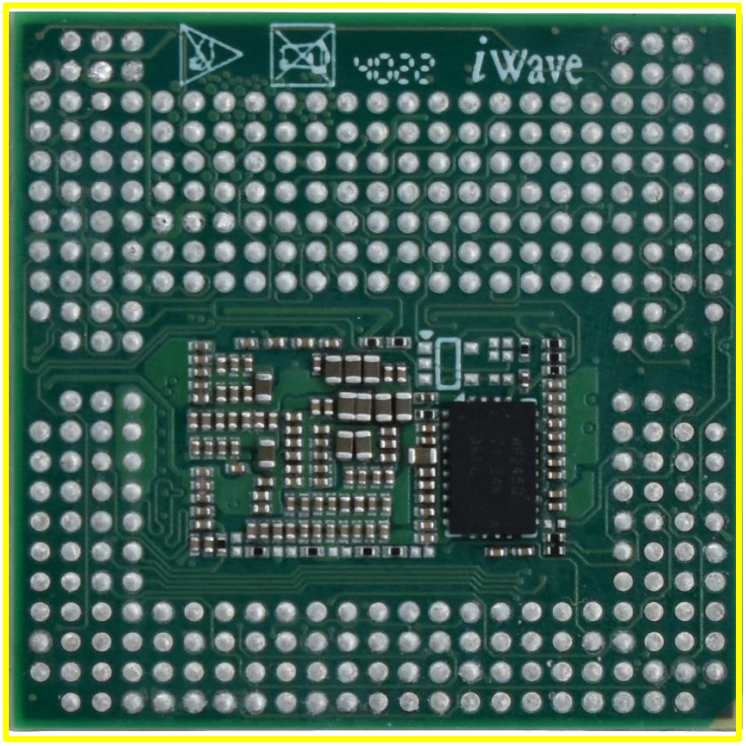

Figure 3: OSM LGA

Number of contacts - : 332

Table 3: OSM Pinouts

OSM Pins	Signal
SIZE 0	
M18	NC
N18	NC
U19	BOOT_MODE0
AB17	FLEXCAN1_RX
AC17	FLEXCAN1_TX
AB19	FLEXCAN2_RX
AC19	FLEXCAN2_TX
V17	CARRIER_PWR_ON
A15	GND
A16	GND
A17	GND
A18	GND
A19	GND
A20	GND
A21	GND
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
C15	NC
C17	NC
C19	NC
C21	NC
AC18	NC
F15	NC
E16	NC
R15	ENET0_QOS_RGMII_RXC
M15	ENET0_QOS_RGMII_RX_CTL
L16	NC
N15	ENET0_QOS_RGMII_RD2
P15	ENET0_QOS_RGMII_RD3
J15	ENET0_QOS_RGMII_TXC
K16	ENET0_QOS_RGMII_TX_CTL
H16	ENET0_QOS_RGMII_TD2
G16	ENET0_QOS_RGMII_TD3
K15	ENET0_QOS_RGMII_RD0

OSM Pins	Signal
L15	ENET0_QOS_RGMII_RD1
H15	ENET0_QOS_RGMII_TD0
G15	ENET0_QOS_RGMII_TD1
N16	NC
T16	ENET_QOS_MDC
T15	ENET_QOS_MDIO
D18	GND
E15	GND
E21	GND
F16	GND
F20	GND
J16	GND
J20	GND
L18	GND
M16	GND
M20	GND
P18	GND
R16	GND
R20	GND
V16	GND
V20	GND
Y18	GND
AA14	GND
AA17	GND
AA19	GND
AA22	GND
AB15	GND
AB21	GND
D17	GPIO3_IO20(QSPI0B_DATA2)
E17	GPIO3_IO21(QSPI0B_DATA3)
F17	GPIO3_IO18(QSPI0B_DATA0)
G17	GPIO3_IO19(QSPI0B_DATA1)
H17	GPIO3_IO22(QSPI0B_DQS)
J17	GPIO3_IO23(QSPI0B_SS0_B)
K17	GPIO3_IO17(QSPI0B_SCLK)
L17	GPIO3_IO16(QSPI0A_SCLK)
D19	GPIO3_IO14(QSPI0A_SS0_B)
E19	GPIO3_IO09(QSPI0A_DATA0)
F19	GPIO3_IO10(QSPI0A_DATA1)
G19	GPIO3_IO11(QSPI0A_DATA2)
H19	GPIO3_IO12(QSPI0A_DATA3)

OSM Pins	Signal
J19	NC
K19	ENET0_REFCLK_125M_25M
L19	NC
AA15	I2C2_SCL(SPI1_SDO)
AA16	I2C2_SDA(SPI1_SCK)
AA20	I2C3_SCL(SPI1_SDI)
AA21	I2C3_SDA(SPI1_CS0)
V21	SAI1_RXD(FLEXCAN1_TX)
W21	SAI1_TXD(FLEXCAN1_RX)
V19	NC
W19	NC
W20	SAI1_TXC(FLEXCAN0_RX)
W18	SAI1_TXFS(FLEXCAN0_TX)
V18	NC
R19	JTAG_NTRST
P19	NC
N17	JTAG_TCK
P17	JTAG_TDI
R17	JTAG_TDO
N19	JTAG_TMS
E18	NC
F18	NC
G18	NC
H18	NC
J18	NC
K18	NC
R18	BOOT_MODE1
T17	NC
T18	NC
T19	NC
Y13	NC
Y14	NC
AA13	NC
W17	VDD_RTC
J21	NC
F21	NC
E20	NC
G20	NC
G21	NC
H20	NC
H21	NC

OSM Pins	Signal
C20	NC
D21	NC
D20	NC
T21	NC
K20	NC
K21	NC
L20	NC
L21	NC
M21	NC
N20	NC
N21	NC
P20	NC
P21	NC
R21	NC
T20	NC
U21	NC
U20	NC
W15	NC
W16	NC
Y15	SPI2_CSO(USDHC1_CD_B)
U16	SPI2_SCK(USDHC1_RESET_B)
U15	SPI2_SDI(USDHC1_WP)
V15	SPI2_SDO(USDHC1_VSELECT)
AA23	NC
Y21	NC
Y22	NC
Y23	NC
U17	SYS_RST#
C18	NC
C14	NC
C13	NC
A14	ADMA_UART3_RX
B13	ADMA_UART3_TX
D16	NC
D15	NC
D14	UART2_RX
D13	UART2_TX
A22	NC
B23	NC
D22	UART0_RX
D23	UART0_TX

OSM Pins	Signal
C22	NC
C23	NC
AB13	USB_OTG1_DM
AC14	USB_OTG1_DP
AC16	USB_OTG1_PWR(USB_SS3_TC0)
AB14	USB_OTG1_ID
AC15	USB_OTG1_OC(USB_SS3_TC2)
AB16	OTG1_VBUS
AB23	USB_OTG2_DM
AC22	USB_OTG2_DP
AC20	USB_OTG2_PWR(USB_SS3_TC1)
AB22	USB_OTG2_ID
AC21	USB_OTG2_OC(USB_SS3_TC3)
AB20	OTG2_VBUS
AA18	NC
AB18	NC
M17	VDD_MAIN_1V0
M19	VDD_MEMC_1V1
Y16	VDD_PER_1V8
Y20	VCC_3V3
Y19	NC
Y17	VCC_IN_5V
U18	NC
B22	PMIC_ON_REQ
C16	NC
P16	NC
SIZE S	
C2	NC
G3	NC
G4	NC
B3	NC
B4	NC
C1	NC
B1	NC
A2	NC
A3	NC
A5	NC
A6	NC
B6	NC
B7	NC
AB8	NC

OSM Pins	Signal
AB7	NC
AB11	NC
AB10	NC
AC9	NC
AC8	NC
AC6	NC
AC5	NC
AB5	NC
AB4	NC
AA3	NC
E1	NC
D2	NC
P1	ENET1_RGMII_RXC
L1	ENET1_RGMII_RX_CTL
K2	NC
M1	ENET1_RGMII_RD2
N1	ENET1_RGMII_RD3
H1	ENET1_RGMII_TXC
J2	ENET1_RGMII_TX_CTL
G2	ENET1_RGMII_TD2
F2	ENET1_RGMII_TD3
J1	ENET1_RGMII_RD0
K1	ENET1_RGMII_RD1
G1	ENET1_RGMII_TD0
F1	ENET1_RGMII_TD1
M2	NC
P4	GND
D8	GND
B5	GND
AC10	GND
AC7	GND
AC4	GND
AB9	GND
AB6	GND
AB3	GND
AA11	GND
AA10	GND
AA8	GND
AA7	GND
AA4	GND
A4	GND

OSM Pins	Signal
A7	GND
A10	GND
B2	GND
B8	GND
B9	GND
C11	GND
D1	GND
D5	GND
E2	GND
H2	GND
H4	GND
L2	GND
L4	GND
P2	GND
U2	GND
U4	GND
V1	GND
W3	GND
Y2	GND
AA1	GND
R1	GND
D3	NC
D4	NC
E3	ENET1_REFCLK_125M_25M
E4	NC
F3	NC
F4	NC
C4	NC
C3	NC
AB2	PCIE0_A_RX0_N
AB1	PCIE0_A_RX0_P
AC3	PCIE0_A_TX0_N
AC2	PCIE0_A_TX0_P
V2	PCIE_RST_B
W2	PCIE_CLKREQ_B
Y1	PCIE_CPU_REFCLK100M_N
W1	PCIE_CPU_REFCLK100M_P
R2	GPIO3_IO13(QSPI0A_DQS)
T1	I2C2_SCL(SPI1_SDO)
U1	I2C2_SDA(SPI1_SCK)
T2	PCIE_WAKE_B

OSM Pins	Signal
AA9	CPU_ON_OFF
M4	ADMA_LCDIF_CLK(MCLK_OUT0)
R4	ADMA_LCDIF_D00_B0(SPI3_SCK)
R3	ADMA_LCDIF_D01_B1(SPI3_SDO)
P3	ADMA_LCDIF_D02_B2(SPI3_SDI)
N3	ADMA_LCDIF_D03_B3(MCLK_IN0)
N4	ADMA_LCDIF_D04_B4(UART1_TX)
M3	ADMA_LCDIF_D05_B5(UART1_RX)
H3	NC
J4	ADMA_LCDIF_RDE(SPI3_CS1)
K4	NC
W4	ADMA_LCDIF_D06_G0(UART1_RTS_B)
V3	ADMA_LCDIF_D07_G1(UART1_CTS_B)
V4	ADMA_LCDIF_D08_G2(SPI0_SCK)
U3	ADMA_LCDIF_D09_G3(SPI0_SDI)
T3	ADMA_LCDIF_D10_G4(SPI0_SDO)
T4	ADMA_LCDIF_D11_G5(SPI0_CS1)
K3	ADMA_LCDIF_HSYNC(SPI3_CS0)
Y7	ADMA_LCDIF_D12_R0(SPI0_CS0)
AA6	ADMA_LCDIF_D13_R1(ADC_IN1)_3V3
Y6	ADMA_LCDIF_D14_R2(ADC_IN0)_3V3
AA5	ADMA_LCDIF_D15_R3(ADC_IN3)_3V3
Y5	ADMA_LCDIF_D16_R4(ADC_IN2)_3V3
Y4	ADMA_LCDIF_D17_R5(ADC_IN5)_3V3
J3	ADMA_LCDIF_RESET(ADC_IN4)_3V3
L3	ADMA_LCDIF_VSYNC(MCLK_IN1)
N2	NC
AA2	NC
D11	NC
D10	NC
C10	NC
D9	NC
C8	NC
B11	NC
B10	NC
A9	NC
A8	NC
C9	NC
Y3	VDD_CPU_1V8
C5	VDD_DDR_1V1
Y9	VCC_IN_5V

OSM Pins	Signal
Y8	VCC_IN_5V
Y11	VCC_IN_5V
Y10	VCC_IN_5V
C6	GPIO2_IO05(SNVS_TAMPER_OUT1)
C7	GPIO2_IO10(SNVS_TAMPER_IN1)
D6	SNVS_TAMPER_IN4
D7	SNVS_TAMPER_OUT0

2.6.1 RGMII Interface

The i.MX 8XLite OSM LGA Module supports RGMII interface on OSM LGA. i.MX 8XLite provides two Ethernet Interfaces ENET0 with AVB and ENET1 with TSN support. The two RGMII Lanes are connected to OSM LGA. Connection of the i.MX 8XLite to the world wide web or a local area network (LAN) is possible using the GbE PHY which is off the module. The PHY can be selected which operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

For more details on ENET0 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
H15	ETH_A_(S)(R)(G)MII_TXD0	ENET0_QOS_RGMII_TD0	ENET0_RGMII_TXD0/J29	O CMOS	Transmit data bit 0 (transmitted first) port A
G15	ETH_A_(S)(R)(G)MII_TXD1	ENET0_QOS_RGMII_TD1	ENET0_RGMII_TXD1/G29	O CMOS	Transmit data bit 1 port A
H16	ETH_A_(R)(G)MII_TXD2	ENET0_QOS_RGMII_TD2	ENET0_RGMII_TXD2/L29	O CMOS	Transmit data bit 2 port A
G16	ETH_A_(R)(G)MII_TXD3	ENET0_QOS_RGMII_TD3	ENET0_RGMII_TXD3/N29	O CMOS	Transmit data bit 3 port A
K16	ETH_A_(R)(G)MII_TX_EN(_ER)	ENET0_QOS_RGMII_TX_CTL	ENET0_RGMII_TX_CTL/C35	O, CMOS	Transmit enable (Error) port A
J15	ETH_A_(R)(G)MII_TX_CLK	ENET0_QOS_RGMII_TXC	ENET0_RGMII_TXC/G27	I/O CMOS	Transmit clock port A
K15	ETH_A_(S)(R)(G)MII_RXD0	ENET0_QOS_RGMII_RD0	ENET0_RGMII_RXD0/B32	I CMOS	Receive data bit 0 (received first) port A
L15	ETH_A_(S)(R)(G)MII_RXD1	ENET0_QOS_RGMII_RD1	ENET0_RGMII_RXD1/A33	I CMOS	Receive data bit 1 port A
N15	ETH_A_(R)(G)MII_RXD2	ENET0_QOS_RGMII_RD2	ENET0_RGMII_RXD2/C31	I CMOS	Receive data bit 2 port A
P15	ETH_A_(R)(G)MII_RXD3	ENET0_QOS_RGMII_RD3	ENET0_RGMII_RXD3/A31	I CMOS	Receive data bit 3 port A
M15	ETH_A_(R)(G)MII_RX_DV(_ER)	ENET0_QOS_RGMII_RX_CTL	ENET0_RGMII_RX_CTL/C33	I CMOS	Receive data valid port A
R15	ETH_A_(R)(G)MII_RX_CLK	ENET0_QOS_RGMII_RXC	ENET0_RGMII_RXC/B34	I/O CMOS	Receive clock port A
T15	ETH_MDIO	ENET_QOS_MDIO	ENET0_MDIO/E35	I/O CMOS	Management data

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
T16	ETH_MDC	ENET_QOS_MDC	ENET0_MDC/E33	O CMOS	Management data clock

For more details on ENET1 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
G1	ETH_B_(S)(R)(G)MII_TXD0	ENET1_RGMII_TD0	ENET1_RGMII_TXD0/N33	O CMOS	Transmit data bit 0 (transmitted first) port A
F1	ETH_B_(S)(R)(G)MII_TXD1	ENET1_RGMII_TD1	ENET1_RGMII_TXD1/N35	O CMOS	Transmit data bit 1 port B
G2	ETH_B_(R)(G)MII_TXD2	ENET1_RGMII_TD2	ENET1_RGMII_TXD2/M34	O CMOS	Transmit data bit 2 port B
F2	ETH_B_(R)(G)MII_TXD3	ENET1_RGMII_TD3	ENET1_RGMII_TXD3/L33	O CMOS	Transmit data bit 3 port B
J2	ETH_B_(R)(G)MII_TX_EN(_ER)	ENET1_RGMII_TX_CTL	ENET1_RGMII_TX_CTL/R29	O CMOS	Transmit enable (Error) port B
H1	ETH_B_(R)(G)MII_TX_CLK	ENET1_RGMII_TXC	ENET1_RGMII_TXC/L35	I/O CMOS	Transmit clock port B
J1	ETH_B_(S)(R)(G)MII_RXD0	ENET1_RGMII_RD0	ENET1_RGMII_RXD0/J33	I CMOS	Receive data bit 0 (received first) port B
K1	ETH_B_(S)(R)(G)MII_RXD1	ENET1_RGMII_RD1	ENET1_RGMII_RXD1/F34	I CMOS	Receive data bit 1 port B
M1	ETH_B_(R)(G)MII_RXD2	ENET1_RGMII_RD2	ENET1_RGMII_RXD2/H34	I CMOS	Receive data bit 2 port B
N1	ETH_B_(R)(G)MII_RXD3	ENET1_RGMII_RD3	ENET1_RGMII_RXD3/G35	I CMOS	Receive data bit 3 port B
L1	ETH_B_(R)(G)MII_RX_DV(_ER)	ENET1_RGMII_RX_CTL	ENET1_RGMII_RX_CTL/J35	I/O CMOS	Receive clock port B
P1	ETH_B_(R)(G)MII_RX_CLK	ENET1_RGMII_RXC	ENET1_RGMII_RXC/G33	I/O CMOS	Receive clock port B

Note: On-OSM series termination resistors for ENET0_TX & ENET1_TX is not provided. Kindly provide the same in the Carrier Board.

2.6.2 USB 2.0 OTG Interface

The i.MX 8XLite OSM LGA Module supports one USB2.0 OTG interface and one USB2.0 Host.

i.MX 8XLite SoC's USB OTG controller supports two independent USB core and includes the PHY and I/O interfaces to support this operation. It supports High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps). It is fully compatible with the USB On-The-Go supplement to the USB 2.0 specification.

For more details on USB 2.0 OTG pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB13	USB_A_D_N	USB_OTG1_DM	USB_OTG1_DN/A19	IO, USB	USB2.0 Port0 Data Negative.
AC14	USB_A_D_P	USB_OTG1_DP	USB_OTG1_DP/B18	IO, USB	USB2.0 Port0 Data Positive.
AB14	USB_A_ID	USB_OTG1_ID	USB_OTG1_ID/C19	I, 3.3V CMOS	USB OTG ID.
AC15	USB_A_OC#	USB_OTG1_OC(USB_SS3_TC2)	USB_SS3_TC2/G25	I, 3.3V CMOS/ 10K PU	USB2.0 Port0 Over Current Indicator.
AB16	USB_A_VBUS	OTG1_VBUS	USB_OTG1_VBUS/G17	I USB VBUS 5V	USB Port0 power detection.
AC16	USB_A_EN	USB_OTG1_PWR(USB_SS3_TC0)	USB_SS3_TC0/G21	O, 3.3V CMOS	USB Power Enable.

2.6.3 USB 2.0 Host Interface

For more details on USB 2.0 Host pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB23	USB_B_D_N	USB_OTG2_DM	USB_OTG2_DN/B16	IO, 3.3V CMOS	USB2.0 Port1 Data Negative.
AC22	USB_B_D_P	USB_OTG2_DP	USB_OTG2_DP/A17	IO, USB	USB2.0 Port1 Data Positive.
AB22	USB_B_ID	USB_OTG2_ID	USB_OTG2_ID/G15	I, 3.3V CMOS	USB OTG ID.
AC21	USB_B_OC#	USB_OTG2_OC(USB_SS3_TC3)	USB_SS3_TC3/G23	I, 3.3V CMOS/ 10K PU	USB 2.0 Port1 Over Current Indicator.
AB20	USB_B_VBUS	OTG2_VBUS	USB_OTG2_VBUS/G13	I USB VBUS 5V	USB Port1 power detection.
AC20	USB_B_EN	USB_OTG2_PWR(USB_SS3_TC1)	USB_SS3_TC1/G19	O, 3.3V CMOS	USB Power Enable.

2.6.4 PCIe Interface

The i.MX 8XLite OSM LGA Module supports one lane PCIe 3.0 on OSM LGA. i.MX 8XLite SoC's PCIe0 lane with integrated PHY is directly connected to PCIe Link A port of OSM LGA. Internal PCIe Reference Clock is used. Also, PCIe reset and PCIe wake are supported on OSM LGA from i.MX 8XLite SoC IOs GPIO1_12 & GPIO1_14 respectively.

For more details on PCIe pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB1	PCIE_A_HSI0_P	PCIE0_A_RX0_P	PCIE0_RXN0_P/ A13	I, PCIe	PCIe Channel-A Transmit Positive.
AB2	PCIE_A_HSI0_N	PCIE0_A_RX0_N	PCIE0_RXN0_N/ B12	I, PCIe	PCIe Channel-A Receive Negative.
AC2	PCIE_A_HSI0_P	PCIE0_A_TX0_P	PCIE0_TXN0_P/ A11	O, PCIe / 0.1µF AC Couple	PCIe Channel-A Transmit Positive.
AC3	PCIE_A_HSO0_ N	PCIE0_A_TX0_N	PCIE0_TXN0_N/ B10	O, PCIe / 0.1µF AC Couple	PCIe Channel-A Transmit Negative.
W1	PCIE_REFCLK_P	PCIE_CPU_REFC LK100M_P	PCIE_REFCLK10 0M_P/A15	O, PCIe	PCIe Channel-A Clock Positive.
Y1	PCIE_REFCLK_N	PCIE_CPU_REFC LK100M_N	PCIE_REFCLK10 0M_N/B14	O, PCIe	PCIe Channel-A Clock Negative.
V2	PCIE_A_PERST#	PCIE_RST_B	PCIE_CTRL0_PE RST_B/B8	O, 3.3V CMOS	PCIe Channel-A Reset Out.
R2	PCIE_SM_ALERT #	GPIO3_IO13(QS PI0A_DQS)	QSPI0A_DQS/AR 9	I, 1.8V CMOS PU 2k2	SMBus Alert# (interrupt) signal
T2	PCIE_WAKE#	PCIE_WAKE_B	PCIE_CTRL0_WA KE_B/A9	I, 3.3V CMOS PU 10k	PCIe wake up interrupt to host – common to PCIe links A
W2	PCIE_A_PRSNT#	PCIE_CLKREQ_B	PCIE_CTRL0_CLK REQ_B/C9	I, 3.3V CMOS PU 10k	PCIe Port A present input

Note: As per Spec, PCIe differential transmitter lines has to be ac coupled off-the module. Kindly provide the same in the Carrier Board.

2.6.5 Audio Interface

The i.MX 8XLite OSM LGA Module supports I2S_A of OSM LGA from SoC's SAI1 channel. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including Transmitter section with independent

bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits and supports 49.152 MHz BCLK.

In i.MX 8XLite OSM LGA Module the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For pinouts on OSM Ball, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
W18	I2S_LRCLK	SAI1_TXFS(FLEXCAN0_TX)	FLEXCAN0_TX/ AJ35	IO, 1.8V CMOS	Serial left Right Synchronization Clock
W20	I2S_BITCLK	SAI1_TXC(FLEXCAN0_RX)	FLEXCAN0_RX/ AH34	IO, 1.8V CMOS	Serial Audio Interface Channel1 Clock
V21	I2S_A_DATA_IN	SAI1_RXD(FLEXCAN1_TX)	FLEXCAN1_TX/ AK34	IO, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
W21	I2S_A_DATA_OUT	SAI1_TXD(FLEXCAN1_RX)	FLEXCAN1_RX/ AJ33	IO, 1.8V CMOS	Serial Audio Interface Channel1 Data Output

2.6.6 SPI Interface

The i.MX 8XLite SoC supports Low Power Serial Peripheral Interface (LPSPI) module that supports an efficient interface to an SPI bus as a master with maximum clock speed of 60MHz and 40MHz in Slave mode. The i.MX 8XLite OSM supports SPIA channels of the OSM with SPI2 of CPU side.

For more details on SPI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y15	SPI_A_CS#	SPI2_CSO(uSDHC1_CD_B)	USDHC1_CD_B/ C29	O, 1.8V CMOS/ 10K PU	SPI0 Chip Select 0
U16	SPI_A_SCK	SPI2_SCK(uSDHC1_RESET_B)	USDHC1_RESET_B/ A29	O, 1.8V CMOS	SPI0 Clock
U15	SPI_A_SDI_(IO0)	SPI2_SDI(uSDHC1_WP)	USDHC1_WP/ B30	I, 1.8V CMOS	SPI0 Master IN Slave Out
V15	SPI_A_SDO_(IO1)	SPI2_SDO(uSDHC1_VSELECT)	USDHC1_VSELECT/ B28	I, 1.8V CMOS	SPI0 Master Out Slave In

2.6.7 Data UART

The i.MX 8XLite OSM supports three UART channels where one is optional. The i.MX i.MX 8XLite SoC's UART0, UART3 are connected to LGA balls whereas UART2 is optionally connected to the LGA. UART3 can be used for any data communication. UART0 of the SoC is connected to LGA and used as Debug UART.

For more details on UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A14	UART_A_RX	ADMA_UART3_RX	SCU_GPIO0_00/ AR27	I, 1.8V CMOS	UART3 Receiver.
B13	UART_A_TX	ADMA_UART3_TX	SCU_GPIO0_01/ AP26	O, 1.8V CMOS	UART3 Transmitter.
D22	UART_CON_RX	UART0_RX	UART0_RX/ AM34	O, 1.8V CMOS	Debug UART Transmitter. *Note: Optionally connected to on-Module programming header.*
D23	UART_CON_TX	UART0_TX	UART0_TX/ AN35	I, 1.8V CMOS	Debug UART Receiver. *Note: Optionally connected to on-Module programming header.*
D14	UART_B_RX	FLEXCAN1_RX(UART2_RX)	UART2_RX/ AN33	I, 1.8V CMOS	NC. *Note: Optional. By default, connected to CAN_A of OSM ball*
D13	UART_B_TX	FLEXCAN1_TX(UART2_TX)	UART2_TX/ AP34	O, 1.8V CMOS	NC. *Note: Optional. By default, connected to CAN_A of OSM ball*

2.6.8 CAN Interface

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported by the FlexCAN module.

The i.MX 8XLite SOC Supports two CAN interface and are connected to OSM Ball.

For more details of CAN pinouts on OSM Ball, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC17	CAN_A_TX	FLEXCAN1_TX(UART2_TX)	UART2_TX/AP34	O, 1.8V CMOS	CAN 1 Transmitter.
AB17	CAN_A_RX	FLEXCAN1_RX(UART2_RX)	UART2_RX/AN33	I, 1.8V CMOS	CAN 1 Receiver.
AC19	CAN_B_TX	FLEXCAN2_TX	FLEXCAN2_TX	O, 1.8V	CAN 2 Transmitter.

			/AL33	CMOS	
AB19	CAN_B_RX	FLEXCAN2_RX	FLEXCAN2_RX /AL35	I, 1.8V CMOS	CAN 2 Receiver.

2.6.9 RGB Interface

i.MX 8XLite SoC supports 8-bit, 16-bit, 18-bit parallel display.

For more details of RGB pinouts on OSM Ball, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M4	RGB_(PIXEL)CLK	ADMA_LCDIF_CLK(MCLK_OUT0)	MCLK_OUT0/V34	O, 3.3V CMOS	Pixel clock signal
R4	RGB_B0	ADMA_LCDIF_D00_B0(SPI3_SCK)	SPI3_SCK/P34	O, 3.3V CMOS	Blue data bit 0
R3	RGB_B1	ADMA_LCDIF_D01_B1(SPI3_SDO)	SPI3_SDO/R35	O, 3.3V CMOS	Blue data bit 1
P3	RGB_B2	ADMA_LCDIF_D02_B2(SPI3_SDI)	SPI3_SDI/R33	O, 3.3V CMOS	Blue data bit 2
N3	RGB_B3	ADMA_LCDIF_D03_B3(MCLK_IN0)	MCLK_IN1/U35	O, 3.3V CMOS	Blue data bit 3
N4	RGB_B4	ADMA_LCDIF_D04_B4(UART1_TX)	UART1_TX/W35	O, 3.3V CMOS	Blue data bit 4
M3	RGB_B5	ADMA_LCDIF_D05_B5(UART1_RX)	UART1_RX/W33	O, 3.3V CMOS	Blue data bit 5
J4	RGB_DE	ADMA_LCDIF_RDE(SPI3_CS1)	SPI3_CS1/U29	O, 3.3V CMOS	Data Enable
W4	RGB_G0	ADMA_LCDIF_D06_G0(UART1_RTS_B)	UART1_RTS_B /W29	O, 3.3V CMOS	Green data bit 0
V3	RGB_G1	ADMA_LCDIF_D07_G1(UART1_CTS_B)	UART1_CTS_B /AA29	O, 3.3V CMOS	Green data bit 1
V4	RGB_G2	ADMA_LCDIF_D08_G2(SPI0_SCK)	SPI0_SCK/Y34	O, 3.3V CMOS	Green data bit 2
U3	RGB_G3	ADMA_LCDIF_D09_G3(SPI0_SDI)	SPI0_SDI/AA33	O, 3.3V CMOS	Green data bit 3
T3	RGB_G4	ADMA_LCDIF_D10_G4(SPI0_SDO)	SPI0_SDO/AA35	O, 3.3V CMOS	Green data bit 4
T4	RGB_G5	ADMA_LCDIF_D11_G5(SPI0_CS1)	SPI0_CS1/AC35	O, 3.3V CMOS	Green data bit 5
K3	RGB_HSYNC	ADMA_LCDIF_HSYNC(SPI3_CS0)	SPI3_CS0/T34	O, 3.3V CMOS	Horizontal synch
Y7	RGB_R0	ADMA_LCDIF_D12_R0(SPI0_CS0)	SPI0_CS0/AB34	O, 3.3V CMOS	Red data bit 0
AA6	RGB_R1	ADMA_LCDIF_D13_R1(ADC_IN1)_3V3	ADC_IN1/AE35	O, 3.3V CMOS	Red data bit 1
Y6	RGB_R2	ADMA_LCDIF_D14_R2(ADC_IN0)_3V3	ADC_IN0/AD34	O, 3.3V CMOS	Red data bit 2
AA5	RGB_R3	ADMA_LCDIF_D15_R3(ADC_IN3)_3V3	ADC_IN3/AF34	O, 3.3V CMOS	Red data bit 3

Y5	RGB_R4	ADMA_LCDIF_D16_R4(ADC_IN2)_3V3	ADC_IN2/AC33	O, 3.3V CMOS	Red data bit 4
Y4	RGB_R5	ADMA_LCDIF_D17_R5(ADC_IN5)_3V3	ADC_IN5/AG35	O, 3.3V CMOS	Red data bit 5
J3	RGB_RESET#	ADMA_LCDIF_RESET(ADC_IN4)_3V3	ADC_IN4/AE33	O, 3.3V CMOS	Global Reset
L3	RGB_VSYNC	ADMA_LCDIF_VSYNC(MCLK_IN1)	MCLK_IN0/U33	O, 3.3V CMOS	Vertical synch

2.6.10 JTAG Interface

The i.MX 8XLite OSM supports JTAG interface for SoC debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG).

For more details on JTAG pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
N17	JTAG_TCK(SWCLK)	JTAG_TCK	JTAG_TCK/AR33	I CMOS ,1V8	JTAG test Clock.
N19	JTAG_TMS(SWDIO)	JTAG_TMS	JTAG_TMS/AP32	I CMOS ,1V8	JTAG test mode select.
P17	JTAG_TDI	JTAG_TDI	JTAG_TDI/AR31	I CMOS ,1V8	JTAG test data input.
R17	JTAG_TDO(SWO)	JTAG_TDO	JTAG_TDO/AN31	O CMOS ,1V8	JTAG test data output.

2.6.11 I2C Interface

The i.MX 8XLite OSM supports two I2C interface on OSM LGA. i.MX 8XLite SoC's I2C2 & I2C3 interfaces are connected to OSM LGA for I2C whereas i.MX 8XLite SoC's PMIC_I2C interface is connected to On-SOM PMIC.

For more details of I2C pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA15	I2C_A_SCL	I2C2_SCL(SPI1_SDO)	SPI1_SDO/ AR17	O, 1.8V CMOS 2.2K PU	I2C2 Clock.
AA16	I2C_A_SDA	I2C2_SDA(SPI1_SCK)	SPI1_SCK/ AP16	IO, 1.8V CMOS 2.2K PU	I2C2 Data.
AA20	I2C_B_SCL	I2C3_SCL(SPI1_SDI)	SPI1_SDI/ AP18	O, 1.8V CMOS 2.2K PU	I2C3 Clock.
AA21	I2C_B_SDA	I2C3_SDA(SPI1_CS0)	SPI1_CS0/ AR15	IO, 1.8V CMOS 2.2K PU	I2C3 Data.

2.6.12 OSM GPIOs

The i.MX 8XLite OSM supports GPIOs on OSM LGA in i.MX 8XLite OSM Development platform's default configuration. Most of the i.MX 8XLite SoC Pins which are connected to OSM LGA can be configured as GPIO with interrupt capable (if not used as other interface). The i.MX 8XLite SoC's GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

For more details on GPIO Interface pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D17	GPIO_A_0	GPIO3_IO20(QSPI0B_DATA2)	QSPI0B_DATA2/AR13	IO, 1.8V CMOS	OSM General Purpose Input/output A0.
E17	GPIO_A_1	GPIO3_IO21(QSPI0B_DATA3)	QSPI0B_DATA3/AP14	IO, 1.8V CMOS	OSM General Purpose Input/output A1.
F17	GPIO_A_2	GPIO3_IO18(QSPI0B_DATA0)	QSPI0B_DATA0/AP10	IO, 1.8V CMOS	OSM General Purpose Input/output A2.
G17	GPIO_A_3	GPIO3_IO19(QSPI0B_DATA1)	QSPI0B_DATA1/AP12	IO, 1.8V CMOS	OSM General Purpose Input/output A3.
H17	GPIO_A_4	GPIO3_IO22(QSPI0B_DQS)	QSPI0B_DQS/AN15	IO, 1.8V CMOS	OSM General Purpose Input/output A4.
J17	GPIO_A_5	GPIO3_IO23(QSPI0B_SS0_B)	QSPI0B_SS0_B/AJ11	IO, 1.8V CMOS	OSM General Purpose Input/output A5.
K17	GPIO_A_6	GPIO3_IO17(QSPI0B_SCLK)	QSPI0B_SCLK/AR7	IO, 1.8V CMOS	OSM General Purpose Input/output A6.
L17	GPIO_A_7	GPIO3_IO16(QSPI0A_SCLK)	QSPI0A_SCLK/AP8	IO, 1.8V CMOS	OSM General Purpose Input/output A7.
D19	GPIO_B_0	GPIO3_IO14(QSPI0A_SS0_B)	QSPI0A_SS0_BAN7	IO, 1.8V CMOS	OSM General Purpose Input/output B0.
E19	GPIO_B_1	GPIO3_IO09(QSPI0A_DATA0)	QSPI0A_DATA0/AR11	IO, 1.8V CMOS	OSM General Purpose Input/output B1.
F19	GPIO_B_2	GPIO3_IO10(QSPI0A_DATA1)	QSPI0A_DATA1/AN13	IO, 1.8V CMOS	OSM General Purpose Input/output B2.
G19	GPIO_B_3	GPIO3_IO11(QSPI0A_DATA2)	QSPI0A_DATA2/AN9	IO, 1.8V CMOS	OSM General Purpose Input/output B3.
H19	GPIO_B_4	GPIO3_IO12(QSPI0A_DATA3)	QSPI0A_DATA3/AN11	IO, 1.8V CMOS	OSM General Purpose Input/output B4.
K19	GPIO_B_6	ENET0_REFCLK_125M_25M	ENET0_REFCLK_125M_25M/D34	IO, 1.8V CMOS	OSM General Purpose Input/output B6.
E3	GPIO_C_2	ENET1_REFCLK_125M_25M	ENET1_REFCLK_125M_25M/K34	IO, 1.8V CMOS	OSM General Purpose Input/output C2.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
B22	VENDOR DEFINED1	PMIC_ON_REQ	PMIC_ON_REQ /AR19	O, 1.8V	Optionally connected.
C6	VENDOR DEFINED4	GPIO2_IO05(SNVS_TAMPER_OUT1)	SNVS_TAMPER_OUT1/ AP24	I, 1.8V	General Purpose Input.
C7	VENDOR DEFINED5	GPIO2_IO10(SNVS_TAMPER_IN1)	SNVS_TAMPER_IN1/AN17	I, 1.8V	General Purpose Input.
D6	VENDOR DEFINED6	SNVS_TAMPER_IN4	SNVS_TAMPER_IN4/AJ13	100K PD	Tamper IN4
D7	VENDOR DEFINED7	SNVS_TAMPER_OUT0	SNVS_TAMPER_OUT0/AP22	100K PD	Tamper OUT0

2.6.13 Control Signals

OSM V1.0 specification supports control Signals, for more details on OSM Control Signals pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U19	BOOT_SEL#	BOOT_MODE0	SCU_BOOT_MODE0/ AR23	I OD CMOS ,1.8V/4.7K PU	**BOOT_MODE (1:0)** **01**-USB Serial Download **10**-eMMC boot
R18	RSVD1	BOOT_MODE1	SCU_BOOT_MODE1/ AR25	I OD CMOS ,1.8V/4.7K PU	
U17	SYS_RST#	SYS_RST#	NA	I, 1.8V CMOS 100K PU	Hard RESET Input to SOM.
AA9	PWR_BTN#	CPU_ON_OFF	ON_OFF_BUTTON/ AR21	I, 1.8V CMOS 10K PU	Power ON /OFF Input to SOM.
V17	CARRIER_PWR_EN	CARRIER_PWR_ON	NA	O, 1.8V CMOS	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.

2.6.14 Power and GND

The i.MX 8XLite OSM LGA Module works with 5V power input (VCC) from OSM PCB Ball and generates all other required powers internally On-SOM itself. i.MX 8XLite OSM LGA Module also supports coin cell power input (VDD_RTC) from OSM PCB Ball to On-SOM RTC controller for real time clock.

For more details on Power & GND Signals pinouts on OSM PCB Ball, refer the below table.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y8, Y9, Y10, Y11, Y17	VCC_IN_5V	VCC_IN_5V	NA	I, 5V Power	Supply Voltage.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M17	VCC_1_TEST	VDD_ENET0	NA	I, 1.8V/3.3V POWER	Module power voltage test point
M19	VCC_2_TEST	VDD_MEMC_1V1	NA	I, 1.1V POWER	Module power voltage test point
Y16	VCC_3_TEST	VDD_PER_1V8	NA	I, 1.8V POWER	Module power voltage test point
Y20	VCC_4_TEST	VCC_3V3	NA	I, 3.3V POWER	Module power voltage test point
Y3	VCC_5_TEST	VDD_CPU_1V8	NA	I, 1.8V POWER	Module power voltage test point
C5	VCC_6_TEST	VDD_DDR_1V1	NA	I, 1.1V POWER	Module power voltage test point
D18,E15,E21,F16,F20,J16,J20,L18,M16,M20,P18,R16,R20,V16,V20,Y18,AA14,AA17,AA19,AA22,AB15,AB21,A4,A7,A10,B2,B5,B8,B9,C11,D1,D5,D8,E2,H2,H4,L2,L4,P2,P4,R1,U2,U4,V1,W3,Y2,AA1,AA4,AA7,AA8,AA10,AA11,AB3,AB6,AB9,AC4,AC7,AC10	GND	GND	NA	Power	Ground.
W17	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.7 Other Features

2.7.1 Programming Header

The i.MX 8XLite OSM LGA Module supports 16 pin programming header for testing the on-module features. The programming header is used for Flashing the board and getting the boot prints.

Number of Pins - 16

Connector Part - 503480-1600 from Molex

Table 4: Programming header Pin assignment

Pin No.	Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination
1	VCC_IN_5V	Power	Supply voltage
2	VCC_IN_5V	Power	Supply voltage
3	VCC_IN_5V	Power	Supply voltage
4	VCC_IN_5V	Power	Supply voltage
5	VCC_IN_5V	Power	Supply voltage
6	GND	Power	Ground
7	USB_OTG1_DM	IO, USB	USB2.0 Data Negative.
8	USB_OTG1_DP	IO, USB	USB2.0 Data Positive.
9	GND	Power	Ground
10	OTG1_VBUS	I, Power	USB VBUS power for detection.
11	GND	Power	Ground
12	UART0_RX	O, 1.8V CMOS	Debug UART Receiver.
13	UART0_TX	I, 1.8V CMOS	Debug UART Transmitter.
14	GND	Power	Ground
15	GND	Power	Ground
16	BOOT_MODE0	SCU_BOOT_MODE0/AR23	I OD CMOS ,1.8V/4.7K PU

2.8 i.MX 8XLite Pin Multiplexing on OSM LGA

The i.MX 8XLite SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8XLite SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8XLite SoC pin connections to the OSM Ball and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8XLite Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the OSM LGA for iWave's BSP reusability and to have compatible OSM modules in future for upgradability.

Table 5: i.MX 8XLite SoC IOMUX for OSM LGA interfaces

	OSM Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
ENET0	J15	G27	CONN.ENET0.RGMII_TXC	CONN.ENET0.RCLK50M_OUT	CONN.ENET0.RCLK50M_IN	CONN.NAND.CE1_B	LSIO.GPIO4.IO29	CONN.USDHC2.CLK	CONN.ENET0.RGMII_TXC
	K16	C35	CONN.ENET0.RGMII_TX_CTL			CONN.USDHC1.RESET_B	LSIO.GPIO4.IO30	CONN.USDHC2.CMD	CONN.ENET0.RGMII_TX_CTL
	H15	J29	CONN.ENET0.RGMII_TXD0			CONN.USDHC1.VSELECT	LSIO.GPIO4.IO31	CONN.USDHC2.DATA0	CONN.ENET0.RGMII_TXD0
	G15	G29	CONN.ENET0.RGMII_TXD1			CONN.USDHC1.WP	LSIO.GPIO5.IO00	CONN.USDHC2.DATA1	CONN.ENET0.RGMII_TXD1
	H16	L29	CONN.ENET0.RGMII_TXD2		CONN.NAND.CE0_B	CONN.USDHC1.CD_B	LSIO.GPIO5.IO01	CONN.USDHC2.DATA2	CONN.ENET0.RGMII_TXD2
	G16	N29	CONN.ENET0.RGMII_TXD3		CONN.NAND.RE_B		LSIO.GPIO5.IO02	CONN.USDHC2.DATA3	CONN.ENET0.RGMII_TXD3
	R15	B34	CONN.ENET0.RGMII_RXC		CONN.NAND.WE_B	CONN.USDHC1.CLK	LSIO.GPIO5.IO03		CONN.ENET0.RGMII_RXC
	M15	C33	CONN.ENET0.RGMII_RX_CTL			CONN.USDHC1.CMD	LSIO.GPIO5.IO04		CONN.ENET0.RGMII_RX_CTL
	K15	B32	CONN.ENET0.RGMII_RXD0			CONN.USDHC1.DATA0	LSIO.GPIO5.IO05		CONN.ENET0.RGMII_RXD0
	L15	A33	CONN.ENET0.RGMII_RXD1			CONN.USDHC1.DATA1	LSIO.GPIO5.IO06		CONN.ENET0.RGMII_RXD1
	N15	C31	CONN.ENET0.RGMII_RXD2	CONN.ENET0.RMII_RX_ER		CONN.USDHC1.DATA2	LSIO.GPIO5.IO07		CONN.ENET0.RGMII_RXD2

	OSM Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
	P15	A31	CONN.ENET0.RGMII_RXD3		CONN.NAND.ALE	CONN.USDHC1.DATA3	LSIO.GPIO5.IO08		CONN.ENET0.RGMII_RXD3
	K19	D34	CONN.ENET0.REFCLK_125M_25M	CONN.ENET0.PPS	CONN.EQOS.PPS_IN	CONN.EQOS.PPS_OUT	LSIO.GPIO5.IO09		CONN.ENET0.REFCLK_125M_25M
	T15	E35	CONN.ENET0.MDIO	ADMA.I2C3.SDA	CONN.EQOS.MDIO		LSIO.GPIO5.IO10	LSIO.GPIO7.IO16	CONN.ENET0.MDIO
	T16	E33	CONN.ENET0.MDC	ADMA.I2C3.SCL	CONN.EQOS.MDC		LSIO.GPIO5.IO11	LSIO.GPIO7.IO17	CONN.ENET0.MDC
SPI2	U16	A29	CONN.USDHC1.RESET_B	CONN.NAND.RE_N	ADMA.SPI2.SCK	CONN.NAND.WE_B	LSIO.GPIO4.IO19	LSIO.GPIO7.IO08	ADMA.SPI2.SCK
	V15	B28	CONN.USDHC1.VSELECT	CONN.NAND.RE_P	ADMA.SPI2.SDO	CONN.NAND.RE_B	LSIO.GPIO4.IO20	LSIO.GPIO7.IO09	ADMA.SPI2.SDO
	U15	B30	CONN.USDHC1.WP	CONN.NAND.DQS_N	ADMA.SPI2.SDI	CONN.NAND.ALE	LSIO.GPIO4.IO21	LSIO.GPIO7.IO10	ADMA.SPI2.SDI
	Y15	C29	CONN.USDHC1.CD_B	CONN.NAND.DQS_P	ADMA.SPI2.CS0	CONN.NAND.DQS	LSIO.GPIO4.IO22	LSIO.GPIO7.IO11	ADMA.SPI2.CS0
CAN1	AC17	AN33	ADMA.UART2.TX	ADMA.FTM.CH1	ADMA.FLEXCAN1.TX		LSIO.GPIO1.IO23	LSIO.GPIO6.IO16	ADMA.FLEXCAN1.TX
	AB17	AP34	ADMA.UART2.RX	ADMA.FTM.CH0	ADMA.FLEXCAN1.RX		LSIO.GPIO1.IO24	LSIO.GPIO6.IO17	ADMA.FLEXCAN1.RX
CAN2	AC19	AL35	ADMA.FLEXCAN2.RX	ADMA.SAI3.RXD	ADMA.UART3.RX	ADMA.SAI1.RXFS	LSIO.GPIO1.IO19	LSIO.GPIO6.IO12	ADMA.FLEXCAN2.RX
	AB19	AL33	ADMA.FLEXCAN2.TX	ADMA.SAI3.RXFS	ADMA.UART3.TX	ADMA.SAI1.RXC	LSIO.GPIO1.IO20	LSIO.GPIO6.IO13	ADMA.FLEXCAN2.TX
USB OTG1	AB16	G17	CONN.USB_OTG1.VBUS						CONN.USB_OTG1.VBUS
	AB14	C19	CONN.USB_OTG1.ID						CONN.USB_OTG1.ID
	AC14	B18	CONN.USB_OTG1.DP						CONN.USB_OTG1.DP
	AB13	A19	CONN.USB_OTG1.DN						CONN.USB_OTG1.DN
	AC16	G21	ADMA.I2C1.SCL	CONN.USB_OTG1.PWR	CONN.USB_OTG2.PWR		LSIO.GPIO4.IO03	LSIO.GPIO7.IO03	CONN.USB_OTG1.PWR

	OSM Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
	AC15	G25	ADMA.I2C1.SDA	CONN.USB_OTG1.OC	CONN.USB_OTG2.OC		LSIO.GPIO4.IO05	LSIO.GPIO7.IO05	CONN.USB_OTG1.OC
USB OTG2	AB20	G13	CONN.USB_OTG2.VBUS						CONN.USB_OTG2.VBUS
	AB22	G15	CONN.USB_OTG2.ID						CONN.USB_OTG2.ID
	AC22	A17	CONN.USB_OTG2.DP						CONN.USB_OTG2.DP
	AB23	B16	CONN.USB_OTG2.DM						CONN.USB_OTG2.DM
	AC20	G19	ADMA.I2C1.SCL	CONN.USB_OTG2.PWR			LSIO.GPIO4.IO04	LSIO.GPIO7.IO04	CONN.USB_OTG2.PWR
	AC21	G23	ADMA.I2C1.SDA	CONN.USB_OTG2.OC			LSIO.GPIO4.IO06	LSIO.GPIO7.IO06	CONN.USB_OTG2.OC
I2C	AA16	AP16	tiedoff input		ADMA.I2C2.SDA	ADMA.SPI1.SCK	LSIO.GPIO3.IO00		ADMA.I2C2.SDA
	AA15	AR17	tiedoff input		ADMA.I2C2.SCL	ADMA.SPI1.SDO	LSIO.GPIO3.IO01		ADMA.I2C2.SCL
	AA20	AP18	tiedoff input		ADMA.I2C3.SCL	ADMA.SPI1.SDI	LSIO.GPIO3.IO02		ADMA.I2C3.SCL
	AA21	AR15	tiedoff input		ADMA.I2C3.SDA	ADMA.SPI1.CS0	LSIO.GPIO3.IO03		ADMA.I2C3.SDA
UART	D22	AM34	ADMA.UART0.RX	ADMA.MQS.R	ADMA.FLEXCAN0.RX	SCU.UART0.RX	LSIO.GPIO1.IO21	LSIO.GPIO6.IO14	ADMA.UART0.RX
	D23	AN35	ADMA.UART0.TX	ADMA.MQS.L	ADMA.FLEXCAN0.TX	SCU.UART0.TX	LSIO.GPIO1.IO22	LSIO.GPIO6.IO15	ADMA.UART0.TX
	A14	AR27	SCU.GPIO0.IO00	SCU.UART0.RX	M40.UART0.RX	ADMA.UART3.RX	LSIO.GPIO2.IO03		ADMA.UART3.RX
	B13	AP26	SCU.GPIO0.IO01	SCU.UART0.TX	M40.UART0.TX	ADMA.UART3.TX	SCU.WDOG0.WDOG_OUT		ADMA.UART3.TX
Audio SAI	W20	AH34	ADMA.FLEXCAN0.RX	ADMA.SAI2.RXC	ADMA.UART0.RTS_B	ADMA.SAI1.TXC	LSIO.GPIO1.IO15	LSIO.GPIO6.IO08	ADMA.SAI1.TXC
	W18	AJ35	ADMA.FLEXCAN0.TX	ADMA.SAI2.RXD	ADMA.UART0.CTS_B	ADMA.SAI1.TXFS	LSIO.GPIO1.IO16	LSIO.GPIO6.IO09	ADMA.SAI1.TXFS

	OSM Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
	V21	AJ33	ADMA.FLEXCAN1.RX	ADMA.SAI2.RXFS	ADMA.FTM.CH2	ADMA.SAI1.TXD	LSIO.GPIO1.IO17	LSIO.GPIO6.IO10	ADMA.SAI1.TXD
	W21	AK34	ADMA.FLEXCAN1.TX	ADMA.SAI3.RXC	ADMA.DMA0.REQ_IN0	ADMA.SAI1.RXD	LSIO.GPIO1.IO18	LSIO.GPIO6.IO11	ADMA.SAI1.RXD
JTAG	N19	AP32	SCU.JTAG.TMS						SCU.JTAG.TMS
	N17	AR33	SCU.JTAG.TCK						SCU.JTAG.TCK
	R17	AN31	SCU.JTAG.TDO						SCU.JTAG.TDO
	P17	AR31	SCU.JTAG.TDI						SCU.JTAG.TDI
ENET1	H1	L35	LSIO.GPIO0.IO00	CONN.EQOS.RCLK50M_OUT	ADMA.LCDIF.D00	CONN.EQOS.RGMII_TXC	CONN.EQOS.RCLK50M_IN		CONN.EQOS.RGMII_TXC
	G2	M34	tiedoff input		ADMA.LCDIF.D01	CONN.EQOS.RGMII_TXD2	LSIO.GPIO0.IO01		CONN.EQOS.RGMII_TXD2
	J2	R29	tiedoff input		ADMA.LCDIF.D02	CONN.EQOS.RGMII_TX_CTL	LSIO.GPIO0.IO02		CONN.EQOS.RGMII_TX_CTL
	F2	L33	tiedoff input		ADMA.LCDIF.D03	CONN.EQOS.RGMII_TXD3	LSIO.GPIO0.IO03		CONN.EQOS.RGMII_TXD3
	P1	G33	tiedoff input		ADMA.LCDIF.D04	CONN.EQOS.RGMII_RXC	LSIO.GPIO0.IO04		CONN.EQOS.RGMII_RXC
	N1	G35	tiedoff input		ADMA.LCDIF.D05	CONN.EQOS.RGMII_RXD3	LSIO.GPIO0.IO05		CONN.EQOS.RGMII_RXD3
	M1	H34	tiedoff input		ADMA.LCDIF.D06	CONN.EQOS.RGMII_RXD2	LSIO.GPIO0.IO06	LSIO.GPIO6.IO00	CONN.EQOS.RGMII_RXD2
	K1	F34	tiedoff input		ADMA.LCDIF.D07	CONN.EQOS.RGMII_RXD1	LSIO.GPIO0.IO07	LSIO.GPIO6.IO01	CONN.EQOS.RGMII_RXD1
	G1	N33	tiedoff input		ADMA.LCDIF.D08	CONN.EQOS.RGMII_TXD0	LSIO.GPIO0.IO08	LSIO.GPIO6.IO02	CONN.EQOS.RGMII_TXD0
	F1	N35	tiedoff input		ADMA.LCDIF.D09	CONN.EQOS.RGMII_TXD1	LSIO.GPIO0.IO09	LSIO.GPIO6.IO03	CONN.EQOS.RGMII_TXD1
	J1	J33	ADMA.SPDIF0.RX	ADMA.MQS.R	ADMA.LCDIF.D10	CONN.EQOS.RGMII_RXD0	LSIO.GPIO0.IO10	LSIO.GPIO6.IO04	CONN.EQOS.RGMII_RXD0
	L1	J35	ADMA.SPDIF0.TX	ADMA.MQS.L	ADMA.LCDIF.D11	CONN.EQOS.RGMII_RX_CTL	LSIO.GPIO0.IO11	LSIO.GPIO6.IO05	CONN.EQOS.RGMII_RX_CTL
RGB	R4	P34	ADMA.SPI3.SCK		ADMA.LCDIF.D13		LSIO.GPIO0.IO13	ADMA.LCDIF.D00	ADMA.LCDIF.D00

	OSM Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
	R3	R35	ADMA.SPI3.SDO		ADMA.LCDIF.D14		LSIO.GPIO0.IO14	ADMA.LCDIF.D01	ADMA.LCDIF.D01
	P3	R33	ADMA.SPI3.SDI		ADMA.LCDIF.D15		LSIO.GPIO0.IO15	ADMA.LCDIF.D02	ADMA.LCDIF.D02
	K3	T34	ADMA.SPI3.CS0	ADMA.ACM.MCLK_OUT1	ADMA.LCDIF.HSYNC		LSIO.GPIO0.IO16	ADMA.LCDIF.CS	ADMA.LCDIF.HSYNC
	J4	U29	ADMA.SPI3.CS1	ADMA.I2C3.SCL	ADMA.LCDIF.RESET	ADMA.SPI2.CS0	ADMA.LCDIF.D16	ADMA.LCDIF.RD_E	ADMA.LCDIF.RD_E
	N3	U35	ADMA.ACM.MCLK_IN1	ADMA.I2C3.SDA	ADMA.LCDIF.EN	ADMA.SPI2.SCK	ADMA.LCDIF.D17	ADMA.LCDIF.D03	ADMA.LCDIF.D03
	L3	U33	ADMA.ACM.MCLK_IN0		ADMA.LCDIF.VSYNC	ADMA.SPI2.SDI	LSIO.GPIO0.IO19	ADMA.LCDIF.RS	ADMA.LCDIF.VSYNC
	M4	V34	ADMA.ACM.MCLK_OUT0		ADMA.LCDIF.CLK	ADMA.SPI2.SDO	LSIO.GPIO0.IO20	ADMA.LCDIF.WR_RWN	ADMA.LCDIF.CLK
	N4	W35	ADMA.UART1.TX	LSIO.PWM0.OUT	LSIO.GPT0.CAPTURE		LSIO.GPIO0.IO21	ADMA.LCDIF.D04	ADMA.LCDIF.D04
	M3	W33	ADMA.UART1.RX	LSIO.PWM1.OUT	LSIO.GPT0.COMPARE	LSIO.GPT1.CLK	LSIO.GPIO0.IO22	ADMA.LCDIF.D05	ADMA.LCDIF.D05
	W4	W29	ADMA.UART1.RTS_B	LSIO.PWM2.OUT	ADMA.LCDIF.D16	LSIO.GPT1.CAPTURE	LSIO.GPT0.CLK	ADMA.LCDIF.D06	ADMA.LCDIF.D06
	V3	AA29	ADMA.UART1.CTS_B	LSIO.PWM3.OUT	ADMA.LCDIF.D17	LSIO.GPT1.COMPARE	LSIO.GPIO0.IO24	ADMA.LCDIF.D07	ADMA.LCDIF.D07
	V4	Y34	ADMA.SPI0.SCK	ADMA.SAI0.TXC	M40.I2C0.SCL	M40.GPIO0.IO00	LSIO.GPIO1.IO04	ADMA.LCDIF.D08	ADMA.LCDIF.D08
	U3	AA33	ADMA.SPI0.SDI	ADMA.SAI0.TXD	M40.TPM0.CH0	M40.GPIO0.IO02	LSIO.GPIO1.IO05	ADMA.LCDIF.D09	ADMA.LCDIF.D09
	T3	AA35	ADMA.SPI0.SDO	ADMA.SAI0.TXFS	M40.I2C0.SDA	M40.GPIO0.IO01	LSIO.GPIO1.IO06	ADMA.LCDIF.D10	ADMA.LCDIF.D10
	T4	AC35	ADMA.SPI0.CS1	ADMA.SAI0.RXC	ADMA.SAI1.TXD	ADMA.LCD_PWM0.OUT	LSIO.GPIO1.IO07	ADMA.LCDIF.D11	ADMA.LCDIF.D11
	Y7	AB34	ADMA.SPI0.CS0	ADMA.SAI0.RXD	M40.TPM0.CH1	M40.GPIO0.IO03	LSIO.GPIO1.IO08	ADMA.LCDIF.D12	ADMA.LCDIF.D12
	AA6	AE35	ADMA.ADC.IN1	M40.I2C0.SDA	M40.GPIO0.IO01	ADMA.I2C0.SDA	LSIO.GPIO1.IO09	ADMA.LCDIF.D13	ADMA.LCDIF.D13

	OSM Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
	Y6	AD34	ADMA.ADC.IN0	M40.I2C0.SCL	M40.GPIO0.IO00	ADMA.I2C0.SCL	LSIO.GPIO1.IO10	ADMA.LCDIF.D14	ADMA.LCDIF.D14
	AA5	AF34	ADMA.ADC.IN3	M40.UART0.TX	M40.GPIO0.IO03	ADMA.ACM.MCLK_OUT0	LSIO.GPIO1.IO11	ADMA.LCDIF.D15	ADMA.LCDIF.D15
	Y5	AC33	ADMA.ADC.IN2	M40.UART0.RX	M40.GPIO0.IO02	ADMA.ACM.MCLK_IN0	LSIO.GPIO1.IO12	ADMA.LCDIF.D16	ADMA.LCDIF.D16
	Y4	AG35	ADMA.ADC.IN5	M40.TPM0.CH1	M40.GPIO0.IO05	ADMA.LCDIF.LCDBUSY	LSIO.GPIO1.IO13	ADMA.LCDIF.D17	ADMA.LCDIF.D17
	J3	AE33	ADMA.ADC.IN4	M40.TPM0.CH0	M40.GPIO0.IO04	ADMA.LCDIF.LCDRESET	LSIO.GPIO1.IO14		ADMA.LCDIF.LCDRESET
PCIe	V2	B8	HSIO.PCIE0.PERST_B						HSIO.PCIE0.PERST_B
	W2	C9	HSIO.PCIE0.CLKREQ_B						HSIO.PCIE0.CLKREQ_B
	T2	A9	HSIO.PCIE0.WAKE_B						HSIO.PCIE0.WAKE_B
	AC2	A11	HSIO.PCIE0.TX0_P						HSIO.PCIE0.TX0_P
	AC3	B10	HSIO.PCIE0.TX0_N						HSIO.PCIE0.TX0_N
	AB1	A13	HSIO.PCIE0.RX0_P						HSIO.PCIE0.RX0_P
	AB2	B12	HSIO.PCIE0.RX0_N						HSIO.PCIE0.RX0_N
	W1	A15	HSIO.PCIE_IOB.EXT_REFCLK100M_P						HSIO.PCIE_IOB.EXT_REFCLK100M_P
	Y1	B14	HSIO.PCIE_IOB.EXT_REFCLK100M_N						HSIO.PCIE_IOB.EXT_REFCLK100M_N
GPIO	E19	AR11	LSIO.QSPI0A.DATA0				LSIO.GPIO3.IO09		LSIO.GPIO3.IO09
	F19	AN13	LSIO.QSPI0A.DATA1				LSIO.GPIO3.IO10		LSIO.GPIO3.IO10
	G19	AN9	LSIO.QSPI0A.DATA2				LSIO.GPIO3.IO11		LSIO.GPIO3.IO11

	OSM Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
	H19	AN11	LSIO.QSPI0A.DATA3				LSIO.GPIO3.IO12		LSIO.GPIO3.IO12
	R2	AR9	LSIO.QSPI0A.DQS				LSIO.GPIO3.IO13		LSIO.GPIO3.IO13
	C7	AN17	tiedoff input		ADMA.SAI3.RXC	SNVS.TAMPER_IN1	LSIO.GPIO2.IO10_IN	LSIO.GPIO6.IO24_IN	LSIO.GPIO2.IO10_IN
	C6	AP24	tiedoff input			SNVS.TAMPER_OUT1	LSIO.GPIO2.IO05_IN	LSIO.GPIO6.IO19_IN	LSIO.GPIO2.IO05_IN
	K17	AR7	LSIO.QSPI0B.SCLK				LSIO.GPIO3.IO17		LSIO.GPIO3.IO17
	F17	AP10	LSIO.QSPI0B.DATA0				LSIO.GPIO3.IO18		LSIO.GPIO3.IO18
	G17	AP12	LSIO.QSPI0B.DATA1				LSIO.GPIO3.IO19		LSIO.GPIO3.IO19
	D17	AR13	LSIO.QSPI0B.DATA2				LSIO.GPIO3.IO20		LSIO.GPIO3.IO20
	E17	AP14	LSIO.QSPI0B.DATA3				LSIO.GPIO3.IO21		LSIO.GPIO3.IO21
	H17	AN15	LSIO.QSPI0B.DQS				LSIO.GPIO3.IO22		LSIO.GPIO3.IO22
	J17	AJ11	LSIO.QSPI0B.SS0_B				LSIO.GPIO3.IO23	LSIO.QSPI0A.SS1_B	LSIO.GPIO3.IO23
	L17	AP8	LSIO.QSPI0A.SCLK				LSIO.GPIO3.IO16		LSIO.GPIO3.IO16
	D19	AN7	LSIO.QSPI0A.SS0_B				LSIO.GPIO3.IO14		LSIO.GPIO3.IO14

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8XLite OSM LGA Module technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the five VCC_IN_5V in Size-S Module and returned through the numerous GND pins on the connector.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX 8XLite OSM LGA Module.

Table 6: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_IN_5V [1]	4.75	5V	5.25	-
2	VDD_RTC [2]	-	3V	-	-

[1] i.MX 8XLite OSM LGA Module is designed to work with VCC_IN_5V input power rail from OSM.
[2] i.MX 8XLite OSM LGA Module use this voltage as backup power source when VCC_IN_5V is OFF.

3.1.2 Power Consumption

Table 7: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Audio	VCC_IN_5V	0.165/0.825
Ping Ethernet (Eth0) at 1000Mbps	VCC_IN_5V	0.171/0.855
Ping Ethernet (Eth1) at 1000Mbps	VCC_IN_5V	0.174/0.87
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_IN_5V	0.168/0.84
eMMC to USB2.0 file transfer	VCC_IN_5V	0.26/1.3
eMMC to USB2.0 OTG file transfer	VCC_IN_5V	0.257/1.285
eMMC to M.2 PCIe file transfer	VCC_IN_5V	0.252/1.26
File Transfer - Transfer the 1GB files in storage devices	VCC_IN_5V	0.324/1.62
Dhrystone	VCC_IN_5V	0.288/1.44
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background	VCC_IN_5V	0.37/1.85
Low Power Mode Power Consumption		
System Idle Mode.	VCC_IN_5V	0.144/0.72
Deep Sleep Mode.	VCC_IN_5V	0.055/0.275
RTC power when no VCC_IN_5V supply is provided	VRTC_3V0	0.0000004/0.0000012

[1] Power consumption measurements have been done in iWave's i.MX 8XLite based Pico ITX SBC with iWave's iW-PRGWZ-SC-01-R2.0-REL1.0-Linux5.15.52 BSP.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 8XLite OSM LGA Module.

Table 8: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]For more information on Thermal solution & Heat sink, refer the following section.

3.2.2 Heat Sink

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Note: iWave supports Heat Sink Solution for i.MX 8XLite OSM LGA Module. For more information on Heat Sink contact iWave support team. Do not Power On the SOM without a proper thermal solution.

3.2.3 RoHS Compliance

iWave's i.MX 8XLite OSM LGA Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's i.MX 8XLite OSM LGA Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX 8XLite OSM LGA Module Mechanical Dimensions

i.MX 8XLite OSM LGA Module PCB size is 30 mm x 30 mm. Module mechanical dimensions are shown below. (All dimensions ae shown in mm).

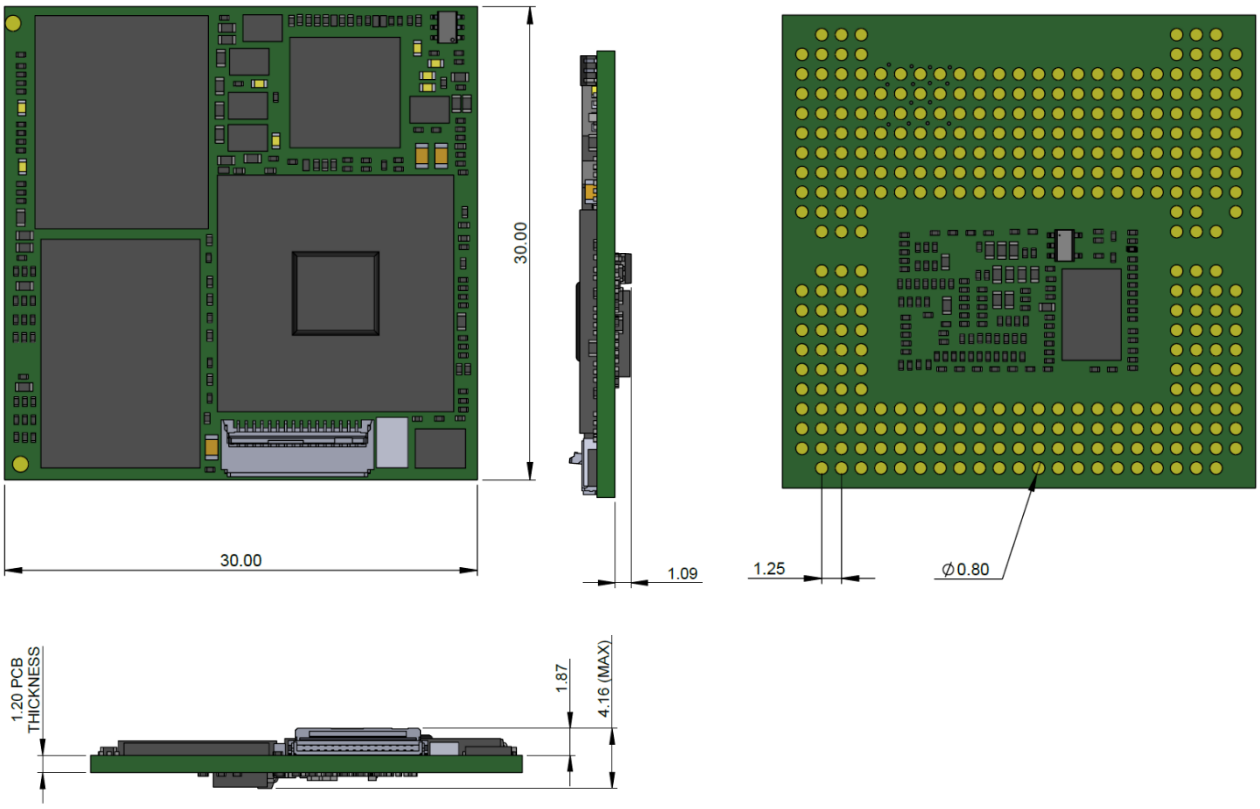

Figure 4: Mechanical dimension of i.MX 8XLite OSM LGA Module

The i.MX 8XLite OSM LGA Module PCB thickness is 1.2mm±0.1mm**,** top side maximum height component is 1.87mm (Programming Header). In bottom side maximum height component is Voltage Level Translator (1mm). Please refer the above figure which gives height details of the i.MX 8XLite OSM LGA Module.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8XLite OSM LGA Module variants. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 9: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G46M - i.MX 8XLite OSM R2.0 SOM		
iW-G46M-OSXD-4L002G-E008G-BIB	i.MX 8XLite Dual, 2GB LPDDR4, 8GB eMMC	-40°C to 85°C

Note:

** Some Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.*

** For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM.*

** Please contact iWave for other RAM and eMMC Configurations.*

** For AEC Grade Modules, please contact iWave.*

5. APPENDIX

5.1 i.MX 8XLite Pico ITX SBC

iWave Systems supports iW-RainboW-G46S-i.MX 8XLite Pico ITX SBC which is targeted for quick validation of i.MX 8XLite SoC based OSM and its features. Being a Pico-ITX form factor with 100mm x 72mm size, the SBC is highly packed with all necessary interfaces & on-board connectors to validate complete OSM supported features.

For more details on i.MX 8XLite SBC, visit the below web link.

https://www.iwavesystems.com/product/i-mx-8xlite-pico-itx-sbc/

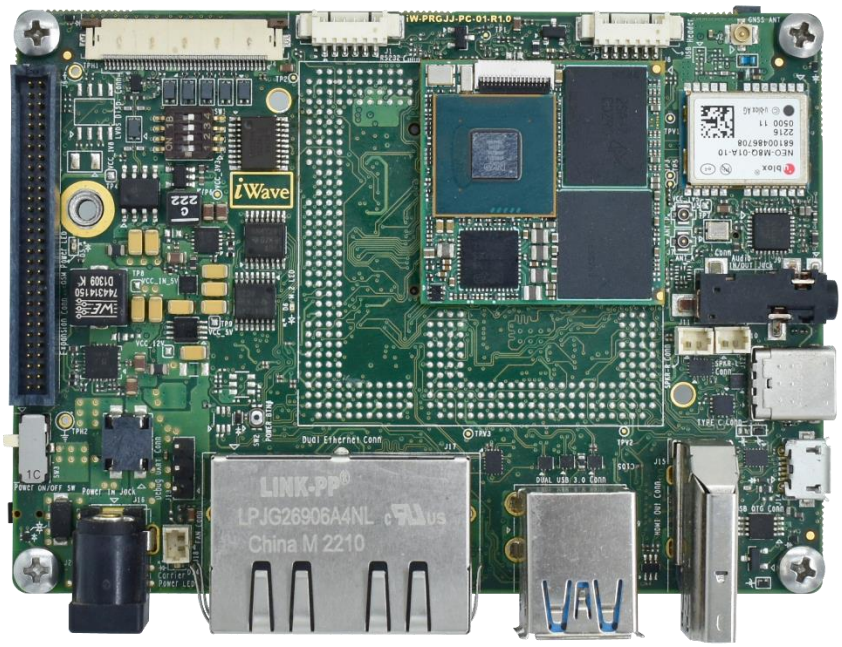

Figure 5: i.MX 8XLite Pico ITX SBC


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