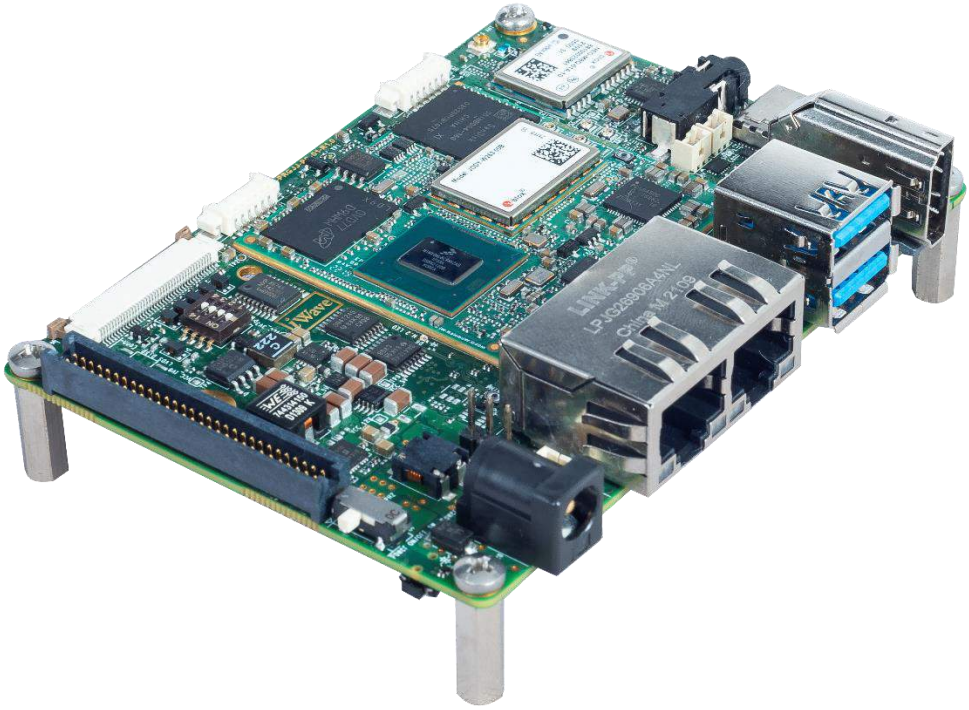
iW-RainboW-G40S

i.MX 8M Plus

Pico ITX Single Board Computer

Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Pico ITX Single Board Computer based on the NXP's i.MX 8M Plus Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8M Plus Pico ITX SBC from a Hardware Systems perspective.

1.2 Pico ITX SBC Overview

The Pico ITX is a versatile small form factor SBC (Single Board Computer) definition targeting application that require low power, low costs, and high performance. The SBCs are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE, GNSS module, LVDS and HDMI display connectors are concentrated on the SBC.

iWave's i.MX 8M Plus Pico ITX Single Board computer is rich with i.MX 8M Plus features along with eMMC, Dual Ethernet connector, Dual USB3.0 connector, GNSS module, Wi-Fi & BT module and comes in compact 100mm x 72mm form factor.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit

Acronyms	Abbreviations
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LVDS	Low Voltage Differential Signal
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OSM	Open standard Module
OTG	On-The-Go
PCB	Printed Circuit Sheet
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SBC	Single Board Computer
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on SBC.

1.5 References

- IMX8MPXEC_Rev_x.pdf
- iMX_8M_Plus_RM_Revx.pdf
- OSM Specification V1.0
- iW-RainboW-G40M_i.MX_8M_Plus_OSM_LGA_Module-HardwareUserGuide-RX.0-RELx.ypdf

1.6 Important Note

In this document, wherever i.MX 8M Plus SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_9)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO1_9*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8M Plus Pico ITX SBC features and Hardware architecture with high level block diagram.

2.1 i.MX 8M Plus Pico ITX SBC Block Diagram

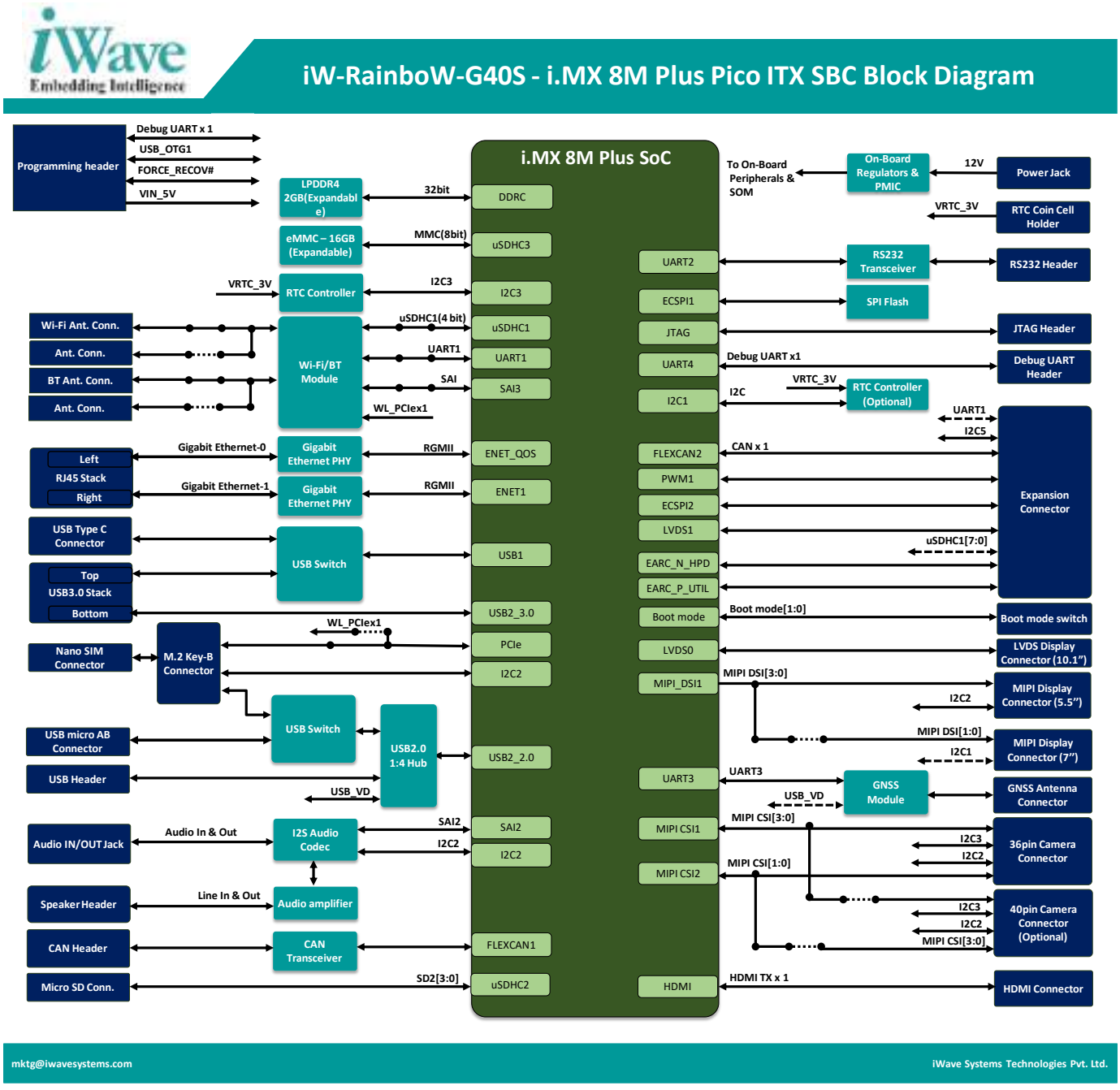

Figure 1: i.MX 8M Plus Pico ITX SBC Block Diagram

2.2 i.MX 8M Plus Pico ITX SBC Features

i.MX 8M Plus Pico ITX SBC supports the following features.

CPU

- i.MX 8M Plus Applications Processor[1]
  - i.MX 8M Plus Quad : 4 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP
  - i.MX 8M Plus Quad Lite : 4 x Cortex-A53, 1 x Cortex-M7 & GPU
  - i.MX 8M Plus Dual : 2 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP

Power

- PCA9450C PMIC

Memory

- LPDDR4 - 2GB (Expandable up to 8GB)
- eMMC Flash - 16GB (Expandable)[2]
- Micro SD slot
- 16Mb SPI Flash

Network & Communication

- WiFi 802.11a/b/g/n/ac/ax (ax is optional) + Bluetooth 5.0 Module
- Gigabit Ethernet PHY Transceiver with RJ45 Magjack Connector x 2
- USB 2.0, 4-Port Hub
- USB 3.0 x 2 (Dual stack type-A connector)
- USB Type-C Connector
- USB 2.0 OTG port through – micro AB Receptacle Connector
- GNSS Module
- RS232 Header x 1
- USB Header x 1
- CAN Header x 1

Audio/Video Features

- HDMI Output through HDMI (Type A) Connector
- 40pin, LVDS Display Connector
- I2S Audio Codec
- 3.5mm Audio IN/OUT
- Speaker out header

- 36pin MIPI_CSI Camera Connector
- 40pin MIPI_CSI Camera Connector (Optional)
- 39pin, 4 Lane MIPI_DSI Display Connector
- 15pin, 2 Lane MIPI_DSI Display Connector (Optional)

Expansion Connector Interfaces

- 4 lane LVDS x 1 Channel
- UART x 1 Port (Optional) [3]
- 8-bit SD (Optional) [4]
- SPI x 1 Port
- PWM x 1 Port
- CAN x 1 Port

Miscellaneous Interfaces

- RTC Controller with RTC Battery Header
- Debug UART Header
- JTAG Connector
- M.2 Connector Key B
    - PCIe × 1
    - USB 2.0 x 1
    - I2C x 1
    - Nano SIM Connector

General Specification

- Power Supply : 12V,2A[5]
- Form Factor : 100mm X 72mm

1. *There are six configurations of i.MX 8M Plus SoC supported by NXP, hence in this document i.MX 8M Plus Q/QL/D/DL/S/SL is used to represent either of one based on SBC Part Number.*
2. *Memory Size will differ based on iWave's SBC Product Part Number.*
3. *In default configuration, UART1 interface of i.MX 8M Plus is connected to the Bluetooth module. UART with CTS and RTS in the Expansion connector can be supported, if Bluetooth is not supported.*
4. *In default configuration, If Wi-Fi module is used, 8-bit SD will not be supported on Expansion connector.*
5. *The i.MX 8M Plus SBC can support input power 7V to 24V. By default, it is designed to support 12V.*

2.3 i.MX 8M Plus SoC

iW-RainboW-G40S Pico ITX SBC can support i.MX 8M Plus SoCs from NXP. The i.MX 8M Plus Family consists of three processors: i.MX 8M Plus Quad, I.MX 8M Plus Quad Lite & i.MX 8M Plus Dual. The Major Difference between i.MX 8M Plus SoCs are:

- i.MX 8M Plus Quad : 4 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP
- i.MX 8M Plus Quad Lite : 4 x Cortex-A53, 1 x Cortex-M7 & GPU
- i.MX 8M Plus Dual : 2 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP

The i.MX 8M Plus processors along with ARM core supports integrated NPU of 2.3 TOPs, OpenCL 1.2 GPU, Image Signal Processor, 1080p60 video encode and decode capable VPU, 3 x display controllers, multiple display output options, including MIPI_DSI, HDMI 2.0, and LVDS. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, SD 3.0 and a wide range of peripheral I/Os such as PCIe Gen3 provide wide flexibility.

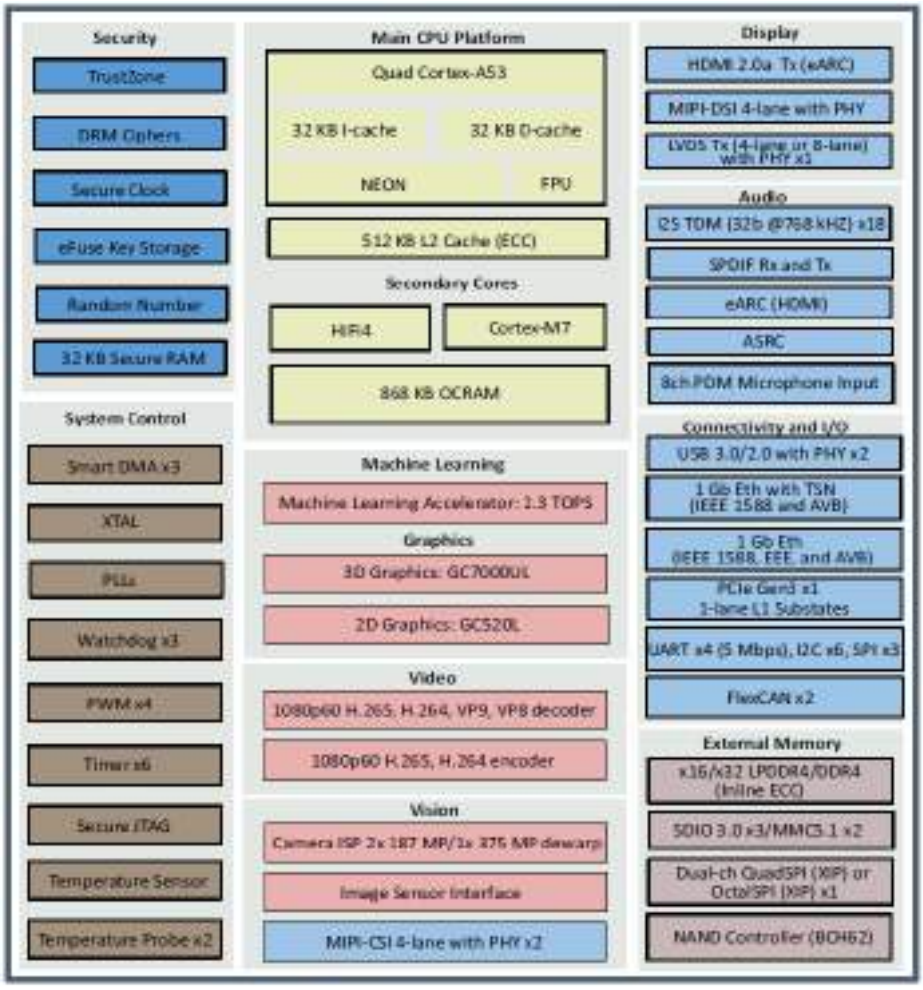

Figure 2: i.MX 8M Plus Block Diagram

Note: The i.MX 8M Plus processor offers numerous advanced features, please refer the latest i.MX 8M Plus Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PMIC

The i.MX 8M Plus Pico ITX SBC uses one PCA9450C PMIC (U3) for module power management. The PCA9450C features six high efficiency step-down regulators and five linear regulators. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PCA9450C PMIC comes in 56pin 7x7 QFN Package and is placed on the Top side of the SBC.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX 8M Plus Pico ITX SBC supports 2GB LPDDR4 RAM memory by default using 32bit DDR_CH0 channel of i.MX 8M Plus SoC to support LPDDR4 up to 2GHz. LPDDR4 part U12 is placed on Top side of the SBC. The RAM size can be expandable up to maximum of 8GB (if chips are available). To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 8M Plus Pico ITX SBC supports 16GB eMMC as default boot and storage device. This is directly connected to uSDHC3 controller of the i.MX 8M Plus SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory is physically located on bottom side of the LGA Module. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD Connector

The i.MX 8M Plus Pico ITX SBC supports Micro SD slot which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J26) is directly connected to the USDHC2 controller of the i.MX 8M Plus SoC. The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 8M Plus Pico ITX SBC supports configurable I/O voltage levels for uSDHC2 lines through GPIO1_IO4. If GPIO1_IO4 is set to low, then 3.3V IO level is selected for uSDHC2 lines. If GPIO1_IO4 is set to high, then 1.8V IO level is selected for uSDHC2 lines. The micro–SD Connector is physically located on bottom side of the i.MX 8M Plus Pico ITX SBC as shown below.

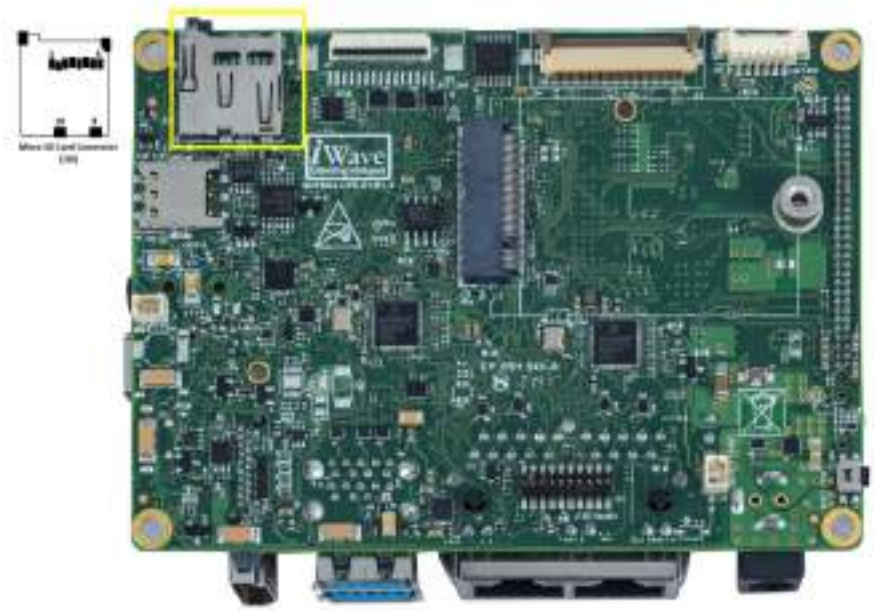

Figure 3: Micro SD Card Connector

2.6 Boot Media Setting

i.MX 8M Plus SoC boot process begins at Power on Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. i.MX 8M Plus SoC Boot ROM code uses the state of the internal register BOOT_MODE [1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device.

Note: Contact iWave if different boot media support is required other than eMMC.

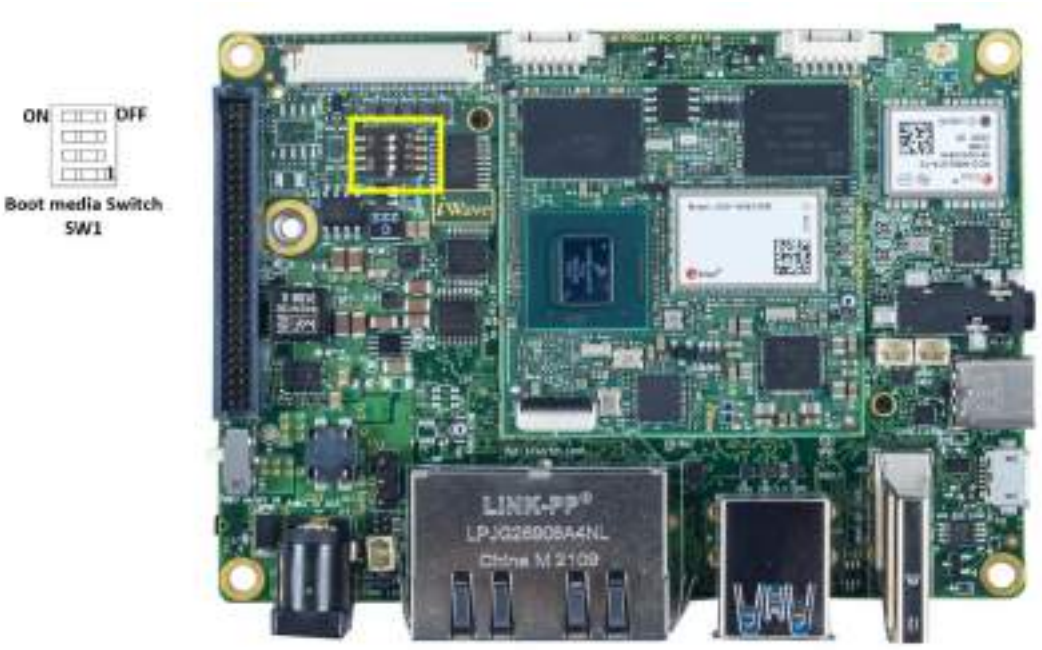

Figure 4: Boot Media Switch

Table 3: Boot Media Settings

Boot Media	Pin number	SW1 (4 Position Switch)			
		POS1	POS2	POS3	POS4
eMMC	1	OFF	OFF	OFF	OFF
uSD	2	ON	OFF	OFF	OFF
Serial Download mode	3	OFF	OFF	ON	OFF

2.7 Network & Communication

2.7.1 Wi-Fi and Bluetooth Interface

The i.MX 8M Plus Pico ITX SBC is integrated with u-blox's "JODY-W263" or "JODY-W374/JODY-W377" based Wi-Fi and Bluetooth module. The JODY-W2 series are compact modules based on the NXP 88W8987 AEC-Q100 compliant chipset and JODY-W3 series are based on the NXP 88W9098 chipset. They enable Wi-Fi, Bluetooth, and Bluetooth low energy communication.

The JODY-W2 modules can be operated in the following modes:

• Wi-Fi 1x1 802.11a/b/g/n/ac in 2.4 GHz or 5 GHz.

• Dual-mode Bluetooth 5.2, including audio, can be operated fully simultaneous with Wi-Fi.

The JODY-W2 undergoes extended automotive qualification according to ISO 16750-4 and is manufactured in line with ISO/TS 16949. Connection to a host processor is through SDIO, or High-Speed UART interfaces. The i.MX 8M Plus SBC uses processor's UART1 interface for Bluetooth and USDHC3 interface for Wi-Fi in a default configuration.

The JODY-W3 modules can be operated in the following modes:

• Wi-Fi 1x1 802.11a/b/g/n/ac/ax in 2.4 GHz and 5 GHz.

• Concurrent Dual Wi-Fi operation with independent MACs, supporting simultaneous Wi-Fi network operation at two different frequency bands.

• Dual-mode Bluetooth 5.3, can be operated fully simultaneous with Wi-Fi.

JODY-W3 modules undergo extended qualification testing in accordance with u-blox Qualification Policy based on AEC-Q104 and are manufactured in line with ISO/TS 16949 AEC-Q104. Host processor connections are made through various interfaces, including PCIe or SDIO for Wi-Fi and highspeed UART for Bluetooth. For 802.11ax, the i.MX 8M Plus SBC uses processor's PCIe interface for Wi-Fi6.

Antenna pins of JODY-W2/W3 Bluetooth and Wi-Fi are connected to J1, J2 connectors and optionally connected to connectors J5 and J7. J3 connector is optionally provided to support Bluetooth independently in JODY-W3.

Note: In default configuration, 802.11ax (Wi-Fi 6) is not supported, but 802.11ax can be supported by changing Wi-Fi module from JODY-W2 to JODY-W3 and some additional changes. Contact iWave Support Team for further information.

Figure 5: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : RECE-20449-001E-01 from Taoglas Limited / MM4829-2702RA4 from Murata.

Antenna Part Number - : FXP830.24.0100B from Taoglas Limited / 2042811100 from Molex

2.7.2 Gigabit Ethernet Interface

The i.MX 8M Plus Pico ITX SBC supports Dual Ethernet Port through external Ethernet PHYs.

The Ethernet PHY AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary Smart EEE. The Smart EEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

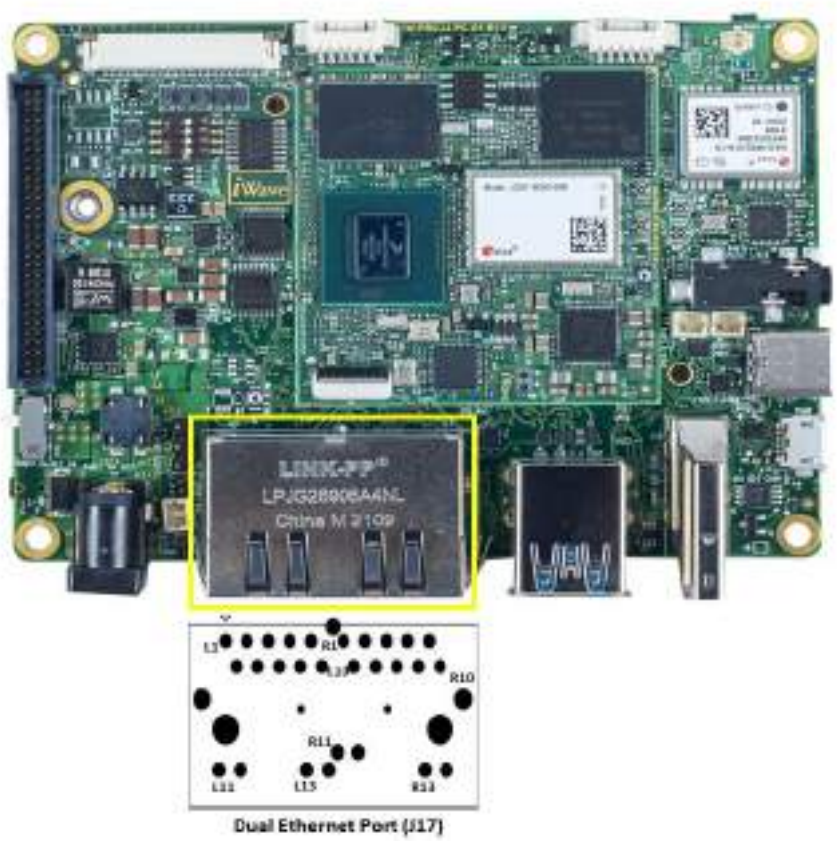

Figure 6: Dual RJ45 Magjack

2.7.3 USB3.0 Interface

The i.MX 8M Plus Pico ITX SBC supports one USB3.0 OTG through i.MX 8M Plus SoC's USB1. USB1 signals of SoC is connected to 1:2 data switch and then one output is connected to USB Type C connector (J12) for OTG as Device or Host support & other one to top port of dual stack USB3.0 Type A connector (J19) for OTG as Host only support.

The selection between USB Type C connector and top port of dual stack USB3.0 Type A connector can be done by setting the 4th bit of Boot media switch (SW1) to appropriate position. If the 4th bit of Board configuration switch (SW1) is set to OFF position, then USB Type C connector can be supported. If the 4th bit of Board configuration switch (SW1) is set to ON position, top port of dual stack USB3.0 Type A connector can be supported.

The VBUS power of USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin. This USB3.0 connector is physically located at the top of the board as shown below.

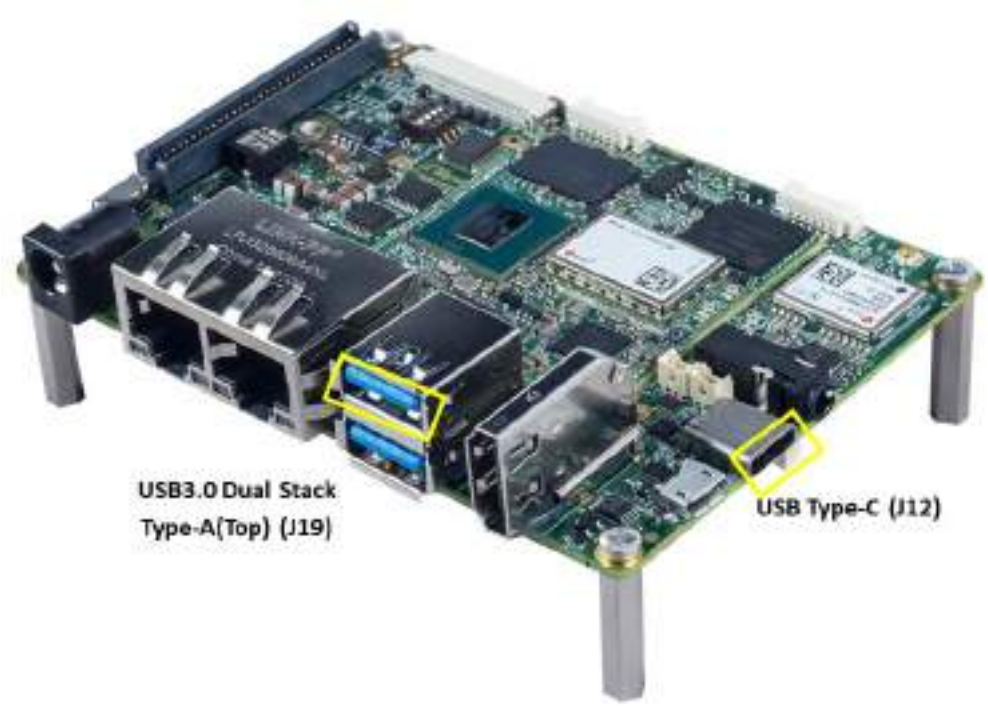

Figure7 USB 3.0 TOP And Type C

2.7.4 USB3.0 Host Port

The i.MX 8M Plus SBC supports USB3.0 Host through i.MX 8M Plus SoC's USB2 interface. Bottom port of dual stack USB3.0 Type A connector (J19) can be directly supported.

The VBUS power of this USB3.0 host connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin. This USB3.0 connector is physically located at the top of the board as shown below.

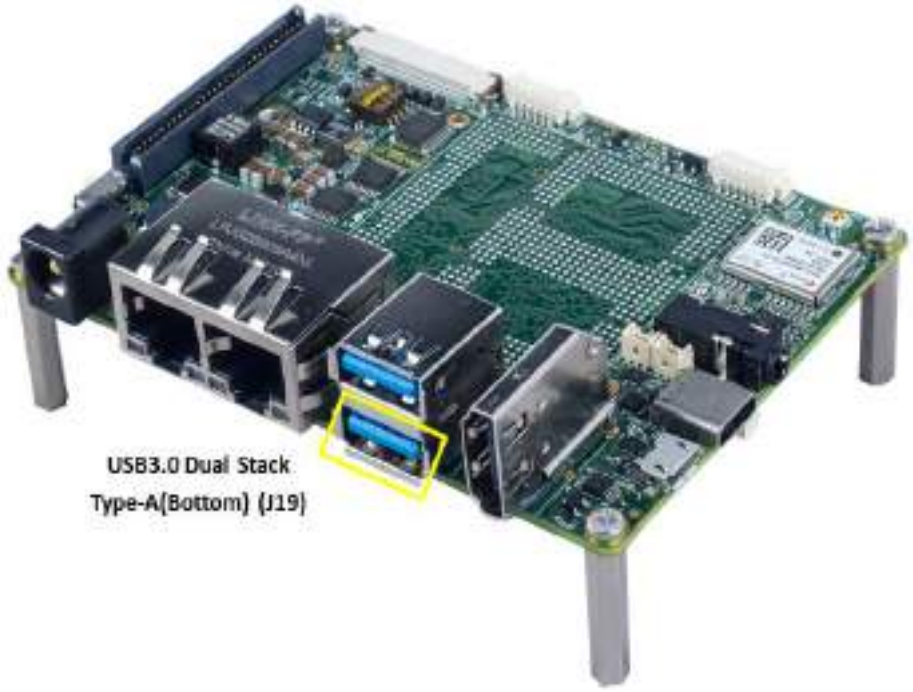

Figure 8: USB3.0 Host Port

2.7.5 USB2.0 OTG Interface

The i.MX 8M Plus Pico ITX SBC supports USB2.0 High Speed OTG interface. This USB2.0 signals is directly connected to 1:2 data switch and then one output is connected to USB2.0 Micro AB connector (J14) for OTG Host support & other one is connected to M.2 key B connector. USB Interface at M.2 Connector or OTG connector can be selected by changing the position of 2nd bit of switch(SW1). This USB2.0 OTG connector is physically located at the top of the board as shown below.

Figure 9: USB OTG Connector

2.7.6 GNSS Module

The i.MX 8M Plus Pico ITX SBC supports u-blox's "NEO-M8Q-01A" based GNSS module. The NEO-M8Q-01A module is built on the exceptional performance of the u-blox M8 GNSS engine in the industry proven NEO form factor. It utilizes concurrent reception of up to three GNSS systems (GPS/Galileo together with BeiDou or GLONASS) for more reliable positioning.

The NEO-M8Q-01A provides high sensitivity and minimal acquisition times while maintaining low system power. The NEO-M8Q-01A combines a high level of robustness and integration capability along with flexible connectivity options via USB, I2C UART and SPI. The DDC (I2C compatible) interface provides connectivity and enables synergies with most u-blox cellular modules.

The i.MX 8M Plus Pico ITX SBC makes use of the UART3 interface. Active antenna can be connected to the the connector J2 which is on the top of the SBC as shown in the below image.

Figure 10: GNSS Antenna Connector

Connector Part Number : 734120110 from Molex.

Antenna Part Number : TBD

2.7.7 CAN Interface

The i.MX 8M Plus Pico ITX SBC supports a Control Area Network (CAN) Port. FLEXCAN1 of the SoC is connected to MCP2562FD-E/SN CAN Transceiver and CANL & CANH of the transceiver are connected to J23 connector. The Connector is placed on Bottom Side of the Board.

Number of Pins:6

Connector Part Number: 532610671 from Molex

Figure 11: CAN Header

Table 4: CAN Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V_CAN0	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	NC.
3	CANL	CAN0_L	IO, DIFF	CAN Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN0_H	IO, DIFF	CAN High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.8 Serial Interface Features

2.8.1 Debug UART Interface

The i.MX 8M Plus Pico ITX SBC supports debug interface through SoC's UART4 interface. This UART4 signals from the SoC is connected to Debug UART header(J13) through 1.8V to 3.3V level Translator.

Figure 12: Debug UART Header

Table 5: Debug UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	TX	UART4_RXD	I, 3.3V CMOS	UART interface Receive signal.
2	RX	UART4_TXD	O, 3.3V CMOS	UART interface Transmit signal.
3	GND	GND	Power	Ground.

2.8.2 RS232 Data UART Interface

The i.MX 8M Plus Pico ITX SBC supports RS232 Data Interface through SoC's UART2 interface. By default, this UART2 signals from the SoC is connected to "MAX3232" RS-232 Line Driver and Receiver via 1.8V to 3.3V level Translator. The RS232 Signals are connected from MAX3232 to RS232 Header (J1), which is physically located at the top of the board as shown below.

Number of Pins: 6

Connector Part number:532610671 from Molex

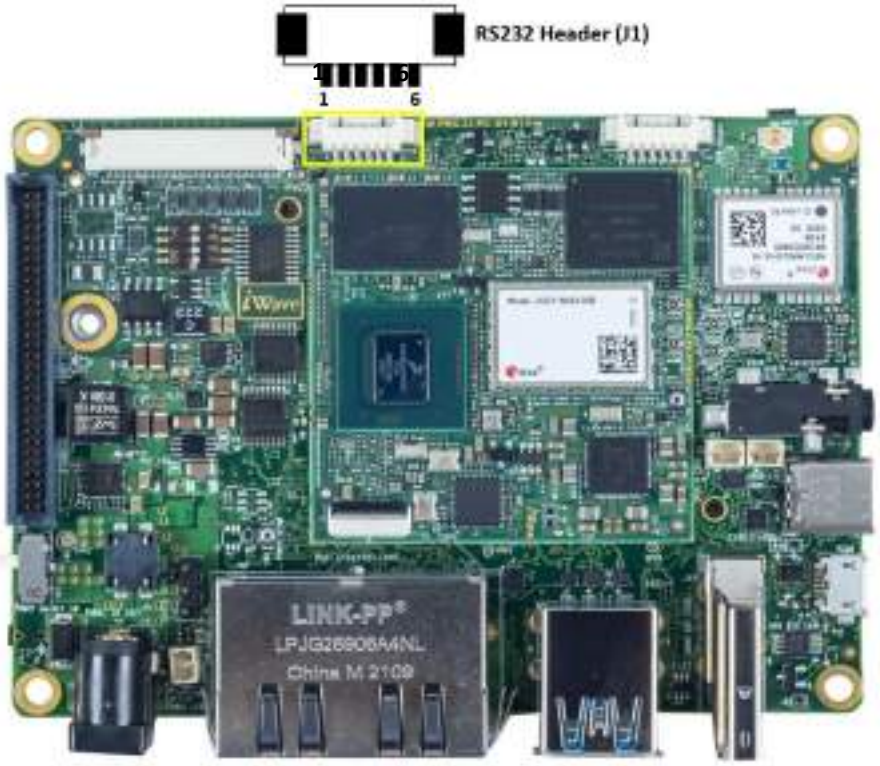

Figure 13: RS232 Header

Table 6: RS232 Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS	RS232_CTS	O, RS232	RS232 interface Clear to Send signal.
3	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	TXD	RS232_RXD	I, RS232	RS232 interface Receive signal.
5	RXD	RS232_TXD	O, RS232	RS232 interface Transmit signal.
6	RTS	RS232_RTS	I, RS232	RS232 interface Ready to Send signal.

2.9 Audio/Video Features

2.9.1 MIPI CSI Connector

The i.MX 8M Plus SBC supports two 4-lane camera connectors J25(36 Pin) and J24 (40 Pin-optional). 36 Pin connector supports 4 lane MIPI_CSI1 and 2 Lane MIPI_CSI2 and the optional 40 Pin connector supports 4 Lane MIPI_CSI1 and MIPI_CSI2. The CSI-2 Rx Controller Core is compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. This MIPI CSI camera connector J25/J24 is physically located on bottom of the board as shown below.

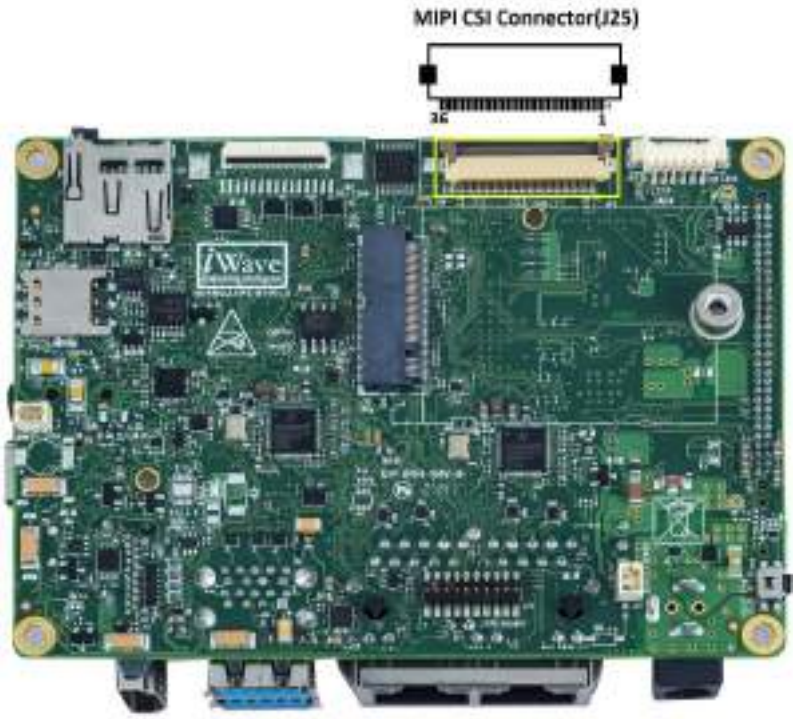

Figure 14: 36 pin MIPI CSI Connector

Number of Pins : 36

Connector Part : FH12A-36S-0.5SH(55) from Hirose Electric Co Ltd

Table 7: MIPI CSI Connector Pinouts

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
2	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
3	CAM0_CSI_D0+	CSI_DATA0_P	I, MIPI	MIPI CSI1 differential data lane 0 positive.
4	CAM0_CSI_D0-	CSI_DATA0_N	I, MIPI	MIPI CSI1 differential data lane 0 negative.
5	GND	GND	Power	Ground.
6	CAM0_CSI_D1+	CSI_DATA1_P	I, MIPI	MIPI CSI1 differential data lane 1 positive.

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
7	CAM0_CSI_D1-	CSI_DATA1_N	I, MIPI	MIPI CSI1differential data lane 1 negative.
8	GND	GND	Power	Ground.
9	CAM0_CSI_D2+	CSI_DATA2_P	I, MIPI	MIPI CSI1 differential data lane 2 positive.
10	CAM0_CSI_D2-	CSI_DATA2_N	I, MIPI	MIPI CSI1 differential data lane 2 negative.
11	CAM0_RST#	CAM0_RST(GPIO_C_7)	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal
12	CAM0_CSI_D3+	CSI_DATA3_P	I, MIPI	MIPI CSI1 differential data lane 3 positive.
13	CAM0_CSI_D3-	CSI_DATA3_N	I, MIPI	MIPI CSI1 differential data lane 3 negative.
14	GND	GND	Power	Ground.
15	CAM0_CSI_CLK+	CSI_CLOCK_P	I, MIPI	MIPI CSI1 differential Clock positive.
16	CAM0_CSI_CLK-	CSI_CLOCK_N	I, MIPI	MIPI CSI1 differential Clock negative.
17	GND	GND	Power	Ground.
18	CAM0_I2C_CLK	I2C_CAM_SCL	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI CSI1 Camera.
19	CAM0_I2C_DAT	I2C_CAM _SDA	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI CSI1 Camera.
20	CAM0_ENA#	NC	I, 1.8V CMOS/10K PU	Camera 0 Enable (active low). *Note:* *Optionally connected to CAM0_EN(GPIO_C_6)*
21	MCLK	CAM_MCK	I, 1.8V CMOS	Master Clock.
22	CAM1_ENA#	NC	I, 1.8V CMOS/10K PU	Camera 1 Enable (active low). *Note:* *Optionally connected to CAM1_EN(GPIO_B_1)*
23	CAM1_I2C_CLK	I2C_A_SCL	I, 1.8V OD	I2C clock Optional
24	CAM1_I2C_DAT	I2C_A_SDA	IO,1V8 OD	I2C Data Optional
25	GND	GND	Power	Ground.
26	CAM1_CSI_CLK+	CSI_2_CLOCK_P(VD_15)	I, MIPI	MIPI CSI2 differential Clock positive
27	CAM1_CSI_CLK-	CSI_2_CLOCK_N(VD_14)	I, MIPI	MIPI CSI2 differential Clock negative.
28	GND	GND	Power	Ground.
29	CAM1_CSI_D0+	CSI_2_DATA0_P(VD_17)	I, MIPI	MIPI CSI2 differential data lane 0 positive.

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
30	CAM1_CSI_D0-	CSI_2_DATA0_N(VD_16)	I, MIPI	MIPI CSI2 differential data lane 0 negative.
31	CAM1_RST#	CAM1_RST	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal *Note:* *Optionally connected to CAM1_RST(GPIO_B_2)*
32	CAM1_CSI_D1+	CSI_2_DATA1_P(VD_19)	I, MIPI	MIPI CSI2 differential data lane 1 positive.
33	CAM1_CSI_D1-	CSI_2_DATA1_N(VD_18)	I, MIPI	MIPI CSI2 differential data lane 1 negative.
34	GND	GND	Power	Ground.
35	CAM0_GPIO	USB_C_SW(GPIO_B_3)	I, 1.8V CMOS/10K PU	*Note:* *Optionally connected*
36	CAM1_GPIO	CAM1_GPIO(GPIO_B_4)	I, 1.8V CMOS/10K PU	*Note:* *Optionally connected*

Number of Pins : 40

Connector Part : FH12A-40S-0.5SH(55) from Hirose Electric Co Ltd

Table 8: MIPI CSI 40 Pin Connector Pinouts(Optional)

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
2	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
3	CAM0_CSI_D0+	CSI_DATA0_P	I, MIPI	MIPI CSI1 differential data lane 0 positive.
4	CAM0_CSI_D0-	CSI_DATA0_N	I, MIPI	MIPI CSI1 differential data lane 0 negative.
5	GND	GND	Power	Ground.
6	CAM0_CSI_D1+	CSI_DATA1_P	I, MIPI	MIPI CSI1 differential data lane 1 positive.
7	CAM0_CSI_D1-	CSI_DATA1_N	I, MIPI	MIPI CSI1differential data lane 1 negative.
8	GND	GND	Power	Ground.
9	CAM0_CSI_D2+	CSI_DATA2_P	I, MIPI	MIPI CSI1 differential data lane 2 positive.
10	CAM0_CSI_D2-	CSI_DATA2_N	I, MIPI	MIPI CSI1 differential data lane 2 negative.
11	CAM0_RST#	CAM0_RST(GPIO_C_7)	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal
12	CAM0_CSI_D3+	CSI_DATA3_P	I, MIPI	MIPI CSI1 differential data lane 3 positive.
13	CAM0_CSI_D3-	CSI_DATA3_N	I, MIPI	MIPI CSI1 differential data lane 3 negative.
14	GND	GND	Power	Ground.

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
15	CAM0_CSI_CLK+	CSI_CLOCK_P	I, MIPI	MIPI CSI1 differential Clock positive.
16	CAM0_CSI_CLK-	CSI_CLOCK_N	I, MIPI	MIPI CSI1 differential Clock negative.
17	GND	GND	Power	Ground.
18	CAM0_I2C_CLK	I2C_CAM_SCL	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI CSI1 Camera.
19	CAM0_I2C_DAT	I2C_CAM _SDA	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI CSI1 Camera.
20	CAM0_ENA#	NC	I, 1.8V CMOS/10K PU	Camera 0 Enable (active low). *Note: Optionally connected to CAM0_EN(GPIO_C_6)*
21	MCLK	CAM_MCK	I, 1.8V CMOS	Master Clock.
22	CAM1_ENA#	NC	I, 1.8V CMOS/10K PU	Camera 1 Enable (active low). *Note: Optionally connected to CAM1_EN(GPIO_B_1)*
23	CAM1_I2C_CLK	I2C_A_SCL	I, 1.8V OD	I2C clock Optional
24	CAM1_I2C_DAT	I2C_A_SDA	IO,1V8 OD	I2C Data Optional
25	GND	GND	Power	Ground.
26	CAM1_CSI_CLK+	CSI_2_CLOCK_P(VD_15)	I, MIPI	MIPI CSI2 differential Clock positive
27	CAM1_CSI_CLK-	CSI_2_CLOCK_N(VD_14)	I, MIPI	MIPI CSI2 differential Clock negative.
28	GND	GND	Power	Ground.
29	CAM1_CSI_D0+	CSI_2_DATA0_P(VD_17)	I, MIPI	MIPI CSI2 differential data lane 0 positive.
30	CAM1_CSI_D0-	CSI_2_DATA0_N(VD_16)	I, MIPI	MIPI CSI2 differential data lane 0 negative.
31	CAM1_RST#	CAM1_RST	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal *Note: Optionally connected to CAM1_RST(GPIO_B_2)*
32	CAM1_CSI_D1+	CSI_2_DATA1_P(VD_19)	I, MIPI	MIPI CSI2 differential data lane 1 positive.
33	CAM1_CSI_D1-	CSI_2_DATA1_N(VD_18)	I, MIPI	MIPI CSI2 differential data lane 1 negative.
34	GND	GND	Power	Ground.
35	CAM0_GPIO	USB_C_SW(GPIO_B_3)	I, 1.8V CMOS/10K PU	*Note: Optionally connected*

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
36	CAM1_GPIO	CAM1_GPIO(GPIO_B_4)	I, 1.8V CMOS/10K PU	*Note: Optionally connected*
37	CAM1_CSI_D2+	CSI_2_DATA2_P(VD_10)	I, MIPI	MIPI CSI2 differential data lane 2 positive.
38	CAM1_CSI_D2-	CSI_2_DATA2_N(VD_9)	I, MIPI	MIPI CSI2 differential data lane 2 negative.
39	CAM1_CSI_D3+	CSI_2_DATA3_P(VD_13)	I, MIPI	MIPI CSI2 differential data lane 3 positive.
40	CAM1_CSI_D3-	CSI_2_DATA3_N(VD_12)	I, MIPI	MIPI CSI2 differential data lane 3 negative.

2.9.2 I2S Audio Interface

The i.MX 8M Plus Pico ITX SBC supports Audio IN/OUT through SoC's SAI2 interface which can support I2S format. This four wire I2S signals from the SoC is connected to I2S Audio Codec "SGTL5000" to support CTIA configuration Headphone Stereo output and Mono Mic input through Single 3.5mm audio Jack (J9).

The Audio IN/OUT Jack is physically located at the top of the board as shown below.

Figure 15: Audio IN/OUT Jack

The i.MX 8M Plus Pico ITX SBC supports 3W Audio Amplifier. The LINEOUT signals from "SGTL5000" are connected to an Audio Amplifier. The Output signals from the Amplifier is connected to two Speaker Headers (J10) and (J11). The Speaker Headers is physically located at the top of the board as shown below**.**

Number of Pins: 2

Connector Part :10114829-10102LF from Molex

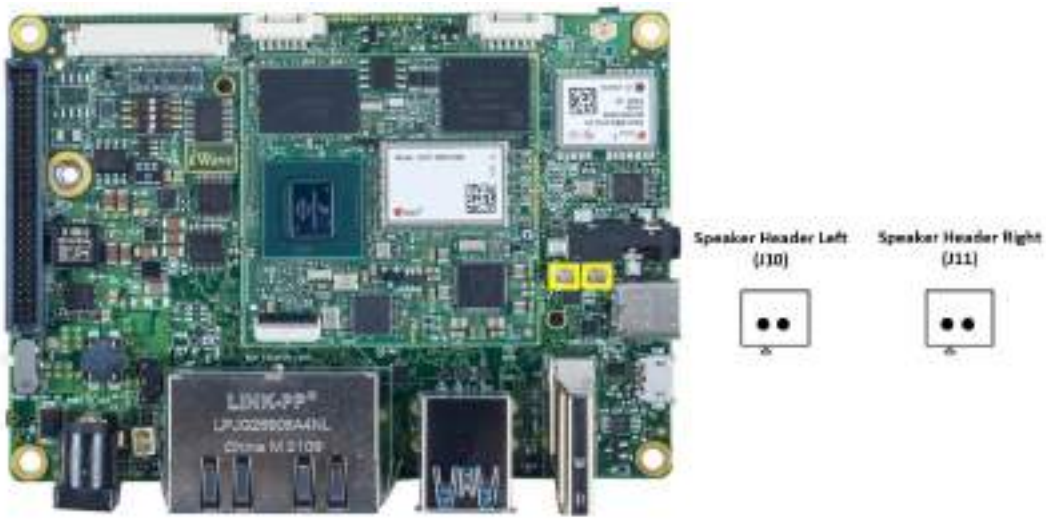

Figure 16: Speaker Headers

2.9.3 HDMI Interface

The i.MX 8M Plus Pico ITX SBC supports HDMI audio/video out through i.MX 8M Plus SoC's HDMI 2.0a interface. The HDMI TX PHY of the i.MX 8M Plus SoC supports video pixel rated from 25MHz up to 297MHz. This HDMI output connector (J15) is physically located on top of the board as shown below.

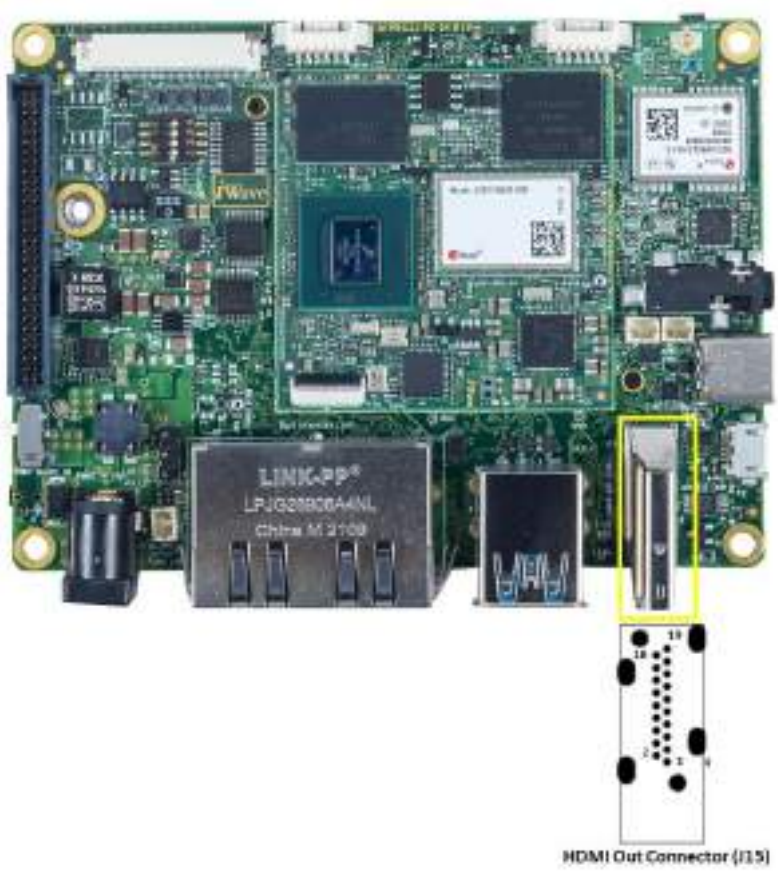

Figure 17: HDMI Connector

2.9.4 LVDS Interface

The i.MX 8M Plus SoC supports two LVDS display channels LVDS0 and LVDS1. Each channel has one clock pair and four data pairs. The LVDS0 of the SoC is connected to a 4 lane LVDS display connector and LVDS1 is connected to the expansion connector. The LVDS Display Connector(J4) and USB Touch Header (J3) are located at top side of the board as shown in the below image.

Number of Pins : 40

Connector Part : 541044033 from Molex

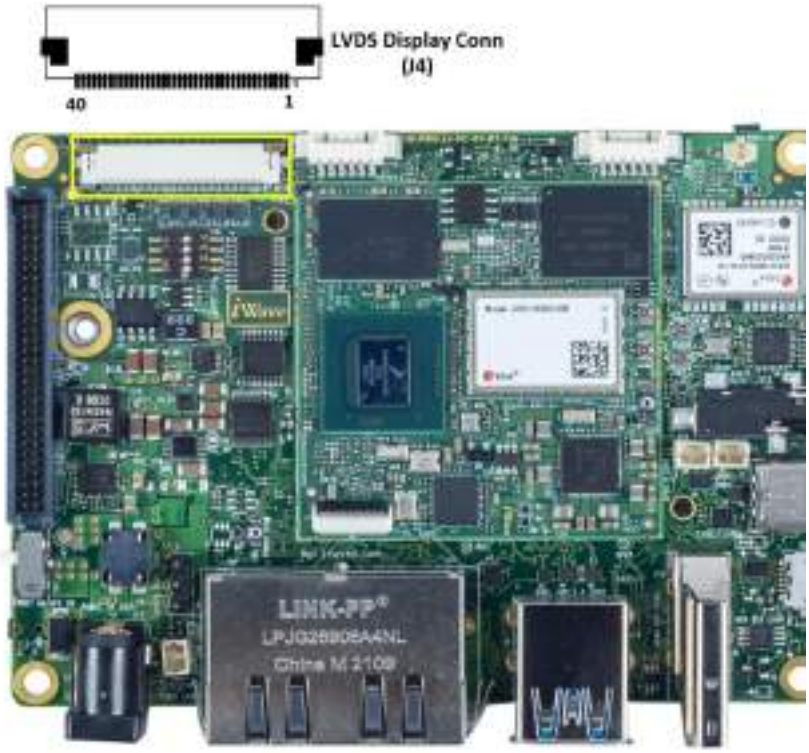

Figure 18: 40 pin LVDS Display Connector

Table 9: 40 Pin 10.1" LVDS Display Pinout

Pin No.	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	NC1	-	-	-	NC
2	VDD1	VCC_3V3	-	Power	3.3V Supply Voltage
3	VDD2	VCC_3V3	-	Power	3.3V Supply Voltage
4	NC2	-	-	-	NC
5	NC3	-	-	-	NC
6	NC4	-	-	-	NC
7	NC5	-	-	-	NC
8	LV0N-	LVDS_CH0_N	LVDS0_D0_N/E28	O, LVDS	LVDS0 differential data Lane 0 negative

Pin No.	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
9	LV0N+	LVDS_CH0_P	LVDS0_D0_P/D29	O, LVDS	LVDS0 differential data lane 0 positive
10	GND1	GND	-	Power	Ground
11	LV1N-	LVDS_CH1_N	LVDS0_D1_N/F28	O, LVDS	LVDS0 differential data Lane 1 negative
12	LV1N+	LVDS_CH1_P	LVDS0_D1_P/E29	O, LVDS	LVDS0 differential data lane 1 positive
13	GND2	GND	-	Power	Ground
14	LV2N-	LVDS_CH2_N	LVDS0_D2_N/H28	O, LVDS	LVDS0 differential data Lane 2 negative
15	LV2N+	LVDS_CH2_P	LVDS0_D2_P/G29	O, LVDS	LVDS0 differential data lane 2 positive
16	GND3	GND	-	Power	Ground
17	LVCLK-	LVDS_CLK_N	LVDS0_CLK_N/G28	O, LVDS	LVDS0 differential Clock negative
18	LVCLK+	LVDS_CLK_P	LVDS0_CLK_P/F29	O, LVDS	LVDS0 differential Clock positive
19	GND4	GND	-	Power	Ground
20	LV3N-	LVDS_CH3_N	LVDS0_D3_N/J28	O, LVDS	LVDS0 differential data Lane 3 negative
21	LV3N+	LVDS_CH3_P	LVDS0_D3_P/H29	O, LVDS	LVDS0 differential data lane 3 positive
22	GND5	GND	-	Power	Ground
23	LED_GND 1	GND	-	Power	Ground
24	LED_GND 2	GND	-	Power	Ground
25	LED_GND 3	GND	-	Power	Ground
26	NC6	-	-	-	NC
27	LED_PW M	PWM2_OUT(SAI5_ RXD0)	SAI5_RXD0/ AE16	O, 3.3V	LCD Back Light Brightness control PWM
28	LED_EN	LCD0_BKLT_EN(NA ND_DATA01_GPIO 3_7)	NAND_DATA01/ L25	O, 3.3V	LCD Backlight Enable
29	NC7	-	-	-	NC
30	NC8	-	-	-	NC
31	LED_VCC1	VCC_12V_LVDS	-	Power	12V Supply Voltage
32	LED_VCC2	VCC_12V_LVDS	-	Power	12V Supply Voltage
33	LED_VCC3	VCC_12V_LVDS	-	Power	12V Supply Voltage
34	NC9	-	-	-	NC
35	BIST	-	-	-	NC
36	NC10	-	-	-	NC

Pin No.	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
37	NC11	-	-	-	NC
38	NC12	-	-	-	NC
39	NC13	-	-	-	NC
40	NC14	-	-	-	NC

2.9.5 USB Touch Connector

The i.MX 8M Plus Pico ITX SBC supports a 6 Pin USB connector (J3). This connector can be used as general- purpose connector for USB interface.

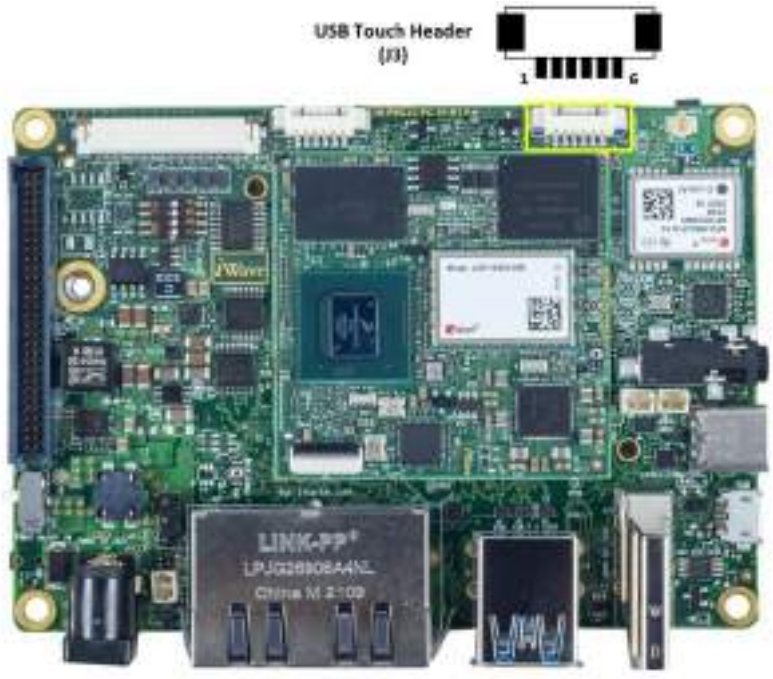

Figure 19: USB Touch Connector

Number of Pins: 6

Connector Part :532610671 from Molex

Table 10: LVDS Display Touch Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	1	VBUS_HOST_TP	5V, Power	Supply Voltage.
2	2	USB_HUB3OUT_DM	IO, USB	Differential USB Negative.
3	3	USB_HUB3OUT_DP	IO, USB	Differential USB Positive.
4	4	NC	-	NC. USB_ID pin is available optionally.
5	5	GND	Power	Ground.
6	6	NC	-	NC. USB_B_VBUS is available optionally.

2.9.6 4-lane MIPI DSI Display Connector

The i.MX 8M Plus SoC supports one 4-lane MIPI DSI. The D-PHY provides a synchronous connection between Master and Slave with clock signal originating at the Master and terminating at the Slave. The main operation modes are HS mode (High Speed Mode) and LP mode (Low Power Mode). The D-PHY is v1.2 spec compatible.

The i.MX 8M Plus Pico ITX SBC supports 4-lane MIPI DSI Display and optionally supports 2-lane MIPI DSI.

Number of Pins: 39

Connector Part : 5025983993 from Molex.

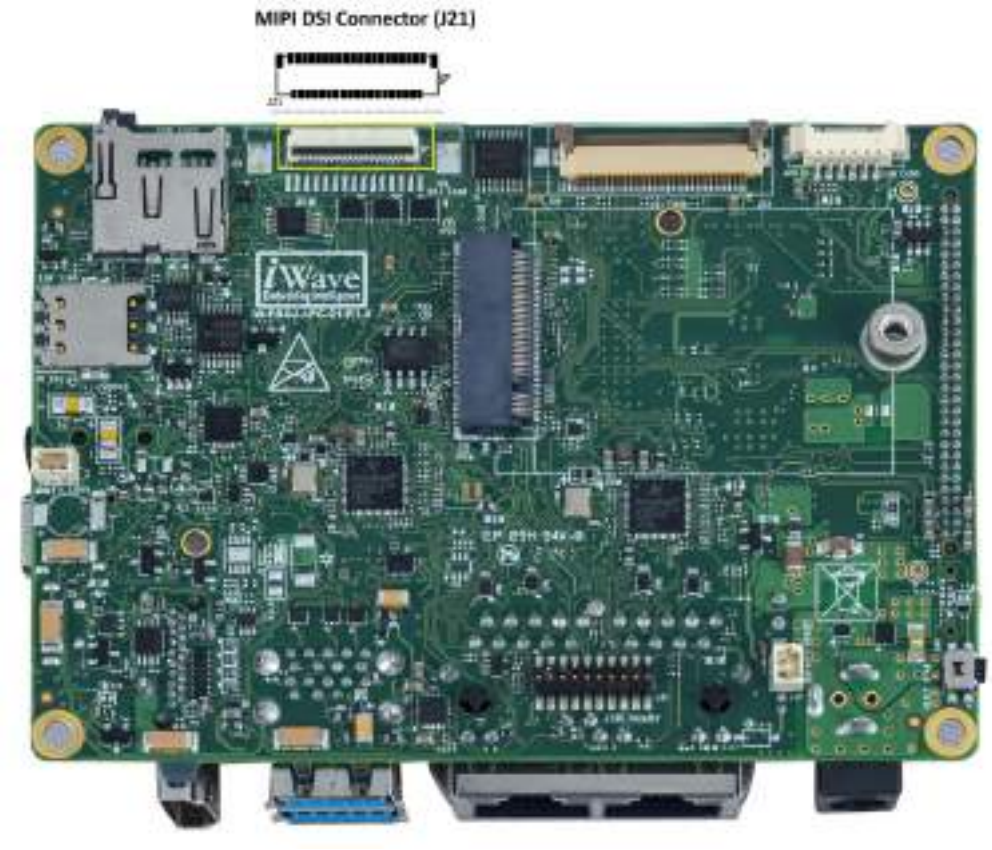

Figure 20: 4-lane MIPI DSI Connector

Table 11: 4-Lane MIPI DSI Connector Pinouts

Pin No	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	GND	-	Power	Ground.
2	GND	GND	-	Power	Ground.
3	GND	GND	-	Power	Ground.
4	VBAT	VCC_3V3_TFT0	-	Power	3.3V Supply Voltage.
5	VBAT	VCC_3V3_TFT0	-	Power	3.3V Supply Voltage.
6	VBAT	VCC_3V3_TFT0	-	Power	3.3V Supply Voltage.
7	VBAT	VCC_3V3_TFT0	-	Power	3.3V Supply Voltage.
8	VBAT	VCC_3V3_TFT0	-	Power	3.3V Supply Voltage.
9	GND	GND	-	Power	Ground.

Pin No	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
10	OTPV	NC	-	-	NC.
11	NC1	NC	-	-	NC.
12	GND	GND	-	Power	Ground.
13	D3P	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P/ A20	O, MIPI	MIPI DSI differential data lane 3 positive
14	D3N	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N/ B20	O, MIPI	MIPI DSI differential data lane 3 negative
15	GND	GND	-	Power	Ground.
16	D0P	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P/ A16	O, MIPI	MIPI DSI differential data lane 0 positive
17	D0N	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N/ B16	O, MIPI	MIPI DSI differential data lane 0 negative
18	GND	GND	-	Power	Ground.
19	DKP	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P /A18	O, MIPI	MIPI DSI differential Clock positive
20	DKN	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N /B18	O, MIPI	MIPI DSI differential Clock negative
21	GND	GND	-	Power	Ground.
22	D1P	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P/ A17	O, MIPI	MIPI DSI differential data lane 1 positive
23	D1N	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N/ B17	O, MIPI	MIPI DSI differential data lane 1 negative
24	GND	GND	-	Power	Ground.
25	D2P	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P/ A19	O, MIPI	MIPI DSI differential data lane 2 positive
26	D2N	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N/ B19	O, MIPI	MIPI DSI differential data lane 2 negative
27	GND	GND	-	Power	Ground.
28	RESX	OSM_GPIO_B_5(GPIO1_IO6)	GPIO1_IO06/A3	O, 1,8V CMOS /10K PU	*Display reset. Active low. OSM_GPIO_A_1(SAI1_TXD 7_GPIO4_19) is optionally connected.*
29	VDDIO	VCC_1V8	-	O, 1.8V Power	1.8V Supply voltage for Display IO Circuit.
30	VCI	VCC_3V3_TFT0	-	O, 3.3V Power	3.3V Supply voltage for Display Circuit.
31	NC2	NC	-	NA	NA.
32	GND	GND	-	Power	Ground.
33	TP_AVDD_3P3V	VCC_3V3_TFT0	-	O, 3.3V Power	3.3V Supply voltage for Touch driver Circuit.
34	TP_DVDD_1P8V	VCC_1V8	-	O, 1.8V Power	1.8V Supply voltage for Touch IO Circuit.
35	TP_SDA	I2C2_SDA	I2C2_SDA/AE8	IO, 1.8V CMOS, 4.7K PU	I2C Data for Capacitive Touch
36	TP_SCL	I2C2_SCL	I2C2_SCL/AH6	O, 1.8V CMOS, 4.7K PU	I2C Clock for Capacitive Touch
37	TP_RESET	OSM_GPIO_A_1(SAI1_TXD7_GPIO4_19	SAI1_TXD7/AJ13	O, 1.8V CMOS, 10K PU	RESET for Capacitive Touch

Pin No	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
38	TP_INT	OSM_GPIO_A_2(SAI1_RXFS_GPIO4_0)	SAI1_RXFS/AJ9	I, 1.8V CMOS	Interrupt from Capacitive Touch
39	GND	GND	-	Power	Ground.

2.9.7 2-Lane MIPI DSI Display Connector (Optional)

The i.MX 8M Plus Pico ITX SBC optionally supports 2-lane MIPI DSI Display.

Number of Pins: 15

Connector Part : 1-84952-5 from TE Connectivity AMP Connectors

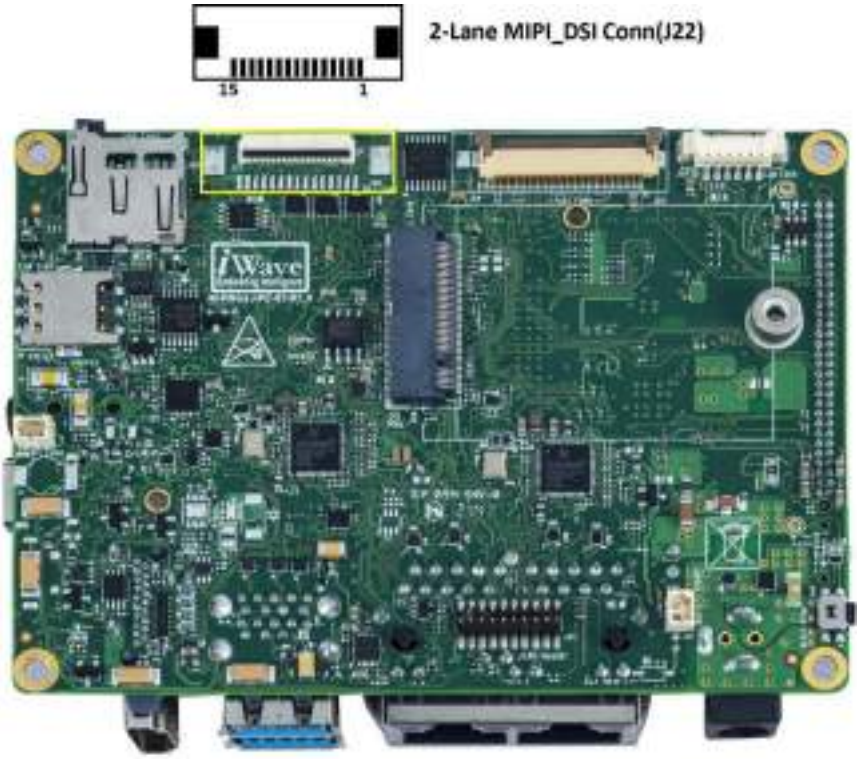

Figure 21: 2-lane MIPI DSI Connector (Optional)

Table 12: 2-lane MIPI DSI Connector Pinouts

Pin No	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND1	GND	-	Power	Ground.
2	DATA1-	MIPI_DSI_DATA1_N	MIPI_DSI1_D1_N/B17	O, MIPI	MIPI DSI differential data lane 1negative
3	DATA1+	MIPI_DSI_DATA1_P	MIPI_DSI1_D1_P/A17	O, MIPI	MIPI DSI differential data lane 1 positive
4	GND2	GND	-	Power	Ground.
5	CLK-	MIPI_DSI_CLK_N	MIPI_DSI1_CLK_N/B18	O, MIPI	MIPI DSI differential Clock negative

Pin No	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
6	CLK+	MIPI_DSI_CLK_P	MIPI_DSI1_CLK_P/A18	O, MIPI	MIPI DSI differential Clock positive
7	GND3	GND	-	Power	Ground.
8	DATA0-	MIPI_DSI_DATA0_N	MIPI_DSI1_D0_N/B16	O, MIPI	MIPI DSI differential data lane 0negative
9	DATA0+	MIPI_DSI_DATA0_P	MIPI_DSI1_D0_P/A16	O, MIPI	MIPI DSI differential data lane 0 positive
10	GND4	GND	-	Power	Ground.
11	SCL	I2C1_SCL	I2C1_SCL/AC8	I,3.3V CMOS/4.7K PU	I2C Clock.
12	SDA	I2C1_SDA	I2C1_SDA/AH7	IO,3,3V CMOS/4.7K PU	I2C Data
13	GND5	GND	-	Power	Ground.
14	VCC1	VCC_3V3	-	Power	3.3V Supply Voltage.
15	VCC2	VCC_3V3	-	Power	3.3V Supply Voltage.

2.12 M.2 Key B Connector

The i.MX 8M Plus Pico ITX SBC supports M.2 key-B socket. M.2 key-B socket is the Next Generation Form Factor (NGFF) which is designed to support multiple modules and make the M.2 more suitable in application like solid-state storage, WWAN. The M.2 Key B Connector supports PCIe ×1, USB 2.0, UIM, I2C and SMBus. The M.2 Key-B Connector (J28) is placed at the bottom side of the board.

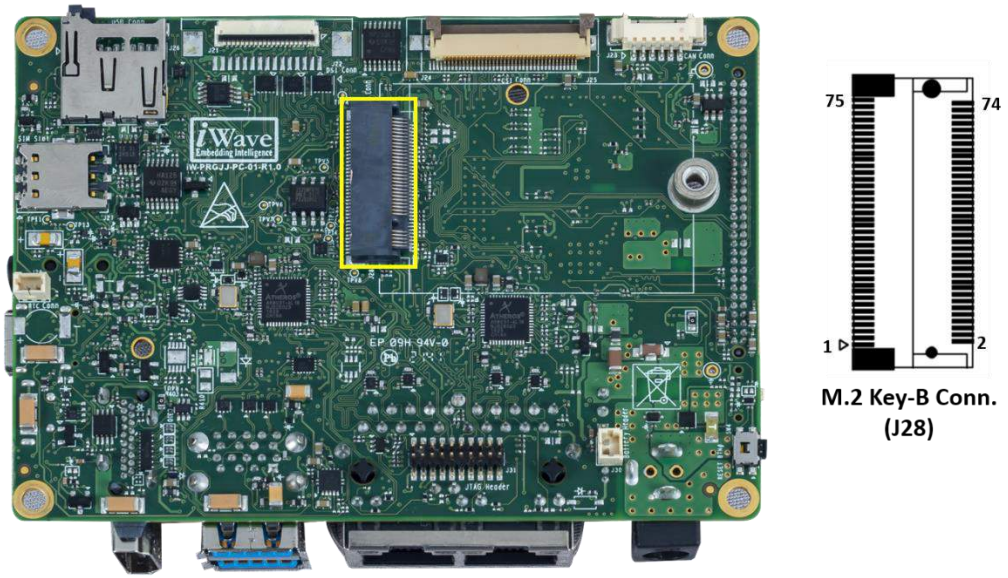

Figure 22: M.2 Key B Connector

Table 13: M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	OSM_GPIO_B_1(SAI1_RXD1_GPIO4_3) (	O, 1.8V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	USB_HUB2OUT_DP	IO, USB	USB2.0 PortA Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	OSM_GPIO_B_7(GPIO1_IO9)	O, 3.3V CMOS 10K PU	M.2 Wireless Disable Signal.
9	USB_D-	USB_HUB2OUT_DM	IO, USB	USB2.0 PortA Data Minus.
10	GPIO9(LED1#/DAS_DSS#) (I)(0/3.3V)	M.2_LED	O, 3.3V CMOS	Provide status indicators via LED.
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	NC	NC	NC.
21	CONFIG_0	M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX)(I/O)(0/1.8V)	NC	NC	NC.
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O)(0/1.8V)	NC	NC	NC.
24	GPIO7(AUDIO2/I2S_TX)(I/O)(0/1.8V)	NC	NC	NC.
25	DPR (O) (0/1.8V)	OSM_GPIO_C_6(GPIO1_IO15)	O, 1.8V CMOS 10K PU	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V))(I/O)(0/1.8V)	NC	NC	NC.
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	NC	NC	NC.
29	PERN1/USB30_RX-/SSIC_RX-	NC	NC	NC.
30	UIM-RESET (I)	M2_UIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	NC	NC	NC.
32	UIM-CLK (I)	M2_UIM_CLK	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	M2_UIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NC	NC.
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NC	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	I2C2_SCL	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	PCIE_RXN_N	I,PCIe	PCIe Port 0 Receive Lane Negative.
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	I2C2_SDA	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	PCIE_RXN_P	I,PCIe	PCIe Port 0 Receive Lane Positive.
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	GPIO_PCIe_SM_ALERT#(SAI3_MCLK_GPIO5_02)	IO, 1.8V CMOS 10K PU	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2) (I/O)(0/1.8V)	OSM_GPIO_C_0(GPIO1_IO7)	IO, 1.8V CMOS	General Purpose Input Output.
47	PETN0/SATA_A-	PCIE_TXN_N	O,PCIe	PCIe Port 0 Transmit Lane Negative.
48	GPIO4(TX_BLK/GNSS_1/UIM_PWR2)(I/O)(0/1.8V)	NC	NC	NC.
49	PETP0/SATA_A+	PCIE_TXN_P	O,PCIe	PCIe Port 0 Transmit Lane Positive.
50	PERST# (O)(0/3.3V)	NC	O, 3.3V CMOS 10K PU	PCIe Reset Signal. *GPIO_PCIE_RST(GPIO1_IO12) is optionally connected*
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	NC	3.3V CMOS 10K PU	M.2 Clock Request Pin
53	REFCLKN	PCIE_REFCLK_DM	O,PCIe	PCIe Channel-A Clock Negative.
54	PEWAKE# (I/O)(0/3.3V)	GPIO_PCIe_Wake(GPIO1_IO14)	O, 3.3V CMOS 10K PU	PCIe Wake Signal.
55	REFCLKP	PCIE_REFCLK_DP	O,PCIe	PCIe Channel-A Clock Positive.
56	MFG_DATA	I2C2_SDA	IO, 1.8V CMOS	NC. *Optionally I2C2_SDA is connected.*
57	GND	GND	Power	Ground.
58	MFG_CLOCK	I2C2_SCL	O, 1.8V CMOS	NC. *Optionally I2C2_SCL is connected.*
59	ANTCTL0 (I)(0/1.8 V)	NC	NC	NC.
60	COEX3 (I/O)(0/1.8V)	NC	NC	NC.
61	ANTCTL1 (I)(0/1.8 V)	NC	NC	NC.
62	COEX_TXD (O)(0/1.8V)	NC	NC	NC.
63	ANTCTL2 (I)(0/1.8 V)	NC	NC	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
64	COEX_RXD (I)(0/1.8V)	NC	NC	NC.
65	ANTCTL3 (I)(0/1.8 V)	NC	NC	NC.
66	SIM_DETECT (I)	NC	NC	NC
67	RESET# (O)(0/1.8V)	OSM_GPIO_C_7(GPIO1_IO10)	O, 1.8V 10K PU	*M.2 Reset Signal OSM_GPIO_C_7(GPIO1_IO10) is Optionally available.*
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK	I, 32.768kHz Clock Supply	*Note: Optionally connected 32.768kHz Clock output*
69	CONFIG_1	M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

Below are the steps for Inserting an M.2 Key B Module to the i.MX 8M Plus Pico ITX SBC

Step 1: Move the Module against housing Chamber.

Step 2: Rotate the Module to 25 Degree and insert until the bottom of the module surface reaches the ramp.

Step 3: Rotate the Module to horizontal Position by hand

Step 4: Fix the module with M3 x4 Screw

Figure 23: M.2 Module Insertion Guide

The i.MX 8M Plus Pico ITX SBC supports a Nano SIM connector to support the WWAN M.2 Modules. The Nano SIM connector (J27) is physically located on the bottom of the board.

Figure 24: Nano SIM Connector

2.13 Expansion Connector

The interfaces which are available at 60 Pin Expansion connector are explained in the following section. This Expansion Connector (J6) is physically located at the top of the SBC as shown below.

Number of Pins : 60

Connector Part : PTSHS-530-D-02-GT-AP-LF from MLE

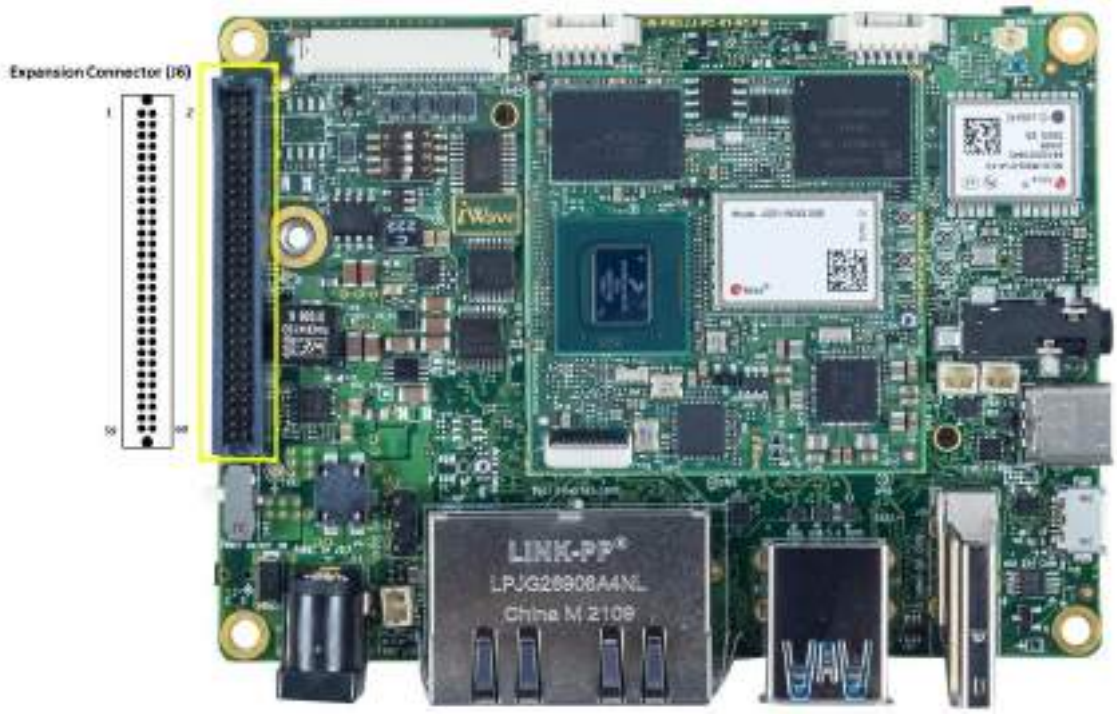

Figure 25: Expansion Connector

Table 14: Expansion Connector Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	EARC_P_UTIL	EARC_P_UTIL/AJ23	I, 1.8V	HDMI EARC Utility pin
2	LVDS_B_LANE3_N	LVDS1_D3_N/D28	O, LVDS	LVDS Channel 3 negative
3	EARC_N_HPD	EARC_N_HPD/ AH22	I, 1.8V	EARC HPD
4	LVDS_B_LANE3_P	LVDS1_D3_P/C29	O, LVDS	LVDS Channel 3 positive
5	GND	-	Power	Ground
6	GND	-	Power	Ground
7	UART_B_RX	UART1_RXD/AD6	I, 1.8V CMOS	Optional By default, connected to Wi-Fi BT module
8	LVDS_B_LANE1_N	LVDS1_D1_N /B27	O, LVDS	LVDS Channel 1 negative
9	UART_B_TX	UART1_TXD/AJ3	O, 1.8V CMOS	Optional By default, connected to Wi-Fi BT module
10	LVDS_B_LANE1_P	LVDS1_D1_P/A27	O, LVDS	LVDS Channel 1 positive

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
11	UART_B_RTS	UART3_RXD/ AE6	I, LVDS	Optional By default, connected to Wi-Fi BT module
12	GND	-	Power	Ground
13	UART_B_CTS	UART3_TXD /AJ4	O, LVDS	Optional By default, connected to Wi-Fi BT module
14	LVDS_B_LANE0_N	LVDS1_D0_N/B26	O, LVDS	LVDS Channel 0 negative
15	GND	-	Power	Ground
16	LVDS_B_LANE0_P	LVDS1_D0_P/A26	O, LVDS	LVDS Channel 0 Positive
17	SPI_B_SDI	I2C4_SCL/AF8	I CMOS	SPI B Serial Data Input
18	GND	-	Power	Ground
19	SPI_B_SD0	ECSPI2_MOSI/AJ21	O CMOS	SPI B Serial Data Output
20	LVDS_B_LANE2_P	LVDS1_D2_P/B29	O, LVDS	LVDS Channel 2 positive
21	SPI_B_CS#	ECSPI2_SS0/AJ22	O CMOS	SPI B Master Chip Select
22	LVDS_B_LANE2_N	LVDS1_D2_N/C28	O, LVDS	LVDS Channel 2 negative
23	SPI_B_SCK	ECSPI2_SCLK /AH21	O CMOS 1.8V	SPI B Serial Data Clock
24	GND	-	Power	Ground
25	GND	-	Power	Ground
26	LVDS_B_CLK_P	LVDS1_CLK_P /A28	O, LVDS	LVDS Channel 0 clock positive
27	SDIO_B_CD#	SD1_RESET_B/W25	I OD CMOS	SDIO B Card Detect
28	LVDS_B_CLK_N	LVDS1_CLK_N /B28	O, LVDS	LVDS Channel 0 clock negative
29	SDIO_B_WP	SD1_STROBE/W26	I OD CMOS	SDIO B Write Protect.
30	GND	-	Power	Ground
31	LVDS_I2C_CLK	SPDIF_TX/AE18	I,1.8V CMOS/4.7K PU	I2C Clock.
32	SDIO_B_CLK	SD1_CLK /W28	IO, 1.8V	SDIO B Clock
33	LVDS_I2C_DAT	SPDIF_RX/AD18	IO, 1.8V CMOS/4.7K PU	I2C Data
34	SDIO_B_CMD	SD1_CMD/W29	I/O CMOS	SDIO B Command/Response.
35	LVDS_VDD_EN	NAND_DATA02 /L24	O CMOS	LVDS channel power enable, active high
36	SDIO_B_D0	SD1_DATA0/ Y29	I/O CMOS	SDIO B Data lines
37	LVDS_BL_PWM	SAI5_RXD0/AE16	IO, 1.8V	Optional By default, used as PWM for LVDS display
38	SDIO_B_D1	SD1_DATA1/Y28	O, 1.8V	Optional By default, connected to WI-FI BT module
39	LVDS_BL_EN	NAND_DATA01/L25	I, 1.8V	LVDS back light Enable
40	SDIO_B_D2	SD1_DATA2/V29	I, 1.8V	Optional

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
				By default, connected to WI-FI BT module
41	PWM_0	I2C4_SDA/AD8	I, 1.8V	PWM signal
42	SDIO_B_D3	SD1_DATA3/V28	IO, 1.8V	Optional By default, connected to WI-FI BT module
43	CAN_B_TX	SAI5_RXD3/AE14	I, 1.8V	CAN TX
44	SDIO_B_D4	SD1_DATA4/U26	IO,1.8V	Optional By default, connected to WI-FI BT module
45	CAN_B_RX	SAI5_MCLK/AF14	O,1.8V	CAN RX
46	SDIO_B_D5	SD1_DATA5/AA29	IO,1.8V	Optional By default, connected to WI-FI BT module
47	UARTD_RX	-	NC	NC
48	SDIO_B_D6	SD1_DATA6/AA28	IO,1.8V	Optional By default, connected to WI-FI BT module
49	UARTD_TX	-	NC	NC
50	SDIO_B_D7	SD1_DATA7/U25	IO,1.8V	Optional By default, connected to WI-FI BT module
51	GND	-	Power	Ground
52	SDIO_B_PWR_EN	NC	NC	NC
53	VCC_5V	-	Power	5V Supply Voltage
54	SDIO_B_IOPWR	-	Power	Supply Voltage
55	VCC_3V3	-	Power	3.3V Supply Voltage
56	VCC_1V8	-	Power	1.8V Supply Voltage
57	VCC_3V3	-	Power	3.3V Supply voltage
58	VCC_12V	-	Power	12V Supply Voltage
59	PIN59	-	GND	Connected to ground
60	GND	-	Power	Ground

*Note: Refer GPIO Column under **"i.MX 8M plus Pin Multiplexing on Expansion Connector** for details on GPIO options available from Expansion connector.*

2.14 Other Features

2.14.1 Fan Header

The i.MX 8M Plus Pico ITX SBC supports a Fan Header to connect a cooling Fan if required. This Fan Header (J18) is physically located at the top of the board as shown below.

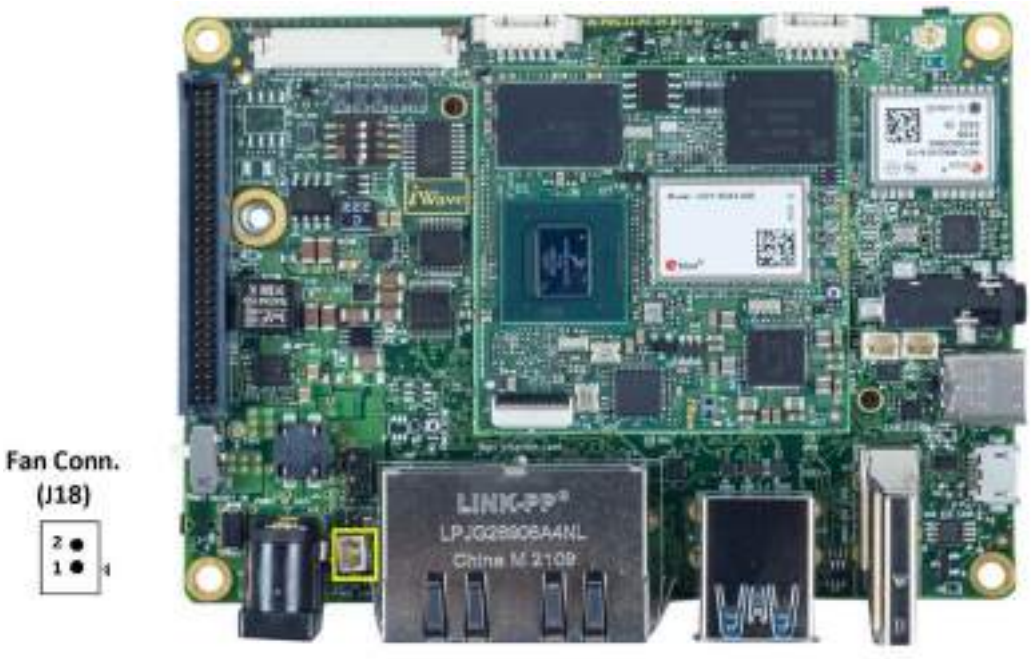

Figure 26: Fan Connector

Number of Pins : 2

Connector Part :10114829-10102LF from Amphenol ICC (FCI)

Table 15: Fan Connector Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN. *Note: Optionally connected to 12V Power.*
2	GND	Power	Ground.

Note: Contact iWave support team if 12V Power Support is required for FAN Header.

2.14.2 RTC Controller with RTC Battery Header

The i.MX 8M Plus Pico ITX SBC supports external RTC Controller “PCF85263” for Real time clock support. This external RTC Controller IC (U9) is connected to i.MX 8M Plus SoC through I2C3 Interface and operates at 1.8V voltage level.

The i.MX 8M Plus Pico ITX SBC supports external RTC cell. The SBC supports 2pin connector for backup battery or coin cell connection. The 2pin RTC (J29) battery connector is physically located on bottom side of the SBC as shown below.

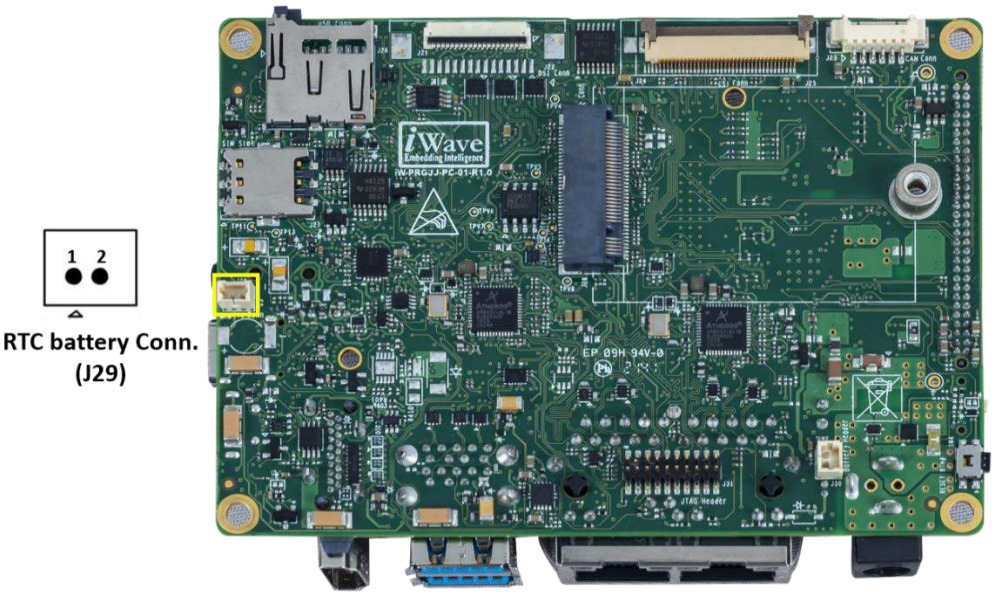

Figure 27: RTC Battery Connector

Number of Pins : 2

Connector Part : 10114829-10102LF from Amphenol ICC (FCI)

Table 16: RTC Battery Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VRTC_3V0	I, Power	+3V Power Input to RTC Controller
2	GND	Power	Ground.

2.14.3 JTAG Interface

The i.MX 8M Plus Pico ITX SBC supports JTAG interface for CPU debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security. JTAG Header (J31) is physically located on bottom side of the SBC.

Number of Pins - 20

Connector Part - 62132021021 from Wruth Electronics.

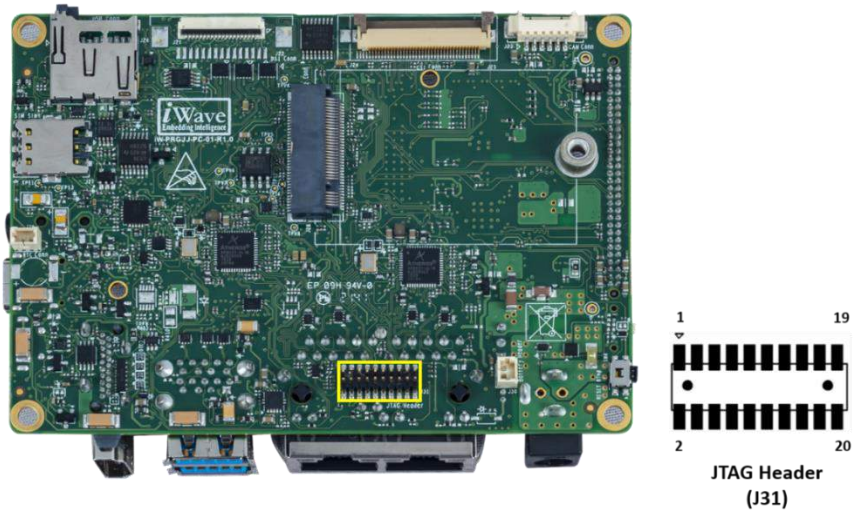

Figure 28: JTAG Header

Table 17: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_1V8	O, 1.8V Power	VTREF Voltage Reference.
2	VCC_1V8	O, 1.8V Power	Supply Voltage.
3	JTAG_TRSTB	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	Power	Ground.
5	JTAG_TDI	I, 3.3V CMOS	JTAG test data input.
6	GND	Power	Ground.
7	JTAG_TMS	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
8	GND	Power	Ground.
9	JTAG_TCK	I, 3.3V CMOS/ 10K PD	JTAG test Clock.
10	GND	Power	Ground.
11	-	-	10K pull down is provided.
12	GND	Power	Ground.
13	JTAG_TDO	O, 3.3V CMOS	JTAG test data output.
14	GND	Power	Ground.
15	JTAG_RESETB	I, 3.3V CMOS/ 10K PU	Reset input.
16	GND	Power	Ground.
17	-	-	10K pull up is provided.
18	GND	Power	Ground.
19	-	-	10K pull down is provided.
20	GND	Power	Ground.

2.14.4 Power ON/OFF Switch

The i.MX 8M Plus Pico ITX SBC has power ON/OFF switch (SW3) to control the Main power Input ON/OFF functionality. The Power ON/OFF switch is physically located at the top of the board as shown below.

Figure 29: Power ON/OFF Switch

2.14.5 Reset Switch

The i.MX 8M Plus Pico ITX SBC Support Push Button Switch (SW4) to reset the i.MX 8M Plus CPU. Reset signal is directly connected from reset push button switch. This Reset push button Switch (SW4) is physically located at the bottom of the board as shown below.

Figure 30: Reset Switch

2.14.6 CPU ON/OFF Switch

The i.MX 8M Plus Pico ITX SBC supports Push button Switch (SW2) for ON/OFF of the i.MX 8M Plus Pico ITX SBC. ON/OFF is directly connected from ON/OFF push button Switch. This ON/OFF push button Switch (SW2) is physically located at the bottom of the board as shown below.

Figure 31: CPU ON/OFF Switch

2.15 i.MX 8M Plus Pin Multiplexing on Expansion Connector

The i.MX 8M Plus SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M plus SOC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8M plus SoC pin connections to the Expansion Connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M plus Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in SBC for iWave's BSP reusability.

Table 18: i.MX 8M Plus CPU IOMUX for Expansion Connector interfaces

Interface/ Function	Exp. Conn. Pin Number	i.MX 8M Plus CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
ECSPI2	17	AF8	I2C4_SCL	PWM2_OUT	PCIE_CLKREQ_B	ECSPI2_MISO		GPIO5_IO20	
	19	AJ21	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI7_TX_DATA0		GPIO5_IO11	
	21	AJ22	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA		CCM_CLKO2	GPIO5_IO13	
	23	AH21	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TX_BCLK		GPIO5_IO10	
PWM	41	AD8	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO21	
SDIO	27	W25	USDHC1_RESET_B	ENET1_INPUT=ENET1_TX_CLK, OUTPUT=CCM_ENET_REF_CLK_ROOT		I2C3_SCL	UART3_RTS_B	GPIO2_IO10	
	29	W26	USDHC1_STROBE			I2C3_SDA	UART3_CTS_B	GPIO2_IO11	
	32	W28	USDHC1_CLK	ENET1_MDC		I2C5_SCL	UART1_TX	GPIO2_IO0	
	34	W29	USDHC1_CMD	ENET1_MDIO		I2C5_SDA	UART1_RX	GPIO2_IO1	
	36	Y29	USDHC1_DATA0	ENET1_RGMII_TD1		I2C6_SCL	UART1_RTS_B	GPIO2_IO2	
	38	Y28	USDHC1_DATA1	ENET1_RGMII_TD0		I2C6_SDA	UART1_CTS_B	GPIO2_IO3	
	40	V29	USDHC1_DATA2	ENET1_RGMII_RD0		I2C4_SCL	UART2_TX	GPIO2_IO4	
	42	V28	USDHC1_DATA3	ENET1_RGMII_RD1		I2C4_SDA	UART2_RX	GPIO2_IO5	

Interface/ Function	Exp. Conn. Pin Number	i.MX 8M Plus CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	44	U26	USDHC1_DATA4	ENET1_RGMII_TX_CTL		I2C1_SCL	UART2_RTS_B	GPIO2_IO6	
	46	AA29	USDHC1_DATA5	ENET1_TX_ER		I2C1_SDA	UART2_CTS_B	GPIO2_IO7	
	48	AA28	USDHC1_DATA6	ENET1_RGMII_RX_CTL		I2C2_SCL	UART3_TX	GPIO2_IO8	
	50	U25	USDHC1_DATA7	ENET1_RX_ER		I2C2_SDA	UART3_RX	GPIO2_IO9	
UART	7	AD6	UART1_RX	ECSPI3_SCLK				GPIO5_IO22	
	9	AJ3	UART1_TX	ECSPI3_MOSI				GPIO5_IO23	
	11	AJ4	UART3_TX	UART1_RTS_B	USDHC3_VSELECT	GPT1_CLK	CAN2_RX	GPIO5_IO27	
	13	AE6	UART3_RX	UART1_CTS_B	USDHC3_RESET_B	GPT1_CAPTURE2	CAN2_TX	GPIO5_IO26	
LVDS 1	2	D28	LVDS1_TX3_N						
	4	C29	LVDS1_TX3_P						
	8	B27	LVDS1_TX1_N						
	10	A27	LVDS1_TX1_P						
	14	B26	LVDS1_TX0_N						
	16	A26	LVDS1_TX0_P						
	20	B29	LVDS1_TX2_P						
	22	C28	LVDS1_TX2_N						
	26	A28	LVDS1_CLK_P						
	28	B28	LVDS1_CLK_N						
	31	AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	FLEXCAN1_TX	GPIO5_IO3	
	33	AD18	SPDIF1_IN	PWM2_OUT	I2C5_SDA	GPT1_COMPARE2	FLEXCAN1_RX	GPIO5_IO4	

Interface/ Function	Exp. Conn. Pin Number	i.MX 8M Plus CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	35	L24	NAND_DATA02	QSPI_A_DATA2	USDHC3_CD_B	UART4_CTS_B		GPIO3_IO8	CORESIGHT_ TRACE06
	37	AE16	SAI5_RX_DATA0	SAI1_TX_DATA2	PWM2_OUT	I2C5_SCL	PDM_BIT_STR EAM0	GPIO3_IO21	
	39	L25	NAND_DATA01	QSPI_A_DATA1	SAI3_TX_SYNC	ISP_PRELIGHT_TRIG_ 0	UART4_TX	GPIO3_IO7	CORESIGHT_ TRACE05
EARC	1	AJ23	EARC_AUX						
	3	AH22	EARC_N_HPD						
CAN	43	AE14	SAI5_RX_DATA3	SAI1_TX_DATA5	SAI1_TX_SYNC	SAI5_TX_DATA0	PDM_BIT_STR EAM3	GPIO3_IO24	FLEXCAN2_X
	45	AF14	SAI5_MCLK	SAI1_TX_BCLK	PWM1_OUT	I2C5_SDA		GPIO3_IO25	FLEXCAN2_X

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Plus Pico ITX SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The i.MX 8M Plus Pico ITX SBC supports 7V to 24V external power and uses on board voltage regulators for internal power management. By default, it supports to work with 12V power input. 12V power input from an external power supply is connected to the i.MX 8M Plus Pico ITX SBC (J20). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. The Power Jack is physically placed at the top of the board as shown below.

Figure 32: Power Input Jack

Table 19: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[1]	2.8V	3V	3.3V	±20mV

[1] The i.MX 8M Plus Pico ITX SBC uses this voltage as backup power source to RTC controller when VCC_12V is OFF.

3.2 Power Consumption

Table 20: i.MX 8M plus Pico ITX SBC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Power Consumption during booting		
During Booting	VCC_ 12V	0.226A/2.172W
Run Mode Power Consumption[1]		
Play 1080p Video run in MIPI display	VCC_ 12V	0.35A/4.2W
Play 1080p Video run in in 4K HDMI display	VCC_ 12V	0.318A/3.816W
Play 1080p Video run in in 10'Inch LVDS display	VCC_ 12V	0.815A/9.78W
Camera streaming in HDMI	VCC_ 12V	0.312A/3.744W
Camera Streaming in MIPI	VCC_ 12V	0.335A/4.02W
Camera Streaming in 10'Inch LVDS	VCC_ 12V	0.885A/10.62W
GPU Processor -Graphics 3D Test	VCC_ 12V	0.349A/4.188W
Play Audio	VCC_ 12V	0.233A/2.796W
Ping Bluetooth	VCC_ 12V	0.218A/2.616W
Ping Wi-Fi	VCC_ 12V	0.258A/3.096W
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_ 12V	0.293A/3.516W
eMMC to Micro SD file transfer	VCC_ 12V	0.27A/3.24W
eMMC to USB3.0 file transfer	VCC_ 12V	0.322A/3.864W
eMMC to M.2 PCIe file transfer	VCC_ 12V	0.306A/3.672W
Dhrystone	VCC_ 12V	0.236A/2.832W
Maximum Power Test: • Maximum Power Test, • Run the below during Maximum Power Test, • Run the video on MIPI diplay,10Inch LVDS & HDMI Connected • Run the Camera Streaming • Ethernet - Run the ping (65500 packet size) test on background (eth0 & eth1) • WIFI- Run the ping test on background • FileTransfer - Transfer the 1MB files in storage devices • Run dry2 application • Run the Graphics (GPU) application on HDMI display	VCC_ 12V	1.422A/17.064W
Low Power Mode Power Consumption		
System Idle Mode.	VCC_ 12V	0.176A/2.112W
Deep Sleep Mode.	VCC_ 12V	0.08A/0.96W

[1] *Power consumption measurements have been done in iWave's i.MX 8Mplus based Pico ITX SBC with iWave's iW-PRGJJ-SC-01-R1.0-REL1.0-Linux 5.4.70 BSP.*

3.3 EnvironmentalCharacteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Plus Pico ITX SBC.

Table 21: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[3] For more information on Thermal solution & Heat sink refer the following section.

3.3.1 Heat Sink

For any highly integrated SBC, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink must be used. Always need to remember that more effective thermal solution will give more performance out of the CPU.

Note: iWave supports Heat Sink Solution for i.MX 8M Plus Pico ITX SBC. For more information on Heat Sink contact iWave support team. Do not Power On the i.MX 8M Plus Pico ITX SBC without a proper thermal solution.

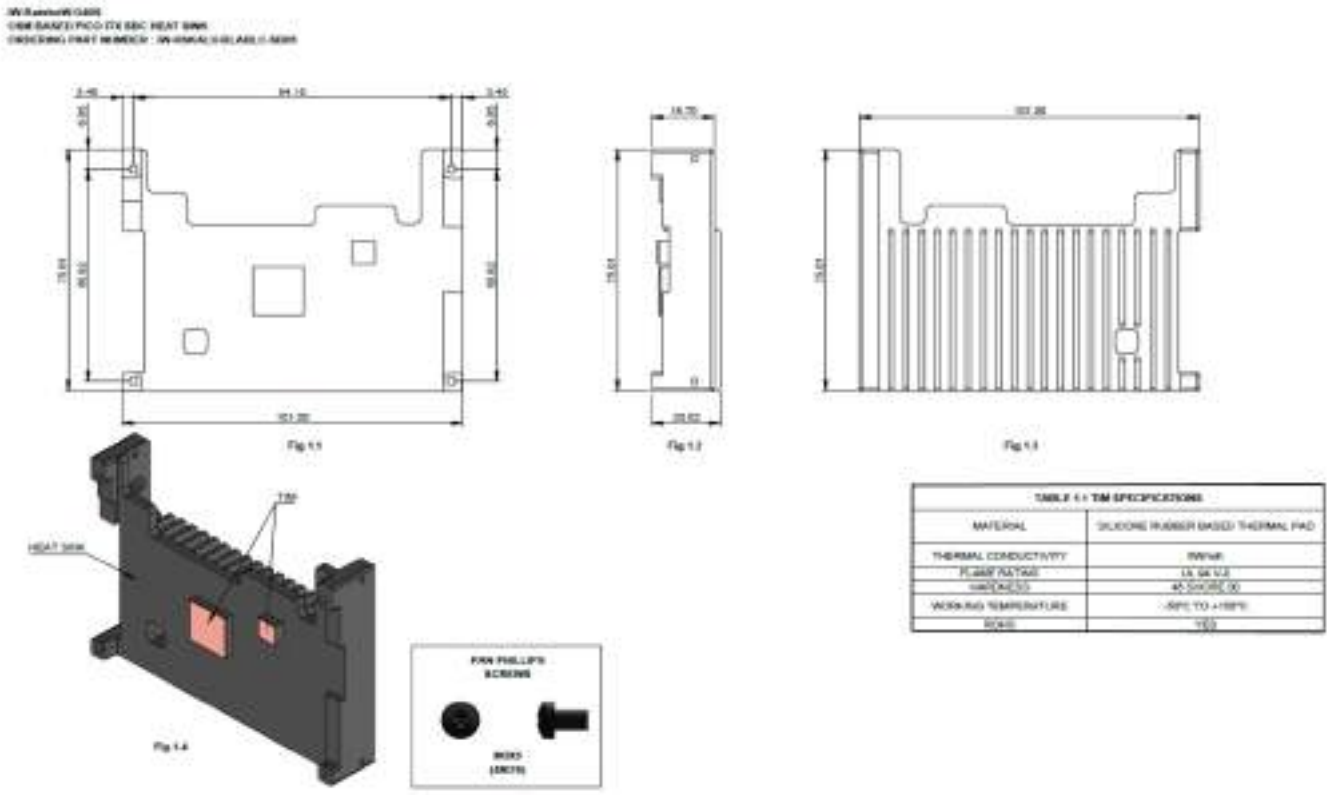

Figure 33: Mechanical Dimension of Heat sink

3.3.2 RoHS Compliance

iWave's i.MX 8M Plus Pico ITX SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's i.MX 8M Plus Pico ITX SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.4 MechanicalCharacteristics

3.4.1 i.MX 8M Plus Pico ITX SBC Mechanical Dimensions

i.MX 8M Pico ITX SBC PCB size is 100mm x 72mm x 1.2mm. Pico ITX SBC mechanical dimension is shown below. (All dimensions are shown in mm)

The i.MX 8M Plus Pico ITX SBC PCB thickness is 1.2mm±0.15mm, top side maximum height component is 16.40mm (HDMI Connector), followed by Dual Ethernet Connector (16.40mm). In bottom side maximum height component is JTAG connector (5.91mm) followed by M.2 SMT spacer (3.99mm).

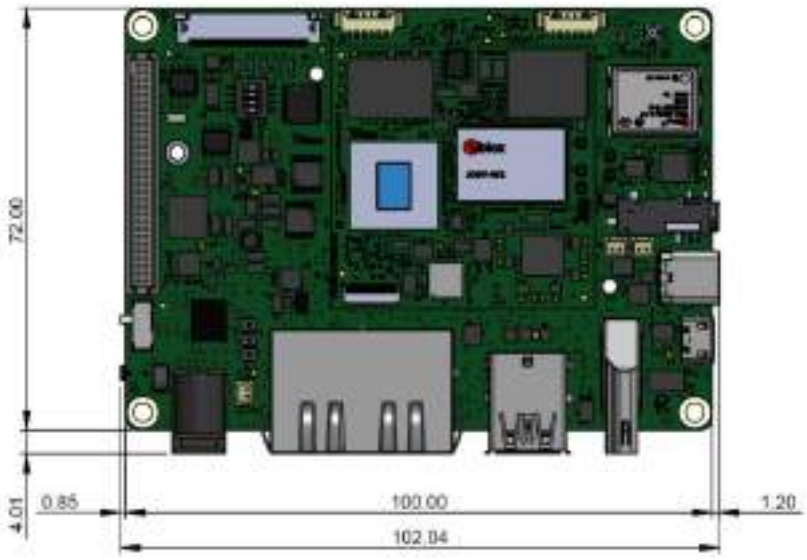

Figure 34: i.MX 8M Plus Pico ITX SBC Mechanical Dimensions Top View

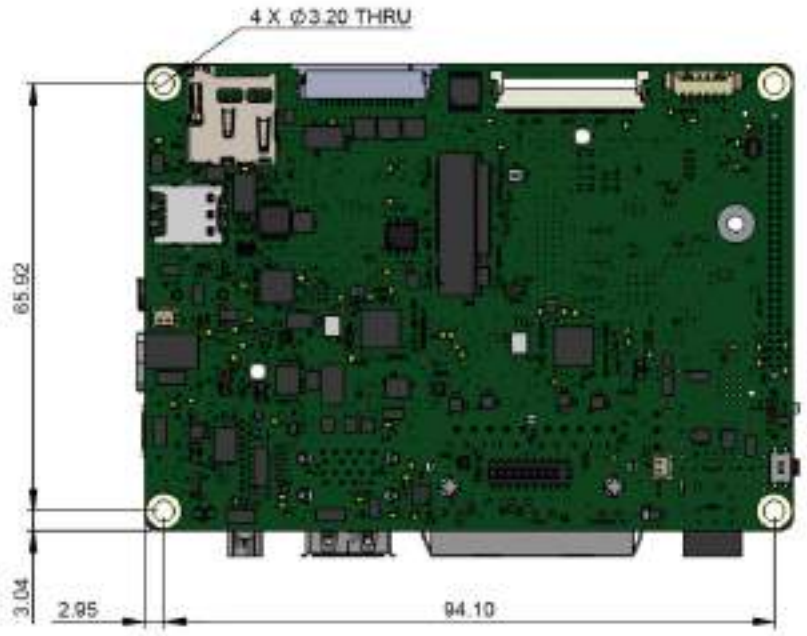

Figure 35: i.MX 8M Plus Pico ITX SBC Mechanical Dimensions Bottom View

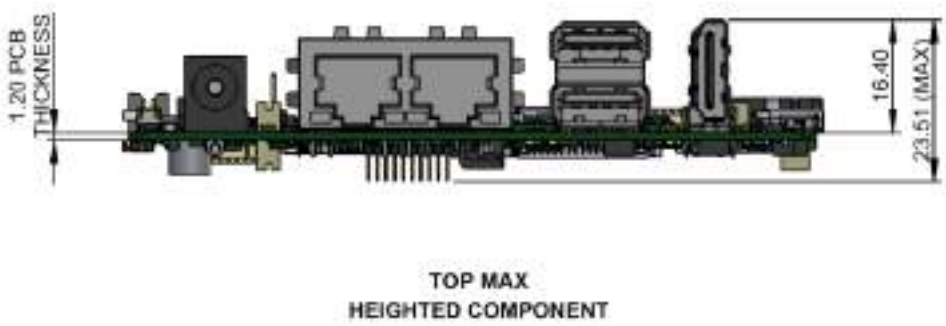

Figure 36: i.MX 8M Plus Pico ITX SBC Mechanical Dimensions - Side View 1

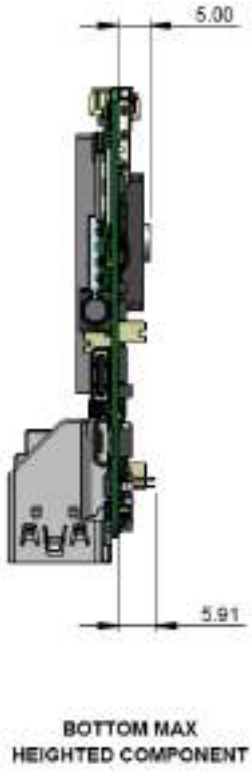

Figure 37: i.MX 8M Plus Pico ITX SBC Mechanical Dimensions - Side View 2

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8M Plus Pico ITX SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 22: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G40S - i.MX 8M Plus Pico ITX SBC (industrial grade)		
iW-G40S-OLPQ-4L002G-E016G-BIA	i.MX8M Plus Quad, 2GB LPDDR4, 16GB eMMC, With Wi-Fi/BT	-40°C to 85°C
iW-G40S-OLPQ-4L004G-E016G-BIA	i.MX8M Plus Quad, 4GB LPDDR4, 16GB eMMC, With Wi-Fi/BT	-40°C to 85°C

For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.


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