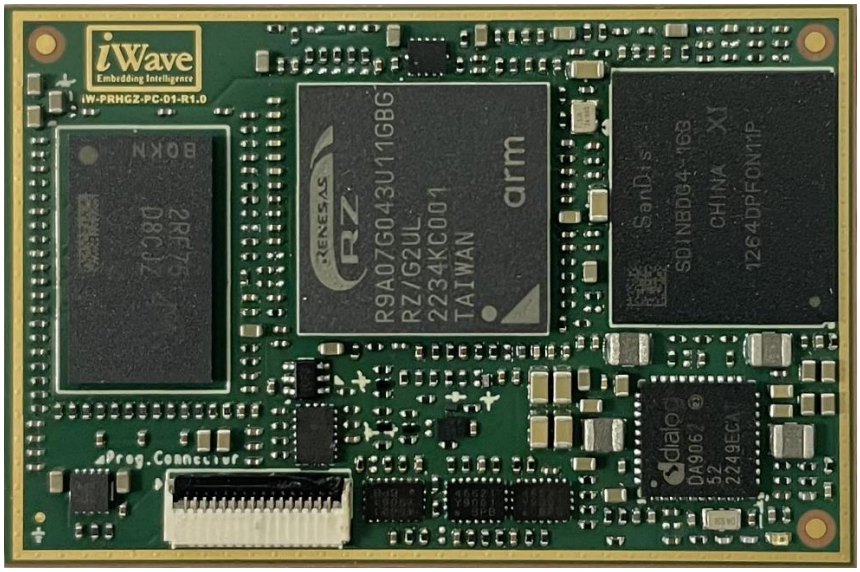
iW-RainboW-G53M
RZ/G2UL or RZ/FIVE or RZ/A3UL
OSM Size-MF Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL Application processor based on OSM v1.1 specification based LGA module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Renesas's RZ/A3UL, G2UL and FIVE OSM Module from a Hardware Systems perspective.

1.2 OSM LGA Module Overview

The OSM V1.1 ("Open Standard Modules™") is a future proof and versatile standard for small size, low-cost embedded computer modules. Combining the key characteristics like completely machine processible during soldering, assembly and testing, Pre-tinned LGA package for direct PCB soldering without connector.

The OSM Module definition targeting application that requires low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL based OSM LGA Module is rich with Renesas features along with on SOM DDR4, eMMC and comes in compact 30mm x 45mm form factor (OSM Size M). The Module PCB has 476 contacts which can be mounted as LGA/BGA on the OSM Carrier Card.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface
DC	Direct current
eMMC	Enhanced Multi Media Card

Acronyms	Abbreviations
EMS	Electronics manufacturing services
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FLEXCAN	Flexible Control Area Network
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
MHz	Mega Hertz
MB	Mega Byte
Mbps	Mega Bits Per Second
MIPI	Mobile Industry Processor Interface
mm	millimetre
MMC	Multi Media Card Interface
NA	Not Applicable
OSM	Open Standard Module
OTG	On-The-Go
PCB	Printed Circuit Board
PMIC	Power Management Integrated circuit
PWM	Pulse Width Modulation
RAM	Random Access Memory
REACH	Regulation Evaluation Authorization of Chemical Substances
RGMII	Reduced gigabit media-independent interface
RIIC	Rx family Inter Integrated Circuit
RoHS	Restriction of Hazardous Substances
RSPI	Rx Family Serial Peripheral Interface
RTC	Real Time Clock
RTS	Request to Send
SCIF	Serial Communication Interface with FIFO
SDHC	Secure Digital High Capacity
SD	Secure Digital
SoC	System on Chip
SOM	System On Module
SPI	Serial Peripheral Interface
SOM	System on Module
TBD	To Be Done
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
V	Voltage

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
PCIe	PCIe differential pair signals
USB	Universal Serial Bus
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-OSM.

1.5 References

- RZ/G2UL Hardware User Manual
- RZ/FIVE Hardware User Manual
- RZ/A3UL Hardware User Manual
- OSM Specification v1.1

1.6 Important Note

In this document, wherever the Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL MPU signal name is mentioned, it is followed as per below format for easy understanding.

- If MPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET1_RGMII_TXC

  In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to MPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about Renesas RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module SOM Hardware architecture with high level block diagram.

2.1 RZ/G2UL,RZ/FIVE and RZ/A3UL OSM LGA Module Block Diagram

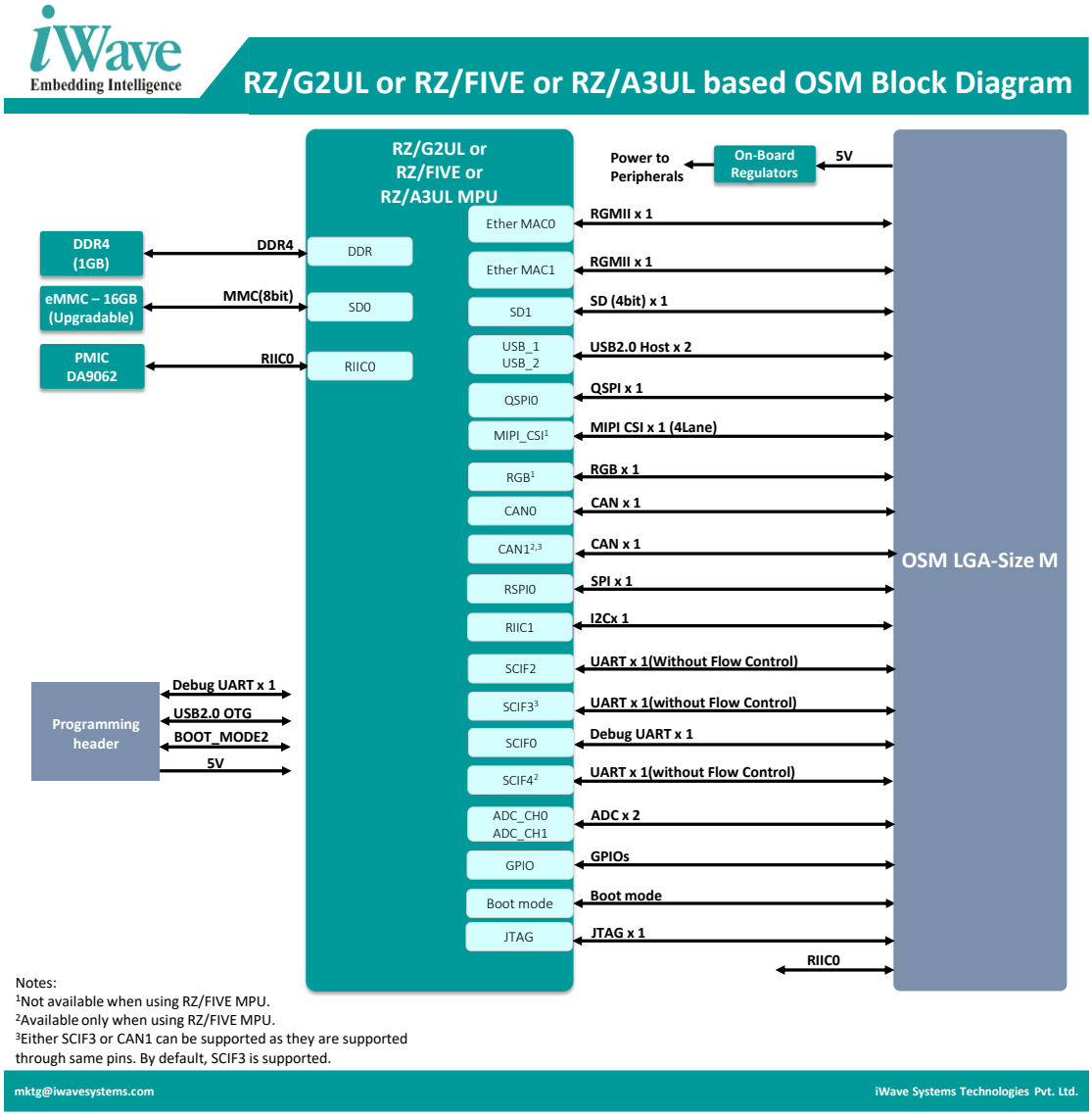

Figure 1: Renesas RZ/G2UL, RZ/FIVE or RZ/A3UL OSM LGA Block Diagram

2.2 RZ/G2UL, RZ/FIVE and RZ/A3UL SOM Features

iW-G53M-Renesas RZ/G2UL or RZ/FIVE or RZ/A3UL MPU based OSM supports the following features.

MPU

- RZ/G2UL: 1 x Cortex-A55 @1.0GHz, 1 x M33 core@200MHz
- RZ/FIVE: 1 x RISC-V (AX45MP Single) @1.0GHz
- RZ/ A3UL: 1 x Cortex-A55@1.0GHz

Power

- DA9062-52AM1 PMIC from Renesas

Memory

- 1GB DDR4 (Expandable)[1]
- 16GB eMMC Flash (Expandable)[1]

Other On-SOM Features

- Programming Header

OSM LGA Interfaces

- RGMII x 2 Ports
- SD (4bit) x 1 Port
- USB 2.0 Host x 1 Port
- USB 2.0 OTG x 1 Port
- QSPI x 1 Port
- RSPI x 1 Port
- MIPI CSI x 1 (4Lane) Port[2]
- I2C x 2 Ports
- RGB x 1 Port[2]
- CAN x 2 Ports[3]
- SCIF x 4(without Flow Control) Ports[4]
- Debug SCIF x 1 Port
- ADC x 2 Ports
- GPIOs
- Boot mode
- JTAG x 1 Port

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 30mm X 45mm (OSM v1.1 Specification – OSM Size-MF)

1. *Memory Size will differ based on iWave's SOM Product Part Number.*
2. *These features are supported only in RZ/G2UL and RZ/A3UL MPU and not in RZ/FIVE MPU.*
3. *2nd CAN support is only available in RZ/FIVE MPU and is multiplexed with SCIF3. By default, SCIF3 is supported.*
4. *3rd and 4th UART support is available only in RZ/FIVE CPU. UART4 supported through SCIF3 is multiplexed with CAN1 and by default SCIF3 is the supported interface.*

2.3 RZ/G2UL or RZ/FIVE or RZ/A3UL MPU

The iW-RainboW-G53M OSM LGA Module can support RZ/G2UL, RZ/FIVE or the RZ/A3UL MPUs from Renesas. The RZ/G2UL MPU features are given below:

- RZ/G2UL : 1 x Cortex-A55 @1.0GHz
  : 1 x M33 core@200MHz

The RZ/G2UL microprocessor includes a Cortex®-A55 (1.0 GHz) CPU, 16-bit DDR3L/DDR4 interface, and simple LCD controller. It also has many interfaces such as camera input, display output, USB 2.0, and Gbit-Ether, making it ideal for applications such as entry-class industrial gateway control and embedded devices with Simple GUI capabilities.

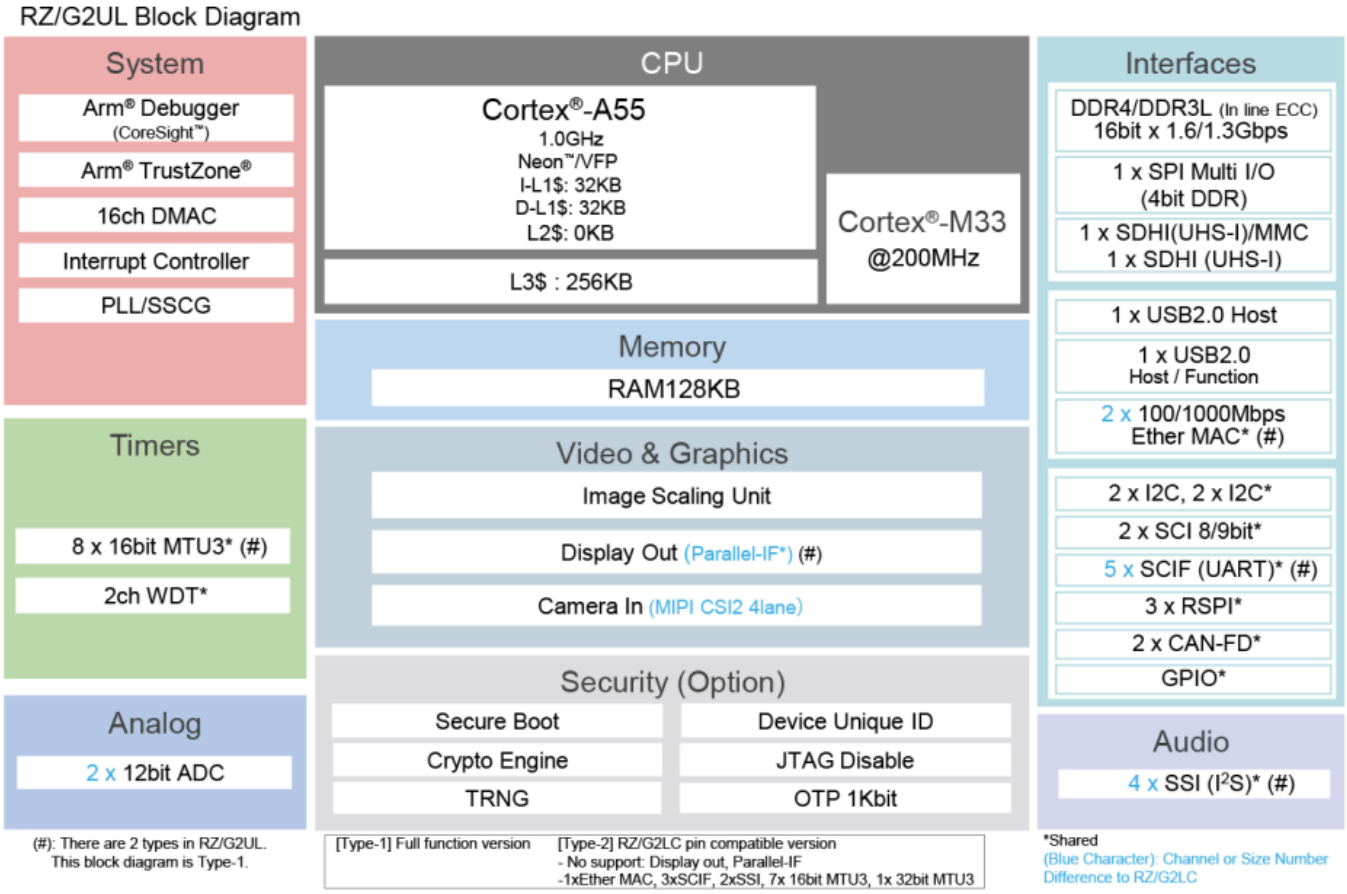

Figure 2: RZ/G2UL MPU Block Diagram

Note: The RZ/G2UL Microprocessor offers numerous advanced features, please refer the latest Datasheet of RZ/G2UL for Electrical characteristics and other information, which may be revised from time to time.

Similarly, the features of the RZ/FIVE MPU with RISC-V CPU core that can be supported in the iW-RainboW-G53M OSM is given below:

- RZ/FIVE : 1 x RISC-V (AX45MP Single) @1.0GHz

The RZ/Five microprocessor includes a RISC-V CPU Core (AX45MP Single) 1.0 GHz, 16-bit DDR3L/DDR4 interface. And it also has many interfaces such as Gbit-Ether, CAN, and USB 2.0, making it ideal for applications such as entry-class social infrastructure gateway control and industrial gateway control.

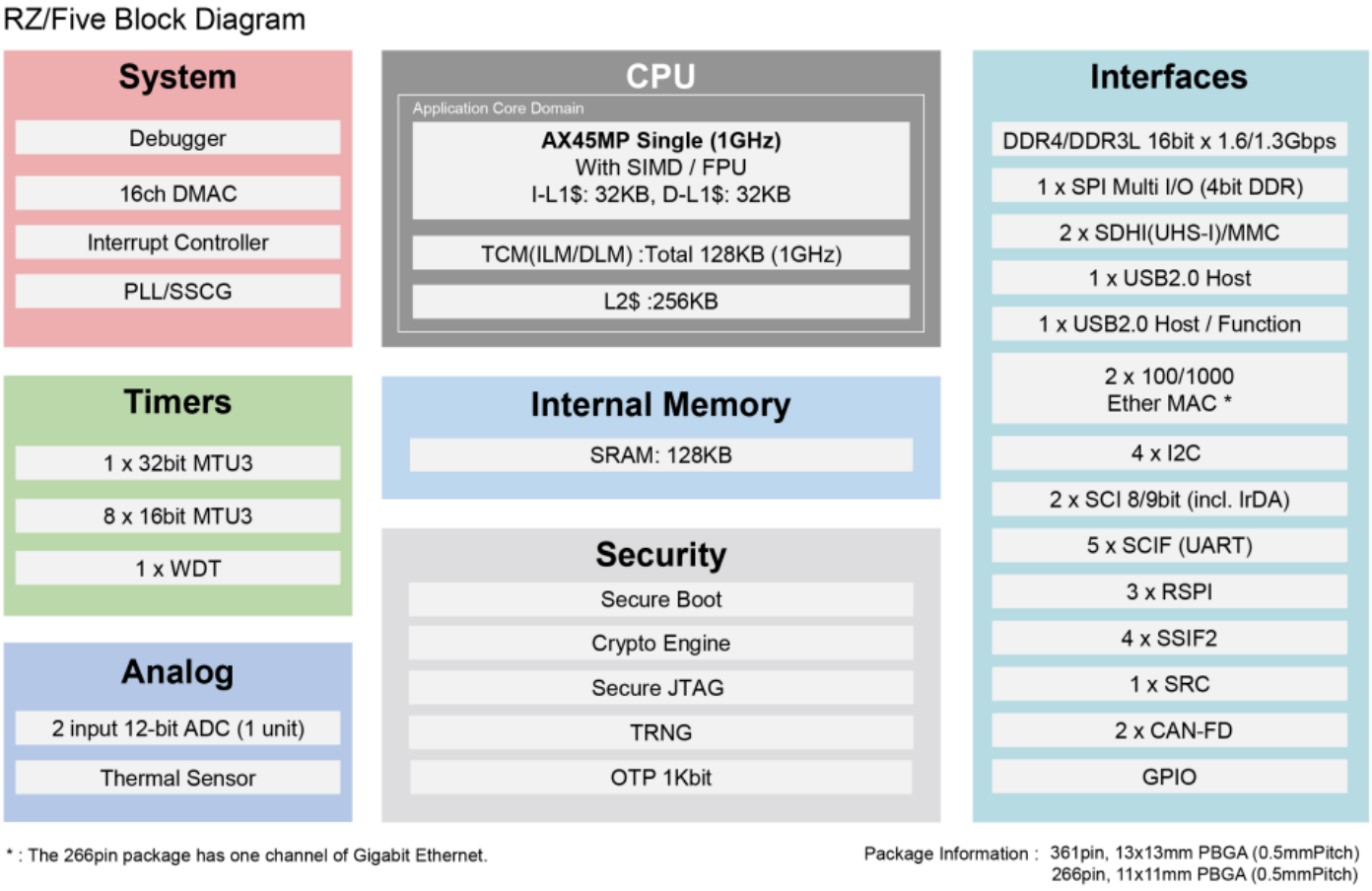

Figure 3: RZ/FIVE MPU Block Diagram

Note: The RZ/FIVE Microprocessor offers numerous advanced features, please refer the latest Datasheet of RZ/FIVE for Electrical characteristics and other information, which may be revised from time to time.

Similarly, the features of the RZ/A3UL MPU with RTOS support that can be supported in the iW-RainboW-G53M OSM is given below:

- RZ/A3UL : 1 x Cortex-A55@1.0GHz

The RZ/A3UL allows customers to achieve the full potential of a real-time operating system (RTOS) while leveraging the performance boost provided by the 64-bit Arm® Cortex®-A55 CPU core with a maximum operating frequency of 1 GHz. Using an RTOS allows systems to start up instantly, in less than a second after boot-up. This feature is ideal for systems that require a fast response time such as industrial equipment, home appliances and office automation equipment with liquid crystal displays or control panels, as well as POS terminals.

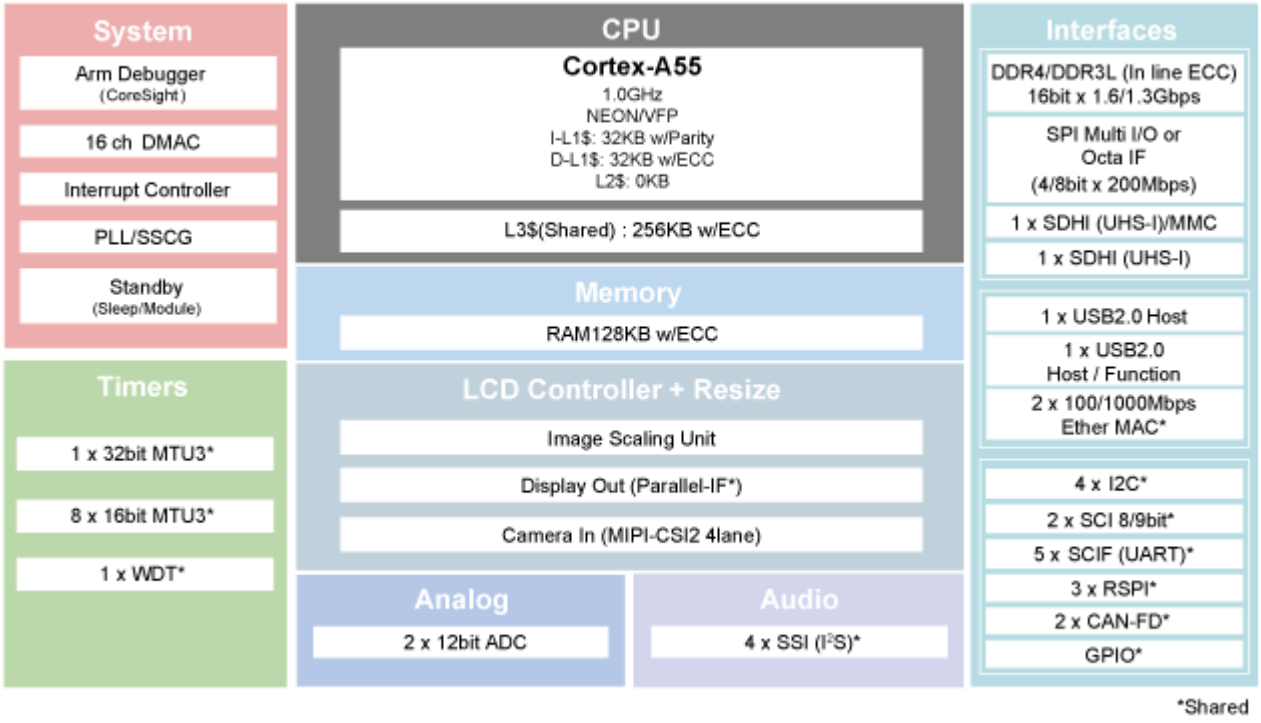

Figure 4: RZ/A3UL MPU Block Diagram

Note: The RZ/A3UL Microprocessor offers numerous advanced features, please refer the latest Datasheet of RZ/A3UL for Electrical characteristics and other information, which may be revised from time to time.

2.4 PMIC with RTC

The RZ/G2UL, RZ/FIVE or RZ/A3UL OSM LGA uses the DA9062-52AM1 (U8) PMIC from Renesas for module power management. The DA9062-52AM1 PMIC features four high efficiency Buck Regulators and four Linear regulators. It is a programable power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators.

The DA9062-52AM1 PMIC is pre-programmed as per the voltage, power sequence and other requirements of RZ/G2UL, RZ/FIVE or RZ/A3UL MPUs. The RIIC0 I2C from the RZ/G2UL, RZ/FIVE or RZ/A3UL MPU is used connected to the PMIC. The I2C slave address of the PMIC is 0x58.

2.5 Memory

2.5.1 DDR4 RAM

The RZ/G2UL, RZ/FIVE or RZ/A3UL OSM LGA Module can support up to 4GB DDR4 RAM memory using the 16bit DDR_CH0 channel of the MPU. The DDR4 part U4 placed at the top of the board can operate at speed of up to 1.2GHz.

By default, in RZ/G2UL and RZ/A3UL, the default DDR density is 2GB and in RZ/FIVE, the density is 1GB. To customize the DDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The RZ/G2UL, RZ/FIVE or RZ/A3UL OSM LGA Module supports 16GB eMMC as default boot and storage device. This is directly connected to SD0 controller of the MPU and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory (U2) is physically located on Top side of the Module. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.6 OSM LGA/BGA Balls

OSM LGA/BGA Balls has standard pinout as per OSM Specification v1.1. The interfaces which are available at 476 contacts are explained in the following sections.

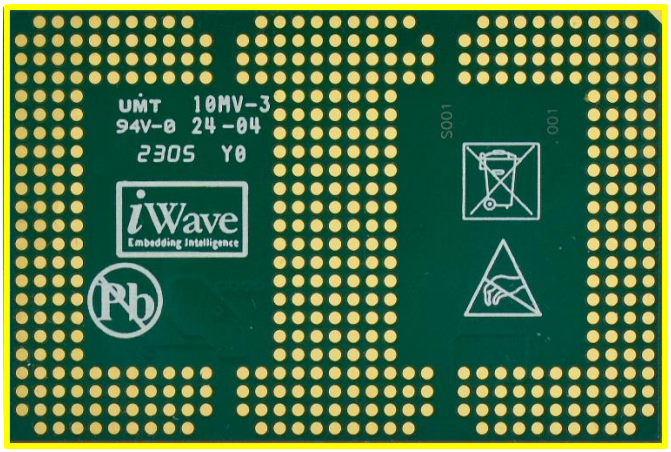

Figure 5: OSM LGA/BGA Balls

Number of contacts - : 476

Table 3: OSM Pinouts

OSM Pins	Signal
SIZE 0	
M18	ADC_CH0
N18	ADC_CH1
U19	BOOT_SEL0#
R18	NC
AB17	CAN0_RX_1V8
AC17	CAN0_TX_1V8
AB19	CAN1_RX[1]
AC19	NC (Optionally CAN1_TX is connected)[1]
V17	PMIC_PGOOD_1V8
A15	GND
A16	NC
A17	GND
A18	GND
A19	GND
A20	NC
A21	GND
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
C15	NC
C17	NC
C19	NC
C21	NC
AC18	DEBUGEN_1V8
F15	NC
E16	NC
R15	ET0_RXC/RX_CLK
M15	ET0_RX_CTL/RX_DV
L16	NC
N15	ET0_RXD2
P15	ET0_RXD3
J15	ET0_TXC/TX_CLK
K16	ET0_TX_CTL/TX_EN
K15	ET0_RXD0

OSM Pins	Signal
L15	ET0_RXD1
H15	ET0_TXD0
G15	ET0_TXD1
H16	ET0_TXD2
G16	ET0_TXD3
N16	NC
M17	VCC_3V3
T16	ET0_MDC
T15	ET0_MDIO
T17	FORCE_RECOV#
F16	GND
J16	GND
J20	GND
E21	GND
E15	GND
M16	GND
M20	GND
P18	GND
R16	GND
R20	GND
V16	GND
V20	GND
Y18	GND
AA14	GND
AA17	GND
AA19	GND
AA22	GND
AB15	GND
AB21	GND
D18	GND
L18	GND
F20	GND
D17	GPIO0
E17	GPIO1
F17	GPIO2
G17	GPIO3
H17	GPIO4
J17	GPIO7
K17	P4_2_1V8
L17	P15_2_1V8
D19	P14_1_1V8

OSM Pins	Signal
E19	NC
F19	NC
G19	NC
H19	NC
J19	NC
K19	NC
L19	NC
AA15	RIIC1_SCL_1V8
AA16	RIIC1_SDA_1V8
AA20	RIIC0_SCL_1V8
AA21	RIIC0_SDA_1V8
V21	NC
W21	NC
V19	NC
W19	NC
W20	NC
W18	NC
V18	NC
R19	JTAG_TRST#
P19	NC
N17	JTAG_TCK
P17	JTAG_TDI
R17	JTAG_TDO
N19	JTAG_TMS
E18	MTIOC3A_1V8
F18	MTIOC4D[1]
G18	NC
H18	NC
J18	NC
K18	NC
T18	NC
T19	NC
Y13	NC
Y14	NC
AA13	NC
W17	VRTC_3V0
J21	SD1_CD_B(P0_2)
F21	SD1_CLK
E20	SD1_CMD
G20	SD1_DATA0
G21	SD1_DATA1

OSM Pins	Signal
H20	SD1_DATA2
H21	SD1_DATA3
C20	VDD_SD1
D21	SDIO_A_PWR_EN
D20	SD1_WP(P0_3)
T21	NC
K20	NC
K21	NC
L20	NC
L21	NC
M21	NC
N20	NC
N21	NC
P20	NC
P21	NC
R21	NC
T20	NC
U21	NC
U20	NC
W15	QSPI0_IO3
W16	QSPI0_IO2
Y15	QSPI0_CS0
U16	QSPI0_SCLK
U15	QSPI0_IO0
V15	QSPI0_IO1
AA23	RSPI0_SSL_1V8
Y21	RSPI0_CK_1V8
Y22	RSPI0_MISO_1V8
Y23	RSPI0_MOSI_1V8
U17	SYS_RST#_1V8
C18	NC
C14	NC
C13	NC
A14	SCIF2_RXD_1V8
B13	SCIF2_TXD_1V8
D16	NC
D15	NC
D14	SCIF1_RXD_1V8
D13	SCIF1_TXD_1V8
A22	SCIF4_RXD[1]
B23	SCIF4_TXD[1]

OSM Pins	Signal
D22	SCIF0_RXD_1V8
D23	SCIF0_TXD_1V8
C22	SCIF3_RXD[1]
C23	SCIF3_TXD[1]
AB13	USB0_DM
AC14	USB0_DP
AC16	USB0_VBUSEN_1V8
AB14	USB0_OTG_ID_1V8
AC15	USB0_OVRCUR_1V8
AB16	OTG1_VBUS
AB23	USB1_DM
AC22	USB1_DP
AC20	USB1_VBUSEN_1V8
AB22	USB_B_ID
AC21	USB1_OVRCUR_1V8
AB20	NC
AB18	NC
AA18	NC
M19	VDD_1V1
Y16	VCC_3V3
Y20	VCC_1V8
Y19	NC
Y17	VCC_IN_5V
U18	NC
B22	nRESETREQ
C16	AUDIO_CLK1
P16	AUDIO_CLK2
SIZE S	
C2	NC
G3	GPIO5
G4	GPIO6
B3	CSI_CLK_N[2]
B4	CSI_CLK_P[2]
C1	CSI_DATA0_N[2]
B1	CSI_DATA0_P[2]
A2	CSI_DATA1_N[2]
A3	CSI_DATA1_P[2]
A5	CSI_DATA2_N[2]
A6	CSI_DATA2_P[2]
B6	CSI_DATA3_N[2]
B7	CSI_DATA3_P[2]

OSM Pins	Signal
AB8	NC
AB7	NC
AB11	NC
AB10	NC
AC9	NC
AC8	NC
AC6	NC
AC5	NC
AB5	NC
AB4	NC
AA3	NC
E1	NC
D2	NC
P1	ET1_RXC/RX_CLK
L1	ET1_RX_CTL/RX_DV
K2	NC
M1	ET1_RXD2
N1	ET1_RXD3
H1	ET1_TXC/TX_CLK
J2	ET1_TX_CTL/TX_EN
J1	ET1_RXD0
K1	ET1_RXD1
G1	ET1_TXD0
F1	ET1_TXD1
G2	ET1_TXD2
F2	ET1_TXD3
C6	ET1_MDC
C7	ET1_MDIO
M2	NC
B5	GND
D8	GND
P4	GND
AC10	GND
AC7	GND
AC4	GND
AB9	GND
AB6	GND
AB3	GND
AA11	GND
AA10	GND
AA8	GND

OSM Pins	Signal
A4	GND
A7	GND
A10	GND
B2	GND
B8	GND
B9	GND
C11	GND
D1	GND
D5	GND
E2	GND
H2	GND
H4	GND
L2	GND
L4	GND
P2	GND
U2	GND
U4	GND
V1	GND
W3	GND
Y2	GND
AA1	GND
AA4	GND
AA7	GND
R1	GND
D3	NC
D4	NC
E3	NC
E4	NC
F3	NC
F4	NC
C4	RIIC1_SCL_1V8
C3	RIIC1_SDA_1V8
AB2	NC
AB1	NC
AC3	NC
AC2	NC
V2	NC
W2	NC
Y1	NC
W1	NC
R2	NC

OSM Pins	Signal
T1	NC
U1	NC
T2	NC
AA9	PWR_BTN#
M4	DISP_CLK[2]
R4	DISP_DATA18[2]
R3	DISP_DATA19[2]
P3	DISP_DATA20[2]
N3	DISP_DATA21[2]
N4	DISP_DATA22[2]
M3	DISP_DATA23[2]
H3	NC
J4	DISP_DE[2]
K4	NC
W4	DISP_DATA10[2]
V3	DISP_DATA11[2]
V4	DISP_DATA12[2]
U3	DISP_DATA13[2]
T3	DISP_DATA14[2]
T4	DISP_DATA15[2]
K3	DISP_HSYNC[2]
Y7	DISP_DATA2[2]
AA6	DISP_DATA3[2]
Y6	DISP_DATA4[2]
AA5	DISP_DATA5[2]
Y5	DISP_DATA6[2]
Y4	DISP_DATA7[2]
J3	RGB_RESET(P0_0)
L3	DISP_VSYNC[2]
AA2	NC
N2	NC
D11	NC
D10	NC
C10	NC
D9	NC
C8	NC
B11	NC
B10	NC
A9	NC
A8	NC
C9	NC

OSM Pins	Signal
Y3	VDD_DDR_2V5
C5	VDD_PVDD_1
Y11	VCC_IN_5V
Y10	VCC_IN_5V
Y9	VCC_IN_5V
Y8	VCC_IN_5V
D6	BSCANP
D7	NMI
SIZE M	
AA31	NC
AA30	NC
AA29	QSPI_RESET#
Y31	PMIC_TP
Y30	PMIC_SCL
Y29	PMIC_SDA
Y27	VCC_IN_5V
Y26	VCC_IN_5V
Y25	VCC_IN_5V
Y28	VCC_IN_5V
B29	VDD_SD0
AA33	VDD_SD1
C27	NC
A27	NC
A28	NC
B25	NC
B26	NC
C28	NC
D27	NC
C26	NC
D25	NC
D26	NC
AB29	NC
AB30	NC
AC28	NC
AC29	NC
AB32	NC
AB33	NC
AC31	NC
AC32	NC
AB27	NC
AC26	NC

OSM Pins	Signal
D30	NC
C29	NC
D29	NC
C30	NC
AB26	NC
AB25	NC
T33	NC
T32	NC
R33	NC
R32	NC
P34	NC
P33	NC
P32	NC
N33	NC
N32	NC
M33	NC
M32	NC
L32	NC
K32	NC
J32	NC
K33	NC
L33	NC
K35	NC
L35	NC
L34	NC
M34	NC
Y33	NC
Y32	NC
W33	NC
W32	NC
V33	NC
V32	NC
U33	NC
U32	NC
AC33	GND
AC30	GND
AC27	GND
AB34	GND
AB31	GND
AB28	GND
AA32	GND

OSM Pins	Signal
A29	GND
A32	GND
B27	GND
B28	GND
B30	GND
B33	GND
C25	GND
C32	GND
C35	GND
D28	GND
D34	GND
F33	GND
F35	GND
G34	GND
H32	GND
J33	GND
J35	GND
K34	GND
M35	GND
N34	GND
AA28	GND
AA27	GND
AA26	GND
AA25	GND
W34	GND
T34	GND
A26	GND
R34	NC
AA35	NC
Y35	NC
U35	NC
V35	NC
AA34	NC
Y34	NC
V34	NC
N35	NC
P35	NC
R35	NC
U34	NC
T35	NC
W35	NC

OSM Pins	Signal
AC34	NC
AB35	NC
H34	NC
J34	NC
G35	NC
H35	NC
E34	NC
F34	NC
D35	NC
E35	NC
E33	NC
G32	NC
E32	NC
F32	NC
G33	NC
H33	NC
B34	NC
B35	NC
A33	NC
A34	NC
B31	NC
B32	NC
A30	NC
A31	NC
C31	NC
D33	NC
D31	NC
D32	NC
C33	NC
C34	NC

Note:

[1]These functions are supported only when using RZ/Five MPU.

[2]These functions are supported only when using RZ/G2UL & RZ/A3UL MPU.

2.6.1 RGMII Interface

The RZ/G2UL, RZ/FIVE or RZ/A3UL MPU based OSM LGA Module supports RGMII interface on OSM LGA. RZ/G2UL, RZ/FIVE or the RZ/A3UL provides two Ethernet Interfaces ET0 and ET1. The two RGMII Lanes are connected to OSM LGA. Connection of the RZ/G2UL, RZ/FIVE or RZ/A3UL to the world wide web or a local area network (LAN) is possible using the GbE PHY which is off the module. The PHY can be selected which operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

For more details on ET0 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	MPU Ball Name/ Pin Number	Signal Type/ Termination	Description
H15	ETH_A_(S)(R)(G)MII_TXD0	ET0_TXD0	P1_2/L1	O, 3.3V CMOS	Transmit data bit 0 (transmitted first) port A.
G15	ETH_A_(S)(R)(G)MII_TXD1	ET0_TXD1	P1_3/L2	O, 3.3V CMOS	Transmit data bit 1 port A.
H16	ETH_A_(S)(R)(G)MII_TXD2	ET0_TXD2	P1_4/K1	O, 3.3V CMOS	Transmit data bit 2 port A.
G16	ETH_A_(S)(R)(G)MII_TXD3	ET0_TXD3	P2_0/K2	O, 3.3V CMOS	Transmit data bit 3 port A.
K16	ETH_A_(R)(G)MII_TX_EN(_ER)	ET0_TX_CTL/TX_EN	P1_1/M1	O, 3.3V CMOS	Transmit enable (Error) port A.
J15	ETH_A_(R)(G)MII_TX_CLK	ET0_TXC/TX_CLK	P1_0/M2	I/O, 3.3V CMOS	Transmit clock port A.
K15	ETH_A_(S)(R)(G)MII_RXD0	ET0_RXD0	P3_2/P2	I, 3.3V CMOS	Receive data bit 0 (received first) port A.
L15	ETH_A_(S)(R)(G)MII_RXD1	ET0_RXD1	P3_3/R3	I, 3.3V CMOS	Receive data bit 1 port A.
N15	ETH_A_(R)(G)MII_RXD2	ET0_RXD2	P4_0/R2	I, 3.3V CMOS	Receive data bit 2 port A.
P15	ETH_A_(R)(G)MII_RXD3	ET0_RXD3	P4_1/R1	I, 3.3V CMOS	Receive data bit 3 port A.
M15	ETH_A_(R)(G)MII_RX_DV(_ER)	ET0_RX_CTL/RX_DV	P3_1/N1	I, 3.3V CMOS	Receive data valid port A.

Pin No.	OSM Pin Name	OSM Signal Name	MPU Ball Name/ Pin Number	Signal Type/ Termination	Description
R15	ETH_A_(R)(G)MII_RX_CLK	ET0_RXC/RX_CLK	P3_0/N3	I, 3.3V CMOS	Receive clock port A.
T15	ETH_MDIO	ET0_MDIO	P4_3/T3	I/O, 3.3V CMOS	Management bus data signal for Ethernet.
T16	ETH_MDC	ET0_MDC	P4_4/T2	O, 3.3V CMOS	Management bus clock signal for Ethernet.
M17	ETH_IOPWR	VCC_3V3	NA	Power, 3.3V	Ethernet IO voltage. It is used to provide the IO Voltage.

For more details on ET1 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
G1	ETH_B_(S)(R)(G)MII_TXD0	ET1_TXD0	P7_2/AD16	O, 3.3V CMOS	Transmit data bit 0 (transmitted first) port A
F1	ETH_B_(S)(R)(G)MII_TXD1	ET1_TXD1	P7_3/AE16	O, 3.3V CMOS	Transmit data bit 1 port B
G2	ETH_B_(R)(G)MII_TXD2	ET1_TXD2	P7_4/AD15	O, 3.3V CMOS	Transmit data bit 2 port B
F2	ETH_B_(R)(G)MII_TXD3	ET1_TXD3	P8_0/AE15	O, 3.3V CMOS	Transmit data bit 3 port B
J2	ETH_B_(R)(G)MII_TX_EN(_ER)	ET1_TX_CTL/TX_EN	P7_1/AD17	O, 3.3V CMOS	Transmit enable (Error) port B
H1	ETH_B_(R)(G)MII_TX_CLK	ET1_TXC/TX_CLK	P7_0/AE18	O, 3.3V CMOS	Transmit clock port B
J1	ETH_B_(S)(R)(G)MII_RXD0	ET1_RXD0	P9_1/AE19	I, 3.3V CMOS	Receive data bit 0 (received first) port B
K1	ETH_B_(S)(R)(G)MII_RXD1	ET1_RXD1	P9_2/AD19	I, 3.3V CMOS	Receive data bit 1 port B
M1	ETH_B_(R)(G)MII_RXD2	ET1_RXD2	P9_3/AE20	I, 3.3V CMOS	Receive data bit 2 port B
N1	ETH_B_(R)(G)MII_RXD3	ET1_RXD3	P10_0/AD20	I, 3.3V CMOS	Receive data bit 3 port B

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
L1	ETH_B_(R)(G)MII_RX_DV(_ER)	ET1_RX_CTL/RX_DV	P9_0/AC18	I, 3.3V CMOS	Receive clock port B
P1	ETH_B_(R)(G)MII_RX_CLK	ET1_RXC/RX_CLK	P8_4/AC17	I, 3.3V CMOS	Receive clock port B
C6	ETH_B_MDC	ET1_MDC	P10_2/AC20	I/O, 3.3V CMOS	Management bus data signal for Ethernet.
C7	ETH_B_MDIO	ET1_MDIO	P10_3/AE21	O, 3.3V CMOS	Management bus clock signal for Ethernet.

2.6.2 SD Interface

The RZ/G2UL, RZ/FIVE or RZ/A3UL MPU based OSM LGA Module supports 4bit SD interface over OSM LGA which can be used to connect SD card as Mass storage device. SDHI1 controller of the MPUs are used to support 4bit SD interface. SDHI1 controller can operate in both 3.3V and 1.8V IO level and supports card bus clock frequency up to 208 MHz. Controlling GPIOs like Write Protect and Card detect signals also operates at both 1.8V and 3.3V IO level.

For more details on SD pinouts, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
F21	SDIO_A_CLK	SD1_CLK	SD1_CLK/G2	IO, 1.8/3.3V CMOS	SD1 Clock.
E20	SDIO_A_CMD	SD1_CMD	SD1_CMD/H6	IO, 1.8/3.3V CMOS	SD1 Command/Response.
G20	SDIO_A_DO	SD1_DATA0	SD1_DATA0/H2	IO, 1.8/3.3V CMOS	SD1 Data Lines.
G21	SDIO_A_D1	SD1_DATA1	SD1_DATA1/J3	IO, 1.8/3.3V CMOS	SD1 Data Lines.
H20	SDIO_A_D2	SD1_DATA2	SD1_DATA2/J1	IO, 1.8/3.3V CMOS	SD1 Data Lines.
H21	SDIO_A_D3	SD1_DATA3	SD1_DATA3/J2	IO, 1.8/3.3V CMOS	SD1 Data Lines.
J21	SDIO_A_CD#	SD1_CD_B(P0_2)	P0_2/D3	I OD, 3.3V CMOS, 10K PU	SD1 Card Detect
D20	SDIO_A_WP	SD1_WP(P0_3)	P0_3/C3	I OD, 3.3V CMOS, 10K PU	SD1 Write Protect.
D21	SDIO_A_PWR_EN	NA	NA	O, 1.8/3.3V CMOS, 10K PU	SD1 Power Enable.
C20	SDIO_A_IOPWR	VDD_SD1		P, 1.8V	SD1 Voltage.

2.6.3 SPI Interface

The RZ/G2UL, RZ/FIVE or the RZ/A3UL MPUs supports QSPI and RSSPI interfaces over the OSM LGA. The QSPI interface can be used as a boot and storage device. The RSPI0 controller supports an efficient interface to an SPI bus as a master which can be used for storage device or can be connected to any other SPI slave. The i.MX 8M Plus OSM LGA Module supports SPI_A and SPI_B channels of the OSM using QSPI and RSPI0 controllers of MPU respectively.

For more details on QSPI pinouts through OSM SPI_A, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U15	SPI_A_SDI_(IO0)	QSPI0_IO0	QSPI0_IO0/C7	I/O, 1.8V CMOS	QSPI0 Master IN and Slave OUT.
V15	SPI_A_SDO_(IO1)	QSPI0_IO1	QSPI0_IO1/A5	I/O, 1.8V CMOS	QSPI0 Master OUT and Slave IN.
W16	SPI_A_/WP_(IO2)	QSPI0_IO2	QSPI0_IO2/B7	I/O, 1.8V CMOS	QSPI0 Input and Output
W15	SPI_A_/HOLD_(IO3)	QSPI0_IO3	QSPI0_IO3/C6	I/O, 1.8V CMOS	QSPI0 Input and Output
Y15	SPI_A_CS0#	QSPI0_CS0	QSPI0_SSL/B5	O, 1.8V CMOS	QSPI0 Master Chip Select 0.
U16	SPI_A_SCK	QSPI0_SCLK	QSPI0_SPCLK/B6	O, 1.8V CMOS	QSPI0 Serial Data Clock.

For more details on RSPI0 pinouts through OSM SPI_B, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y22	SPI_B_SDI	RSPI0_MISO_1V8	P2_3/M6	I, 1.8V CMOS	RSPI0 Master IN and Slave OUT.
Y23	SPI_B_SDO	RSPI0_MOSI_1V8	P2_2/M3	O, 1.8V CMOS	RSPI0 Master IN and Slave OUT.
AA23	SPI_B_CS0#	RSPI0_SSL_1V8	P18_5/A21	O, 1.8V CMOS	RSPI0 Master Chip Select 0.
Y21	SPI_B_SCK	RSPI0_CK_1V8	P2_1/K6	O, 1.8V CMOS	RSPI0 Serial Data Clock.

2.6.4 CAN Interface

The RZ/G2UL, RZ/FIVE and RZ/A3UL MPUs based OSM supports one CAN-FD interface support on the OSM. The RZ/FIVE MPU based OSM module is capable of providing an additional CAN in the module, when SCIF3 interface is not used.

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported by the FlexCAN module.

For more details of CAN_A pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC17	CAN_A_TX	CAN0_TX_1V8	P6_1/AE2	O, 1.8V CMOS	CAN 0 Transmitter.
AB17	CAN_A_RX	CAN0_RX_1V8	P6_2/AB2	I, 1.8V CMOS	CAN 0 Receiver.

For more details of CAN_B pinouts on OSM LGA of RZ/FIVE, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC19	CAN_B_TX	CAN1_TX	P24_2/B4	O, 1.8V CMOS	CAN 1 Transmitter.
AB19	CAN_B_RX	CAN1_RX	P24_3/A3	I, 1.8V CMOS	CAN 1 Receiver.

Note: *CAN_B support on the OSM LGA is not available in RZ/G2UL and RZ/A3UL based OSM. CAN_B can be supported in RZ/FIVE based OSM only when SCIF3 interface is not used.*

2.6.5 USB2.0 OTG Interface

The RZ/G2UL, RZ/FIVE or the RZ/A3UL MPU based OSM LGA Module supports two USB2.0 controllers USB0 and USB1. The USB0 controller of the MPU is connected to USB_A port of the OSM and the USB1 controller is connected to the USB_B port.

The USB0 controller supports OTG functionality and includes the PHY and I/O interfaces to support this operation. It supports High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps). It is fully compatible with the USB On-The-Go supplement to the USB 2.0 specification.

For more details on USB 2.0 OTG pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB13	USB_A_D_N	USB0_DM	USB0_DM/AE6	I/O, USB	USB2.0 Port0 Data Negative.
AC14	USB_A_D_P	USB0_DP	USB0_DP/AD6	I/O, USB	USB2.0 Port0 Data Positive.
AB14	USB_A_ID	USB0_OTG_ID_1V8	P5_3/AD2	I OD, 1.8V CMOS/ 10K PU	USB OTG ID.
AC15	USB_A_OC#	USB0_OVRCUR_1V8	P5_2/AE3	I OD, 1.8V CMOS/ 10K PU	USB2.0 Port0 Over Current Indicator.
AB16	USB_A_VBUS	OTG1_VBUS	NA	I USB VBUS 5V	USB Port0 Power detection.
AC16	USB_A_EN	USB0_VBUSEN_1V8	P5_0/AD3	O, 1.8V CMOS	USB Power enable.

2.6.6 USB2.0 Host Interface

The USB1 controller of the RZ/G2UL, RZ/FIVE or the RZ/A3UL MPU is connected to the USB_B port of the OSM and supports only the USB2.0 Host functionality. The USB0 controller supports USB Host functionality and includes the PHY and I/O interfaces to support this operation. It supports High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps).

For more details on USB2.0 Host pinouts on the OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB23	USB_B_D_N	USB1_DM	USB1_DM/AE5	I/O, USB	USB2.0 Port1 Data Negative.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC22	USB_B_D_P	USB1_DP	USB1_DP/AD5	I/O, USB	USB2.0 Port1 Data Positive.
AB22	USB_B_ID	USB_B_ID	NA	I OD, 1.8V CMOS/ 10K PU	USB OTG ID.
AC21	USB_B_OC#	USB1_OVRCUR_1V8	P5_4/AB3	I OD 1.8V CMOS/ 10K PU	USB 2.0 Port1 Over Current Indicator.
AB20	USB_B_VBUS	NA	NA	NA	NC.
AC20	USB_B_EN	USB1_VBUSEN_1V8	P18_4/B22	O, 1.8V CMOS	USB Power Enable.

2.6.7 I2C Interface

The RZ/G2UL, RZ/FIVE or the RZ/A3UL OSM supports two I2C interface on OSM LGA. The MPUs' RIIC1 & RIIC0 controllers are connected to the I2C_A and I2C_B ports of the OSM LGA respectively. The RIIC0 connected to I2C_B port is also connected to the On Module PMIC with the slave address 0x58.

For more details on the I2C pinouts on the OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA15	I2C_A_SCL	RIIC1_SCL_1V8	RIIC1_SCL/A19	O, 1.8V CMOS 2.2K PU	RIIC1 Clock.
AA16	I2C_A_SDA	RIIC1_SDA_1V8	RIIC1_SDA/A20	IO, 1.8V CMOS 2.2K PU	RIIC1 Data.
AA20	I2C_B_SCL	RIIC0_SCL_1V8	RIIC0_SCL/B19	O, 1.8V CMOS 2.2K PU	RIIC0 Clock.
AA21	I2C_B_SDA	RIIC0_SDA_1V8	RIIC0_SDA/B20	IO, 1.8V CMOS 2.2K PU	RIIC0 Data.

2.6.8 Data UART

The RZ/G2UL & RZ/A3UL OSM supports two UART channels on the OSM LGA excluding the Console UART. The RZ/FIVE MPU can support two additional UARTs bringing the count to four on the OSM LGA. In RZ/G2UL, RZ/FIVE and RZ/A3UL SCIF2 and SCIF1 are connected to UART_A and UART_B ports of the OSM LGA respectively. In addition to these two, SCIF4 and SCIF3 are available on UART ports UART_C and UART_D of the OSM respectively when RZ/FIVE is used. The Data UARTs can be used for any data communication. In addition to these the SCIF0 is connected to the Console UART on the OSM for debugging purposes.

For more details on UART pinouts on the OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A14	UART_A_RX	SCIF2_RXD_1V8	P5_1/AC3	I, 1.8V CMOS	SCIF2 Receiver.
B13	UART_A_TX	SCIF2_TXD_1V8	P6_0/AD1	O, 1.8V CMOS	SCIF2 Transmitter.
D14	UART_B_RX	SCIF1_RXD_1V8	P13_1/A11	I, 1.8V CMOS	SCIF1 Receiver.
D13	UART_B_TX	SCIF1_TXD_1V8	P11_2/B10	O, 1.8V CMOS	SCIF1 Transmitter.
A22	UART_C_RX	SCIF4_RXD[1]	P24_4/B3	I, 1.8V CMOS	SCIF4 Receiver.
B23	UART_C_TX	SCIF4_TXD[1]	P24_5/A2	O, 1.8V CMOS	SCIF4 Transmitter.
C22	UART_D_RX	SCIF3_RXD[1]	P24_1/A4	I, 1.8V CMOS	SCIF3 Receiver.
C23	UART_D_TX	CAN1_TX(SCIF3_TXD)[1]	P24_2/B4	O, 1.8V CMOS	SCIF3 Transmitter.

Note:
[1] These pins are available only in RZ/FIVE OSM.

2.6.9 Debug Console UART

In the RZ/G2UL, RZ/FIVE and RZ/A3UL OSM, the SCIF0 of the MPU is connected to the Console UART Port of the OSM LGA. This UART is used for getting the debug console prints and also for programming purposes.

For more details on Console UART pinouts on the OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D22	UART_CON_RX	SCIF0_RXD_1V8	P6_3/AC1	I, 1.8V CMOS	SCIF0 Receiver.
D23	UART_CON_TX	SCIF0_TXD_1V8	P6_4/AC2	O, 1.8V CMOS	SCIF0 Transmitter.

2.6.10PWM Interface

The RZ/G2UL and RZ/A3UL OSM supports one PWM interface on the PWM_0 port of the OSM LGA, while the RZ/FIVE OSM can support one additional PWM on PWM_1 port of the OSM LGA bringing the count to 2.

These PWM channels can be set to PWM mode independently and can have duty cycle in range of 0% to 100%. These two PWM can function in the PWM Mode 1 of the MPU and PWM waveforms in up to 12 phases can be output.

For more details on PWM pinouts on the OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
E18	PWM_0	MTIOC3A_1V8	P17_0/C16	O, 1.8V CMOS	Pulse width modulation 0.
F18	PWM_1	MTIOC4D[1]	P24_0/B2	O, 1.8V CMOS	Pulse width modulation 1.

Note: *This pin is available only when using RZ/FIVE OSM.*

2.6.11ADC Interface

The RZ/G2UL, RZ/A3UL and RZ/FIVE OSM supports two channels of ADC- ADC_CH0 and ADC_CH1 connected to ADC_0 and ADC_1 port of the OSM LGA respectively. These ADCs have a resolution of 12bit, 0V-1.8V input range and has a conversion time of 1µs. They can be operated in both single scan and continuous mode. The MPU pinout for RZ/FIVE is different with respect to RZ/G2UL and RZ/A3UL.

For more details on ADC pinouts on the RZ/G2UL & RZ/A3UL OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M18	ADC_0	ADC_CH0	ADC_CH0/B18	Analog ,1V8	Analog to Digital Converter 0.
N18	ADC_1	ADC_CH1	ADC_CH1/A18	Analog ,1V8	Analog to Digital Converter 1.

For more details on ADC pinouts on the RZ/FIVE OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M18	ADC_0	ADC_CH0	ADC_CH0/AE13	Analog ,1V8	Analog to Digital Converter 0.
N18	ADC_1	ADC_CH1	ADC_CH1/AD13	Analog ,1V8	Analog to Digital Converter 1.

2.6.12JTAG Interface

The RZ/G2UL, RZ/FIVE or the RZ/A3UL OSM supports JTAG interface for MPU debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features and boundary scan based on the IEEE Standard 1149.1 (JTAG).

For more details on JTAG pinouts on the OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
N17	JTAG_TCK(SWCLK)	JTAG_TCK	TCK/SWDCLK/U2	I CMOS ,1V8	JTAG test Clock.
N19	JTAG_TMS(SWDIO)	JTAG_TMS	TMS/SWDIO/U1	I CMOS ,1V8	JTAG test mode select.
P17	JTAG_TDI	JTAG_TDI	TDI/W1	I CMOS ,1V8	JTAG test data input.
P19	JTAG_RTCK	NA	NA	NA	NC.
R17	JTAG_TDO(SWO)	JTAG_TDO	TDO/V2	O CMOS ,1V8	JTAG test data output.
R19	JTAG_NTRST	JTAG_TRST#	TRST#/V1	I CMOS ,1V8	JTAG Reset.

2.6.13RGB Display interface

The RZ/G2UL and RZ/A3UL OSM supports single channel 18-bit parallel display output support on the OSM LGA. This can support max resolution of 1280 x 800 @60fps refresh rate. It also has support for the Clock, Vertical and Horizontal timing signals. The Output data format supported is RGB666.

The support for RGB display interface is available only in RZ/G2UL and RZ/A3UL OSM. When using RZ/FIVE MPU these pins can be used as GPIOs or as any other function mentioned in the pin multiplexing section.

For more details on RGB Display pinouts on the OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M4	RGB_(PIXEL)CLK	DISP_CLK	P11_3/ A10	O, 3.3V CMOS	Pixel clock signal
R4	RGB_B0	DISP_DATA18	P17_2/A16	O, 3.3V CMOS	Blue data bit 0
R3	RGB_B1	DISP_DATA19	P17_1/B16	O, 3.3V CMOS	Blue data bit 1
P3	RGB_B2	DISP_DATA20	P18_1/ A17	O, 3.3V CMOS	Blue data bit 2
N3	RGB_B3	DISP_DATA21	P18_2/ B17	O, 3.3V CMOS	Blue data bit 3
N4	RGB_B4	DISP_DATA22	P17_3/ C17	O, 3.3V CMOS	Blue data bit 4
M3	RGB_B5	DISP_DATA23	P18_3/ C20	O, 3.3V CMOS	Blue data bit 5
J4	RGB_DE	DISP_DE	P11_1/C9	O, 3.3V CMOS	Data Enable
W4	RGB_G0	DISP_DATA10	P16_0/ A14	O, 3.3V CMOS	Green data bit 0
V3	RGB_G1	DISP_DATA11	P15_0/ C14	O, 3.3V CMOS	Green data bit 1
V4	RGB_G2	DISP_DATA12	P16_1/B14	O, 3.3V CMOS	Green data bit 2
U3	RGB_G3	DISP_DATA13	P15_1/ C15	O, 3.3V CMOS	Green data bit 3
T3	RGB_G4	DISP_DATA14	P15_3/ A15	O, 3.3V CMOS	Green data bit 4
T4	RGB_G5	DISP_DATA15	P18_0/ F16	O, 3.3V CMOS	Green data bit 5
K3	RGB_HSYNC	DISP_HSYNC	P11_0/ B9	O, 3.3V CMOS	Horizontal sync
Y7	RGB_R0	DISP_DATA2	P13_0/ B11	O, 3.3V CMOS	Red data bit 0
AA6	RGB_R1	DISP_DATA3	P13_4/A12	O, 3.3V CMOS	Red data bit 1

Y6	RGB_R2	DISP_DATA4	P13_3/ B12	O, 3.3V CMOS	Red data bit 2
AA5	RGB_R3	DISP_DATA5	P12_1/C11	O, 3.3V CMOS	Red data bit 3
Y5	RGB_R4	DISP_DATA6	P13_2/C12	O, 3.3V CMOS	Red data bit 4
Y4	RGB_R5	DISP_DATA7	P14_0/C13	O, 3.3V CMOS	Red data bit 5
J3	RGB_RESET#	P0_0	P0_0/B1	O, 3.3V CMOS	Global Reset
L3	RGB_VSYNC	DISP_VSYNC	P12_0/ C10	O, 3.3V CMOS	Vertical sync

Note: *This feature is not available when using RZ/FIVE OSM.*

2.6.14MIPI CSI Camera Interface

The RZ/G2UL and RZ/A3UL OSM supports single channel 4-lane MIPI CSI camera interface support on the OSM LGA. The MIPI CSI-2 Rx block can receive signals conforming to MIPI CSI-2 standard. This module supports MIPI CSI-2 V2.1 and MIPI D-PHY V2.1 (80 Mbps ~ 1500 Mbps). This can be used to connect to 1/2/4 lanes cameras with maximum resolution of 5MP, 30fps (RAW12). It can support various input image data formats.

The support for the MIPI CSI camera interface is available only in RZ/G2UL and RZ/A3UL OSM. When using RZ/FIVE OSM these pins are NC.

For more details on MIPI CSI Camera pinouts on the RZ/G2UL & RZ/A3UL OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
C1	CSI_DATA0_N	CSI_DATA0_N	CSI_DATA0_N/NC /AE12	I, MIPI	MIPI CSI1 differential data lane0 negative.
B1	CSI_DATA0_P	CSI_DATA0_P	CSI_DATA0_P/NC /AD12	I, MIPI	MIPI CSI1 differential data lane0 positive.
A2	CSI_DATA1_N	CSI_DATA1_N	CSI_DATA1_N/NC /AE10	I, MIPI	MIPI CSI1 differential data lane1 negative.
A3	CSI_DATA1_P	CSI_DATA1_P	CSI_DATA1_P/NC /AD10	I, MIPI	MIPI CSI1 differential data lane1 positive.
A5	CSI_DATA2_N	CSI_DATA2_N	CSI_DATA2_P/AD C_CH1/AD13	I, MIPI	MIPI CSI1 differential data lane2 negative.
A6	CSI_DATA2_P	CSI_DATA2_P	CSI_DATA2_N/AD C_CH0/AE13	I, MIPI	MIPI CSI1 differential data lane2 positive.
B6	CSI_DATA3_N	CSI_DATA3_N	CSI_DATA3_N/NC /AE9	I, MIPI	MIPI CSI1 differential data lane3 negative.
B7	CSI_DATA3_P	CSI_DATA3_P	CSI_DATA3_P/NC /AD9	I, MIPI	MIPI CSI1 differential data lane3 positive.
B3	CSI_CLOCK_N	CSI_CLK_N	CSI_CLKN/NC/AE1 1	I, MIPI	MIPI CSI1 differential Clock negative
B4	CSI_CLOCK_P	CSI_CLK_P	CSI_CLKP/NC/AD1 1	I, MIPI	MIPI CSI1 differential Clock positive
C2	CAM_MCK	NA	NA	O, 1.8V CMOS	Master Clock for Camera.
C3	I2C_CAM_SDA / CSI_TX_N	RIIC1_SDA_1V8	RIIC1_SDA/A20	IO, 1.8V CMOS/ 2.2K PU	MIPI CSI1 I2C Data.
C4	I2C_CAM_SCL / CSI_TX_P	RIIC1_SCL_1V8	RIIC1_SCL/A19	IO, 1.8V CMOS/ 2.2K PU	MIPI CSI1 I2C Clock.

2.6.15OSM GPIOs

The RZ/G2UL, RZ/FIVE or the RZ/A3UL OSM supports GPIOs on the OSM LGA. Most of the MPU Pins which are connected to OSM LGA can be configured as GPIO with interrupt capability if not used as other interface. The MPU's GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

For the OSM GPIO ports, some of the signals are connected from a General-Purpose Output Expander, connected to RIIC1 with slave address 0x25.

For more details on GPIO Interface pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D17	GPIO_A_0	GPIO0	NA	O, 1.8V CMOS	OSM General Purpose Output A0.
E17	GPIO_A_1	GPIO1	NA	O, 1.8V CMOS	OSM General Purpose Output A1.
F17	GPIO_A_2	GPIO2	NA	O, 1.8V CMOS	OSM General Purpose Output A2.
G17	GPIO_A_3	GPIO3	NA	O, 1.8V CMOS	OSM General Purpose Output A3.
H17	GPIO_A_4	GPIO4	NA	O, 1.8V CMOS	OSM General Purpose Output A4.
J17	GPIO_A_5	GPIO7	NA	O, 1.8V CMOS	OSM General Purpose Output A5.
K17	GPIO_A_6	P4_2_1V8	P4_2/ N2	IO, 1.8V CMOS	OSM General Purpose Input/output A6.
L17	GPIO_A_7	P15_2_1V8	P15_2/ B15	IO, 1.8V CMOS	OSM General Purpose Input/output A7.
D19	GPIO_B_0	P14_1_1V8	P14_1/ B13	IO, 1.8V CMOS	OSM General Purpose Input/output B0.
F3	GPIO_C_4 / DISP_VDD_EN	P4_5_1V8	P4_5/ P1	IO, 1.8V CMOS	OSM General Purpose Input/output C4.
F4	GPIO_C_5 / DISP_BL_EN	P14_2_1V8	P14_2/ A13	IO, 1.8V CMOS	OSM General Purpose Input/output C5.
G3	CAM_PWR / GPIO_C_6	GPIO5	NA	O, 1.8V CMOS	OSM General Purpose Output C6.
G4	CAM_RST# / GPIO_C_7	GPIO6	NA	O, 1.8V CMOS	OSM General Purpose Output C7.

2.6.16Control Signals

OSM v1.1 specification supports Control Signals, for various purposes like resetting the Module, Powering ON/OFF the CPU, Enabling the Carrier Power, etc.

For more details on the Control Signals pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U17	SYS_RST#	SYS_RST#_1V8	NA	I, 1.8V CMOS	Hard RESET Input to SOM.
AA9	PWR_BTN#	PWR_BTN#	NA	I, 1.8V CMOS 10K PU	Power ON /OFF Input to SOM.
V17	CARRIER_PWR_EN	PMIC_PGOOD_1V8	NA	O, 1.8V CMOS	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.
AC18	DEBUG_EN	DEBUGEN_1V8	DEBUGEN	I, 1.8V CMOS	Debug Enable

2.6.17Vendor Defined

In the RZ/G2UL, RZ/FIVE or the RZ/A3UL OSMs, other than the OSM dedicated functionalities, some additional features are made available making use of the Vendor defined pins.

For more details on the Vendor Defined Contacts pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA29	Vendor Defined11	QSPI_RESET#	QSPI_RESET#/A7	I, MIPI	QSPI Reset
D7	Vendor Defined7	NMI	NMI/AA2	I, MIPI	CPU Interrupt
D6	Vendor Defined6	BSCANP	BSCANP/AE22	I, MIPI	Switches between normal operation and boundary scan test mode
C16	Vendor Defined2	AUDIO_CLK1	AUDIO_CLK1/A9	I, MIPI	Audio Clock1 – reference clock to be used when using Audio interface.
P16	Vendor Defined3	AUDIO_CLK2	AUDIO_CLK2/B8	I, MIPI	Audio Clock2 – reference clock to be used when using Audio interface.

2.6.18 Boot Media Selection

The RZ/G2UL, RZ/FIVE or the RZ/A3UL supports one Boot Select pin connected to BOOT_SEL0# Port of the OSM LGA that can be used to switch between boot media. The OSM supports booting from On-SOM eMMC, and Carrier QSPI. Any of these boot media can selected by properly setting the Boot Select Pins status from the carrier board as mentioned below.

BOOT_SEL0#	Description
GND	eMMC Flash (SDHI0)
Float	QSPI FLASH (SPIBSC)

Also, RZ/G2UL, RZ/FIVE or the RZ/A3UL OSM supports active low FORCE_RECOV# functionality as per OSM v1.1 specification. Pulling low this pin forces the MPU to serial download mode where the MPU boot media can be programmed using SCIF0, connected to the Console UART of OSM LGA.

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U19	BOOT_SEL0#	BOOT_SEL0#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 0
T17	FORCE_RECOVERY#	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Force Recovery

2.6.19Power and GND

The RZ/G2UL, RZ/FIVE and the RZ/A3UL works with 5V power input (VCC) from the OSM LGA and generates all other required powers internally On-SOM itself. The Module also supports coin cell power input (RTC_PWR) from OSM LGA to On-SOM RTC controller (Integrated in PMIC) for real time clock.

For more details on Power & GND Signals pinouts on OSM LGA, refer the below table.

Pin No.	OSM LGA Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y8, Y9, Y10, Y11, Y17 Y25, Y26, Y27, Y28	VCC_IN_5V	VCC_IN_5V	NA	I, 5V Power	Supply Voltage
M17	ETH_IOPWR	VCC_3V3	NA	O, 3V3 POWER	Voltage indicating the IO level of RGMII.
M19	VCC_2_TEST	VDD_1V1	NA	I,1V1 POWER	Module power voltage test point
Y16	VCC_3_TEST	VCC_3V3	NA	I, 3V3 POWER	Module power voltage test point
Y20	VCC_4_TEST	VCC_1V8	NA	I,1V8 POWER	Module power voltage test point
Y3	VCC_5_TEST	VDD_DDR_2V5	NA	I,2V5 POWER	Module power voltage test point
C5	VCC_6_TEST	VDD_PVDD_1	NA	I,3V3 POWER	Module power voltage test point
AA33	VCC_7_TEST	VDD_SD1	NA	I, SD1 POWER	Module power voltage test point
B29	VCC_8_TEST	VDD_SD0	NA	I, SD0 POWER	Module power voltage test point
D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21, A15, A17, A18, A19, A21, B15, B16, B17, B18, B19, B20, B21, A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10,	GND	GND	NA	Power	Ground.

Pin No.	OSM LGA Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA11, AB3, AB6, AB9, AC4, AC7, AC10, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33, A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, K34, M35, N34					
W17	RTC_PWR	VRTC_3V0	NA	I, 3V Power	3V coin cell input for RTC.

2.7 Other Features

2.7.1 Programming Header

The RZ/G2UL, RZ/FIVE or the RZ/A3UL OSM LGA Module supports 16 pin programming header for testing the on-module features. The programming header is used for Flashing the board and getting the boot prints.

Number of Pins - 16

Connector Part - 503480-1600 from Molex

For more details on the pinout of Programming Header, refer the below table.

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_IN_5V	NA	Power	Supply voltage
2	VCC_IN_5V	NA	Power	Supply voltage
3	VCC_IN_5V	NA	Power	Supply voltage
4	VCC_IN_5V	NA	Power	Supply voltage
5	VCC_IN_5V	NA	Power	Supply voltage
6	GND	NA	Power	Ground
7	USB0_DM	USB0_DM/AE6	IO, USB	USB OTG High Speed Data Positive
8	USB0_DP	USB0_DP/AD6	IO, USB	USB OTG High Speed Data Negative
9	GND	NA	Power	Ground
10	OTG1_VBUS	NA	I, Power	USB OTG VBUS power for detection.
11	GND	NA	Power	Ground
12	SCIF0_RXD	P6_3/AC1	O, 1.8V CMOS	Debug UART Receiver
13	SCIF0_TXD	P6_4/AC2	I, 1.8V CMOS	Debug UART Transmitter
14	GND	NA	Power	Ground
15	BOOT_SEL0#	NA	I, 1.8V CMOS	Boot selection media
16	FORCE_RECOV#	NA	I, 1.8V CMOS	Force Recovery

2.8 RZ/G2UL, RZ/FIVE and RZ/A3UL Pin Multiplexing on OSM BGA

The RZ/G2UL, RZ/FIVE and RZ/A3UL MPU IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of RZ/G2UL, RZ/FIVE and RZ/A3UL MPU's IO pins can be configured as GPIO if required. The below table provides the details of the MPUs pin connections to the OSM LGA and with selected pin function highlighted and available alternate functions. This table has been prepared by referring Renesas's Pin Function Table.

Important Note: It is strongly recommended to use the pin function same as selected in the OSM BGA for iWave's BSP reusability and to have compatible OSM modules in future for upgradability.

Blue	*Function available only in RZ/FIVE*
RED	*Function available in RZ/A3UL and RZ/Five*
GREEN	*Function available in RZ/A3UL & RZ/G2UL*

Table 4: RZ/G2UL, RZ/FIVE and RZ/A3UL MPU for OSM BGA interfaces

Interface/ Function	OSM Pin Number	MPU Pin Number	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	Default
ENET0	J15	M2	P1_0	ET0_TXC/TX_CLK	RSPI0_CK	CAN_CLK	MTIOC1A	SCIF2_TXD			ET0_TXC/TX_CLK
	K16	M1	P1_1	ET0_TX_CTL/TX_EN	RSPI0_MOSI	CAN0_TX	MTIOC1B	SCIF2_RXD			ET0_TX_CTL/TX_EN
	H15	L1	P1_2	ET0_TXD0	RSPI0_MISO	CAN0_RX	MTIC5U	SCIF2_SCK			ET0_TXD0
	G15	L2	P1_3	ET0_TXD1	RSPI0_SSL	CAN0_TX_DATARATE_EN	MTIC5V	SCIF2_CTS#			ET0_TXD1
	H16	K1	P1_4	ET0_TXD2		CAN0_RX_DATARATE_EN	MTIC5W	SCIF2_RTS#			ET0_TXD2
	G16	K2	P2_0	ET0_TXD3	SSI0_BCK	CAN1_TX	MTCLKA				ET0_TXD3
	R15	N3	P3_0	ET0_RXC/RX_CLK	SSI1_BCK	POE0#	MTIOC0A				ET0_RXC/RX_CLK

Interface/ Function	OSM Pin Number	MPU Pin Number	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	Default
	M15	N1	P3_1	ET0_RX_CTL/RX_DV	SSI1_RCK	POE4#	MTIOC0B				ET0_RX_CTL/RX_DV
	K15	P2	P3_2	ET0_RXD0	SSI1_TXD	POE8#	MTIOC0C				ET0_RXD0
	L15	R3	P3_3	ET0_RXD1	SSI1_RXD	POE10#	MTIOC0D				ET0_RXD1
	N15	R2	P4_0	ET0_RXD2	RSPI1_CK	MTIOC8A	MTIOC2A	USB1_VBUSEN			ET0_RXD2
	P15	R1	P4_1	ET0_RXD3	RSPI1_MOSI	MTIOC8B	MTIOC2B	USB1_OVRCUR			ET0_RXD3
	T15	T3	P4_3	ET0_MDC	RSPI1_SSL	MTIOC8D	MTIOC3B	CAN0_TX			ET0_MDC
	T16	T2	P4_4	ET0_MDIO			MTIOC3C	CAN0_RX			ET0_MDIO
QSPI	U16	B6	QSPI0_SPCLK								QSPI0_SPCLK
	U15	C7	QSPI0_IO0	SCIF3_TXD	SCIF1_TXD	MTIOC0A	SCI0_RXD				QSPI0_IO0
	V15	A5	QSPI0_IO1	SCIF3_RXD	SCIF1_RXD	MTIOC0B	SCI0_TXD				QSPI0_IO1
	W16	B7	QSPI0_IO2	CAN_CLK	SCIF1_SCK	MTIOC4A	USB1_VBUSEN				QSPI0_IO2
	W15	C6	QSPI0_IO3	CAN0_TX	SCIF1_CTS#	MTIOC4B	USB1_OVRCUR				QSPI0_IO3
	Y15	B5	QSPI0_SSL	CAN0_RX	SCIF1_RTS#	MTIOC4C					QSPI0_SSL
CAN0	AC17	AE2	P6_1	USB1_OVRCUR	RSPI2_MOSI	CAN0_TX	SCIF2_RXD	MTIOC7B			CAN0_TX
	AB17	AB2	P6_2	ADC_TRG	RSPI2_MISO	CAN0_RX	SCIF2_SCK	MTIOC7C		IRQ2	CAN0_RX
CAN1	AC19	B4	OM_SIO4	CAN1_TX	SCIF0_SCK	MTIC5U	SCI0_RXD	SCIF3_TXD			CAN1_TX
	AB19	A3	OM_SIO5	CAN1_RX	SCIF0_CTS#	MTIC5V	SCI0_TXD	SCIF4_SCK			CAN1_RX
USB 0	AC14	AD6	USB0_DP								USB0_DP
	AB13	AE6	USB0_DM								USB0_DM

Interface/ Function	OSM Pin Number	MPU Pin Number	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	Default
	AC16	AD3	P5_0	USB0_VBUSEN	SCIF2_TXD	MTIOC7A		CAN0_RX_DATARATE_EN			USB0_VBUSEN
	AC15	AE3	P5_2	USB0_OVRCUR	SCIF2_SCK	MTIOC7C	SSI2_BCK		ADC_TRG		USB0_OVRCUR
	AB14	AD2	P5_3	USB0_OTG_ID	SCIF2_CTS#	MTIOC7D	SSI2_RCK	USB1_VBUSEN	RIIC2_SDA		USB0_OTG_ID
USB 1	AC22	AD5	USB1_DP								USB1_DP
	AB23	AE5	USB1_DM								USB1_DM
	AC20	B22	P18_4	IRQ6	RSPI0_MISO	SCI0_RXD	USB1_VBUSEN	ADC_TRG	SCI1_TXD	SCIF4_RXD	USB1_VBUSEN
	AC21	AB3	P5_4	USB0_OTG_EXICEN	SCIF2_RTS#		SSI2_DATA	USB1_OVRCUR	RIIC2_SCL		P5_4
I2C	AA15	A19	RIIC1_SCL								RIIC1_SCL
	AA16	A20	RIIC1_SDA								RIIC1_SDA
	AA20	B19	RIIC0_SCL								RIIC0_SCL
	AA21	B20	RIIC0_SDA								RIIC0_SDA
SCIF2	A14	AC3	P5_1		SCIF2_RXD	MTIOC7B	ADC_TRG	SCI0_CTS#/RTS#	RSPI0_SSL	IRQ2	SCIF2_RXD
	B13	AD1	P6_0	USB1_VBUSEN	RSPI2_CK	CAN_CLK	SCIF2_TXD	MTIOC7A			SCIF2_TXD
SCIF1	D14	A11	P13_1	SCIF0_RXD		CAN0_TX	MTIOC4B	USB1_OVRCUR	DISP_DATA1	SCIF1_RXD	SCIF1_RXD
	D13	B10	P11_2	SSI0_TXD	POE8#	SCI1_SCK	RSPI2_MISO		DISP_DATA0	SCIF1_TXD	SCIF1_TXD
SCIF4	A22	B3	OM_SIO6	CAN1_TX_DATARATE_EN	SCIF0_RTS#	MTIC5W	SCI0_SCK	SCIF4_RXD			SCIF4_RXD
	B23	A2	OM_SIO7	CAN1_RX_DATARATE_EN	IRQ0	WDTOVF_PERROUT#	SCI0_CTS#/RTS#	SCIF4_TXD			SCIF4_TXD
SCIF3	C22	A4	OM_DQS	CAN0_RX_DATARATE_EN	SCIF0_RXD			SCIF3_RXD			SCIF3_RXD
	C23	B4	OM_SIO4	CAN1_TX	SCIF0_SCK	MTIC5U	SCI0_RXD	SCIF3_TXD			SCIF3_TXD

Interface/ Function	OSM Pin Number	MPU Pin Number	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	Default
SCIF0	D22	AC1	P6_3	RIIC2_SDA	RSPI2_SSL	CAN0_TX_DATARATE_EN	SCIF2_CTS#	MTIOC7D	SCIF0_RXD	IRQ3	SCIF0_RXD
	D23	AC2	P6_4	RIIC2_SCL		CAN0_RX_DATARATE_EN	SCIF2_RTS#	ADC_TRG	SCIF0_TXD	IRQ4	SCIF0_TXD
JTAG	N17	U2	TCK/SWDCLK								TCK/SWDCLK
	N19	U1	TMS/SWDIO								TMS/SWDIO
	P17	W1	TDI								TDI
	R17	V2	TDO								TDO
	R19	V1	TRST#								TRST#
ET1	H1	AE18	P7_0	ET1_TXC/TX_CLK	ADC_TRG	RSPI2_CK	CAN_CLK	MTIOC0A	SCIF2_TXD	IRQ5	ET1_TXC/TX_CLK
	J2	AD17	P7_1	ET1_TX_CTL/TX_EN	SCI1_SCK	RSPI2_MOSI	CAN0_TX	MTIOC0B	SCIF2_RXD		ET1_TX_CTL/TX_EN
	G1	AD16	P7_2	ET1_TXD0	SCI1_TXD	RSPI2_MISO	CAN0_RX	MTIOC0C	SCIF2_SCK		ET1_TXD0
	F1	AE16	P7_3	ET1_TXD1	SCI1_RXD	RSPI2_SSL	CAN0_TX_DATARATE_EN	MTIOC0D	SCIF2_CTS#		ET1_TXD1
	G2	AD15	P7_4	ET1_TXD2	SCI1_CTS#/RTS#	IRQ2	CAN0_RX_DATARATE_EN		SCIF2_RTS#		ET1_TXD2
	L1	AC18	P9_0	ET1_RX_CTL/RX_DV	RSSPI0_CK		SSI2_BCK	MTIOC4A	SCIF4_SCK		ET1_RX_CTL/RX_DV
	J1	AE19	P9_1	ET1_RXD0	RSPI0_MOSI		SSI2_RCK	MTIOC4B	SCIF4_RXD		ET1_RXD0
	K1	AD19	P9_2	ET1_RXD1	RSPI0_MISO		SSI2_DATA	MTIOC4C	SCIF4_TXD		ET1_RXD1
	M1	AE20	P9_3	ET1_RXD2	RSPI0_SSL	IRQ3		MTIOC4D	IRQ1		ET1_RXD2
	N1	AD20	P10_0	ET1_RXD3	SSI0_BCK	IRQ4		MTIOC6A	IRQ2		ET1_RXD3
	C6	AC20	P10_2	ET1_MDC	SSI0_TXD	SSI3_RCK		MTIOC6C			ET1_MDC
	C7	AE21	P10_3	ET1_MDIO	SSI0_RXD	SSI3_TXD	USB1_VBUSEN	MTIOC6D			ET1_MDIO
	F2	AE15	P8_0	ET1_TXD3	SCIF0_SCK	SCIF1_RXD	SSI1_BCK	SCI0_SCK	MTIOC7A	IRQ1	ET1_TXD3
	P1	AC17	P8_4	ET1_RXC/RX_CLK	SCIF0_RTS#				ADC_TRG	RSPI2_SSL	ET1_RXC/RX_CLK
RGB	K3	B9	P11_0	SSI0_BCK	POE0#	SCI1_RXD	RSPI2_CK		DISP_HSYNC		DISP_HSYNC
	J4	C9	P11_1	SSI0_RCK	POE4#	SCI1_TXD	RSPI2_MOSI		DISP_DE		DISP_DE

Interface/ Function	OSM Pin Number	MPU Pin Number	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	Default
	Y7	B11	P13_0	SCIF0_TXD		CAN_CLK	MTIOC4A	USB1_VBUSEN	DISP_DATA2		DISP_DATA2
	M4	A10	P11_3	SSI0_RXD	POE10#	SCI1_CTS#/RTS#	RSPI2_SSL		DISP_CLK		DISP_CLK
	L3	C10	P12_0	IRQ0	SCI0_RXD		MTIOC0A	SCIF3_TXD	DISP_VSYNC		DISP_VSYNC
	Y4	C13	P14_0	SCIF1_TXD		CAN1_TX	MTIC5U	SCI0_RXD	DISP_DATA7		DISP_DATA7
	Y6	B12	P13_3	SCIF0_CTS#		CAN0_TX_DATARATE_EN	MTIOC4D		DISP_DATA4		DISP_DATA4
	AA6	A12	P13_4	SCIF0_RTS#		CAN0_RX_DATARATE_EN			DISP_DATA3		DISP_DATA3
	W4	A14	P16_0	SCIF1_CTS#		CAN1_RX_DATARATE_EN		SCI0_CTS#/RTS#	DISP_DATA10		DISP_DATA10
	Y5	C12	P13_2	SCIF0_SCK		CAN0_RX	MTIOC4C		DISP_DATA6		DISP_DATA6
	AA5	C11	P12_1	IRQ1	SCI0_TXD		MTIOC0B	SCIF3_RXD	DISP_DATA5		DISP_DATA5
	V3	C14	P15_0	RSPI0_CK			IRQ4	MTIOC8A	DISP_DATA11		DISP_DATA11
	U3	C15	P15_1	RSPI0_MOSI			IRQ5	MTIOC8B	DISP_DATA13		DISP_DATA13
	V4	B14	P16_1	SCIF1_RTS#					DISP_DATA12		DISP_DATA12
	T4	F16	P18_0	IRQ2	ADC_TRG			SCI0_SCK	DISP_DATA15	SCIF3_SCK	DISP_DATA15
	R3	B16	P17_1	RSPI1_MOSI	SSI1_RCK	CAN1_RX	MTIOC3B		DISP_DATA19		DISP_DATA19
	N4	C17	P17_3	RSPI1_SSL	SSI1_RXD	CAN1_RX_DATARATE_EN	MTIOC3D		DISP_DATA22		DISP_DATA22
	P3	A17	P18_1	IRQ3			SCIF3_SCK	SCI0_TXD	DISP_DATA20	SCIF3_RXD	DISP_DATA20
	T3	A15	P15_3	RSPI0_SSL			IRQ7	MTIOC8D	DISP_DATA14		DISP_DATA14
	R4	A16	P17_2	RSPI1_MISO	SSI1_TXD	CAN1_TX_DATARATE_EN	MTIOC3C		DISP_DATA18		DISP_DATA18
	M3	C20	P18_3	IRQ5	RSPI0_MOSI	SCI0_TXD	SCIF3_TXD	SCI0_CTS#/RTS#	DISP_DATA23	SCIF4_SCK	DISP_DATA23

Interface/ Function	OSM Pin Number	MPU Pin Number	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	Default
	N3	B17	P18_2	IRQ4	RSPI0_CK	SCI0_SCK	SCIF3_RXD	SCI0_RXD	DISP_DATA21	SCIF3_TXD	DISP_DATA21
	J3	B1	P0_0	SD0_CD		RIIC3_SDA	MTIOC2A	SCI0_TXD	IRQ2		P0_0
RSPI	Y21	K6	P2_1	ET0_TX_ER R	SSI0_RCK	CAN1_RX	MTCLKB	SCI0_SCK	RSPI0_CK		RSPI0_CK
	Y23	M3	P2_2	ET0_TX_C OL	SSI0_TXD	CAN1_TX_DAT ARATE_EN	MTCLKC	SCI0_TXD	RSPI0_MOSI		RSPI0_MOSI
	Y22	M6	P2_3	ET0_TX_CR S	SSI0_RXD	CAN1_RX_DAT ARATE_EN	MTCLKD	SCI0_RXD	RSPI0_MISO		RSPI0_MISO
	AA23	A21	P18_5	IRQ7	RSPI0_SSL	SCI0_CTS#/RT S#	USB1_OVRCU R		SCI1_RXD	SCIF4_TXD	RSPI0_SSL
SD1	F21	G2	SD1_CLK								SD1_CLK
	E20	H6	SD1_CMD	SSI0_BCK	POE0#	SCI1_RXD	RSPI2_CK	SSI3_BCK			SD1_CMD
	G20	H2	SD1_DAT A0	SSI0_RCK	POE4#	SCI1_TXD	RSPI2_MOSI	SSI3_RCK			SD1_DATA0
	G21	J3	SD1_DAT A1	SSI0_TXD	POE8#	SCI1_SCK	RSPI2_MISO	SSI3_TXD			SD1_DATA1
	H20	J1	SD1_DAT A2	SSI0_RXD	POE10#	SCI1_CTS#/RT S#	RSPI2_SSL	SSI3_RXD			SD1_DATA2
	H21	J2	SD1_DAT A3								SD1_DATA3
	J21	D3	P0_2	SD1_CD		MTIOC1A	RIIC2_SDA	USB1_VBUS EN	IRQ4	IRQ0	SD1_CD
	D20	C3	P0_3	SD1_WP		MTIOC1B	RIIC2_SCL			IRQ1	SD1_WP
CSI	B3	AE11	CSI_CLKN/ NC								CSI_CLKN/NC
	B4	AD11	CSI_CLKP/ NC								CSI_CLKP/NC
	C1	AE12	CSI_DATA 0_N/NC								CSI_DATA0_N /NC
	B1	AD12	CSI_DATA 0_P/NC								CSI_DATA0_P/ NC

Interface/ Function	OSM Pin Number	MPU Pin Number	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	Default
	A2	AE10	CSI_DATA1_N/NC								CSI_DATA1_N/NC
	A3	AD10	CSI_DATA1_P/NC								CSI_DATA1_P/NC
	A6	AD13	CSI_DATA2_P / ADC_CH1								CSI_DATA2_P / ADC_CH1
	A5	AE13	CSI_DATA2_N/ ADC_CH0								CSI_DATA2_N / ADC_CH0
	B6	AE9	CSI_VDD18/NC								
	B7	AD9	CSI_VDD18/NC								
GPIO	K17	N2	P4_2	ET0_RX_ERR	RSPI1_MISO	MTIOC8C	MTIOC3A	CAN_CLK			P4_2
	L17	B15	P15_2	RSPI0_MISO			IRQ6	MTIOC8C	DISP_DATA16	SCI1_TXD	P15_2
	D19	B13	P14_1	SCIF1_RXD		CAN1_RX	MTIC5V	SCI0_TXD	DISP_DATA9	IRQ2	P14_1
	F3	P1	P4_5	ET0_LINKSTA			MTIOC3D	CAN0_TX_DATARATE_EN			P4_5
	F4	A13	P14_2	SCIF1_SCK	ADC_TRG	CAN1_TX_DATARATE_EN	MTIC5W	SCI0_SCK	DISP_DATA8	IRQ3	P14_2

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Renesas RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the five VCC_IN_5V in Size-M Module and returned through the numerous GND pins on the connector.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Renesas RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module.

Table 5: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_IN_5V [1]	4.5	5	5.5	±50mV
2	VDD_RTC [2]	2.8V	3V	3.3V	±20mV

3.1.2 Power Consumption

TBD

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module.

Table 6: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]For more information on Thermal solution & Heat sink/ Heat Spreader, refer the following section.

3.2.2 Heat Sink/ Heat Spreader

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Heat spreader acts as thermal coupling device between Module and external thermal solution. Heat spreader also provides thermal coupling to SoC via gap filler for better heat exchange. Heat spreader is not a complete thermal solution by itself. Heat spreader has to be used with application specific thermal solutions like heat sinks, Chassis, fans, Heat pipes etc.

Note: iWave supports Heat Sink/ Heat Spreader Solution for Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module. For more information on Heat Sink/ Heat Spreader contact iWave support team. Do not Power On the SOM without a proper thermal solution.

3.2.3 RoHS Compliance

iWave's Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Renesas RZ/G2UL, RZ/FIVE and RZ/A3UL OSM LGA Module variants. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 7: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G53M - Renesas RZ/G2UL, RZ/FIVE and RZ/A3UL OSM		
iW-G53M-OMUL-4D002G-E016G-BIA	RZ/G2UL CPU, 2GB LPDDR4, 16GB eMMC based OSM	-40°C to 85°C
iW-G53M-OMA3-4D001G-E008G-BIA	RZ/A3UL CPU, 1GB LPDDR4, 8GB eMMC based OSM	-40°C to 85°C
iW-G53M-OMFV-4D001G-E008G-BIA	RZ/FIVE CPU, 1GB LPDDR4, 8GB eMMC based OSM	-40°C to 85°C

Note:

** Some Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.*

** For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM.*

** Please contact iWave for other RAM and eMMC Configurations.*

5. APPENDIX

5.1 Renesas RZ/G2UL, RZ/FIVE and RZ/A3UL SBC

iWave Systems supports iW-RainboW-G53S Renesas's RZ/G2UL, RZ/FIVE and RZ/A3UL SBC which is targeted for quick prototyping and testing of the MPU features. The SBC being based on OSM they can also act as a development platform for the quick validation and testing of the OSM and its features. Being a PICO-ITX form factor with 85mm x 56mm size, the OSM Development Platform is highly packed with all necessary interfaces & on-board connectors to validate complete OSM supported features.

For more details on RZ/G2UL, RZ/A3UL or the RZ/FIVE SOM and SBC, visit the below web link:

https://www.iwavesystems.com/product/renesas-rz-g2ul-rz-a3ul-rz-five-based-osm-mf-lga-module/