iW-RainboW-G50S

i.MX 93 or i.MX 91 Pico ITX Single Board Computer

Hardware User Guide

Embedding Intelligence

DRAFT VERSION SUBJECT TO CHANGE

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Pico ITX Single Board Computer based on the NXP's i.MX 93 or i.MX 91 Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 93 Pico ITX SBC from a Hardware Systems perspective.

1.2 Pico ITX SBC Overview

The Pico ITX is a versatile small form factor SBC (Single Board Computer) definition targeting application that require low power, low costs, and high performance. The SBCs are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE, LVDS and MIPI display connectors are concentrated on the SBC.

NXP's i.MX 93 or i.MX 91 SoC based Pico ITX Single Board computer is rich with i.MX 93 or i.MX 91 features along with eMMC, Dual Ethernet PHY, USB2.0 Hub, Wi-Fi & BT module and comes in compact 100mm x 72mm form factor.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group

Acronyms	Abbreviations
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
OTG	On-The-Go
PCB	Printed Circuit Sheet
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SBC	Single Board Computer
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on SBC.

1.5 References

- IMX93IEC_Rev_x.pdf
- IMX91PEC_Revx
- i.MX93RM Rev_x.pdf

1.6 Important Note

In this document, wherever i.MX 93 or i.MX 91 SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_9)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO1_9*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 93 or i.MX 91 Pico ITX SBC features and Hardware architecture with high level block diagram.

2.1 i.MX 93 or i.MX 91 Pico ITX SBC Block Diagram

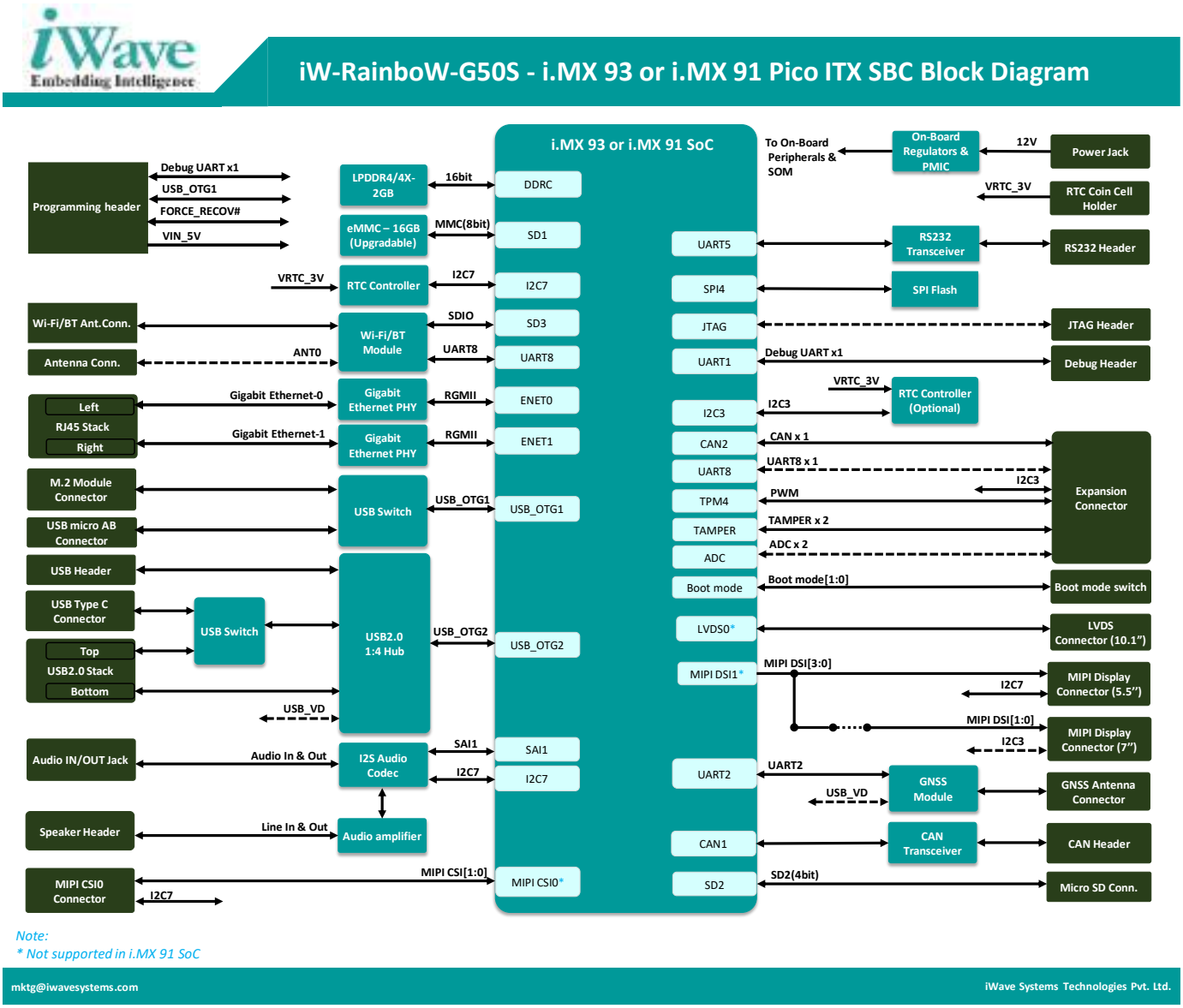

Figure 1: i.MX 93 or i.MX 91 Pico ITX SBC Block Diagram

2.2 i.MX 93 or i.MX 91 Pico ITX SBC Features

i.MX 93 or i.MX 91 Pico ITX SBC supports the following features.

SoC

- i.MX 93 Processor[1]
  - i.MX 9352: 2 x Cortex-A55@1.7GHz ,1 x M33 core@250MHz, NPU
  - i.MX 9351: 1 x Cortex-A55@1.7GHz ,1 x M33 core@250MHz, NPU
  - i.MX 9332: 2 x Cortex-A55@1.7GHz ,1 x M33 core@250MHz
  - i.MX 9331: 1 x Cortex-A55@1.7GHz ,1 x M33 core@250MHz
- i.MX 91 Processor
  - i.MX 91: 1x Cortex®-A55, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0

Power

- PCA9451 PMIC

Memory

- LPDDR4X - 2GB[2,3]
- eMMC Flash - 16GB (Expandable)[2]
- Micro SD slot
- 16Mb SPI Flash[4]

Network & Communication

- IEEE 802.11a/b/g/n/ac/ax+ Bluetooth 5.3+ IEEE802.15.4[4]
- Gigabit Ethernet PHY Transceiver with RJ45 Magjack Connector x 2
- USB 2.0 x 2 (Dual stack type-A connector)
- USB 2.0 OTG port through micro–AB Receptacle Connector
- USB Type-C Connector
- RS232 x 1
- CAN x 1
- GNSS Module (Optional)

Audio/Video Features

- 40pin, LVDS Display Connector*
- USB Touch Header
- I2S Audio Codec
- 3.5mm Audio IN/OUT
- Speaker out header
- 36pin MIPI_CSI Camera Connector*

- 39pin, 4 Lane MIPI_DSI Display Connector *[5]
- 15pin, 2 Lane MIPI_DSI Display Connector (Optional) *[5]

Expansion Connector Interfaces

- CAN x 1 Port
- PWM x 1
- I2C x 1
- GPIO x 1
- ADC x 2 [7]
- UART x 1 Port (Optional)[6]
- Tamper x 2[7] (Optional)

Miscellaneous Interfaces

- Debug UART Header
- JTAG Header
- RTC Battery Connector
- M.2-Key B Connector
    - USB 2.0 x 1

General Specification

- Power Supply : 12V, 2A[8]
- Form Factor : 100mm X 72mm
- Temperature Support : -40°C to +85°C (Industrial Grade)
- Environment Specification : RoHS2 and REACH Compliance

1. *There are four configurations of i.MX 93 Processor, hence this document is used to represent either of one based on SOM Part Number.*
2. *Memory Size will differ based on iWave's SBC Product Part Number.*
3. *i.MX 93 SBC supports LPDDR4X by default and i.MX 91 SBC supports LPDDR4.*
4. *SPI4 is shared between Wi-Fi/BT module to support IEEE802.15.4 and SPI Flash. If Wi-Fi/BT is required, SPI Flash is not supported. If SPI is required, Wi-Fi/BT module will be made DNP.*
5. *By default, 4 Lane MIPI_DSI Display is supported.*
6. *UART8 is muxed with Bluetooth Module and Expansion Connector. By default, it is connected to Bluetooth module.*
7. *Tamper and ADC signals are muxed. By default, ADC signals are available in the Expansion Connector.*
8. *The i.MX 93 SBC can support wide range input power from 7V to 24V. By default, it is designed to support 12V.*

** Not supported in i.MX 91 SoC.*

2.3 CPU

iW-RainboW-G50S i.MX 93 or i.MX 91 Pico ITX SBC can support different i.MX 93 or i.MX 91 SoCs from NXP.

2.3.1 i.MX 93 CPU

The i.MX 93 (11 x 11 mm) Family consists of 4 processors.

- i.MX 9352: 2x Cortex®-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9351: 1 x Cortex-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9332: 2x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9331: 1x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM

The i.MX 93 includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing. Memory interfaces supporting 16-bit LPDDR4/LPDDRX, eMMC 5.1, SD 3.0 and a wide range of peripheral IOs providing wide flexibility.

Figure 2: i.MX 93 SoC Block Diagram

2.3.2 i.MX 91 CPU

The i.MX 91 (11 x 11 mm) Family consists of two processors.

- i.MX 91P1C: Industrial Grade
- i.MX 91P1D: Consumer Grade

The i.MX 91 includes powerful single Arm® Cortex®-A55 processor with speeds up to 1.4 GHz. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbps Ethernet controllers, drive gateway applications with low latency. Memory interfaces supporting 16-bit LPDDR4, eMMC 5.1, SD 3.0 and a wide range of peripheral IOs providing wide flexibility.

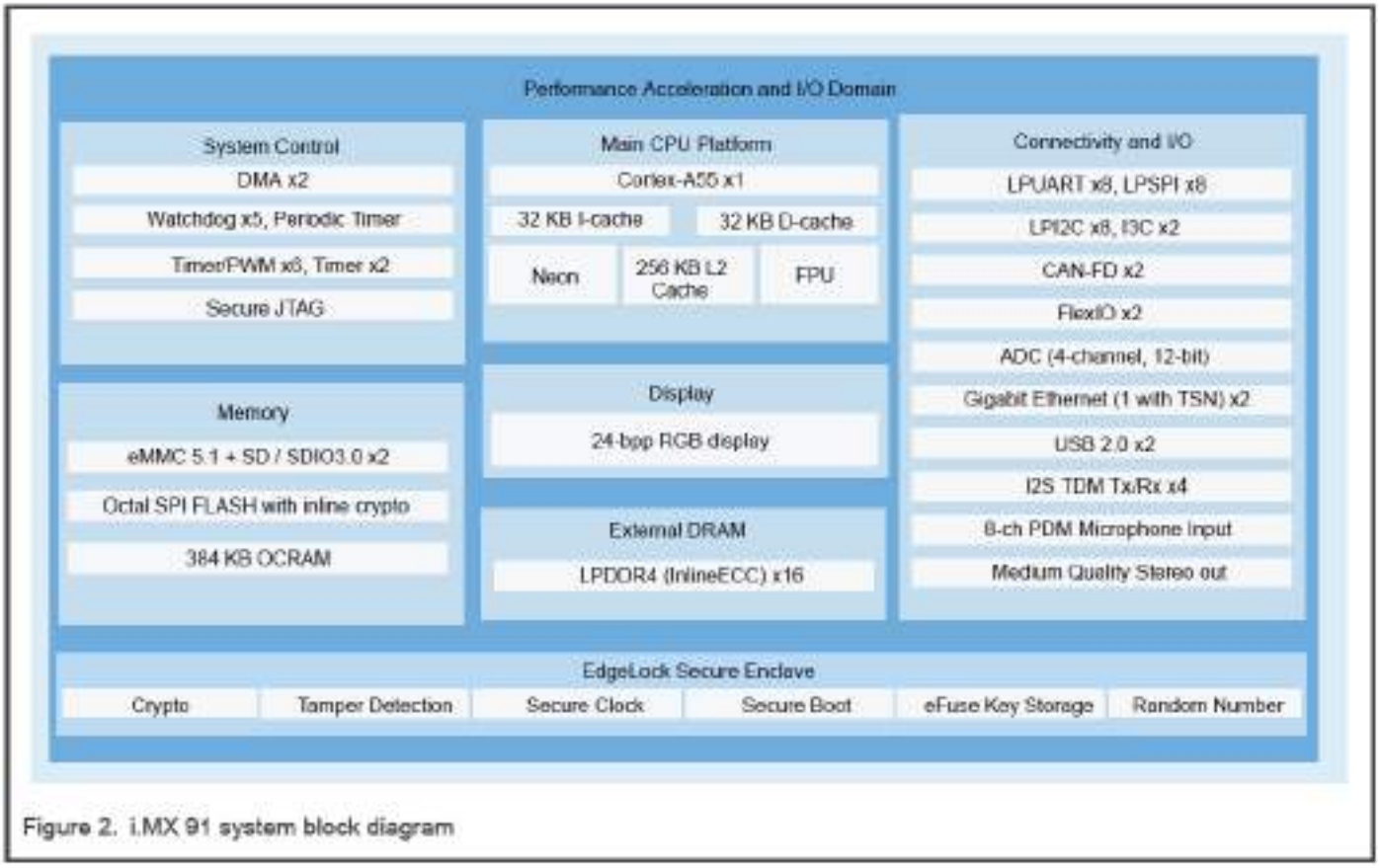

Figure 3: i.MX 91 SoC Block Diagram

Note: The i.MX 93 and i.MX 91 processor offers numerous advanced features, please refer the latest i.MX 93 or i.MX 91 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PMIC

The i.MX 93 or i.MX 91 Pico ITX SBC uses one PCA9451 PMIC (U4) for module power management. The PCA9451 features six high efficiency step-down regulators and three linear regulators. The PCA9451 is a single chip Power Management IC (PMIC) specifically designed to support i.MX 93x family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5V adapter non-portable applications. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PCA9451 PMIC comes in 56-pin HVQFN package and is placed on the Top side of the SBC.

2.5 Memory

2.5.1 LPDDR4X/LPDDR4

The i.MX 93 or i.MX 91 Pico ITX SBC supports 2GB RAM by using 16bit 2GB LPDDR4 IC connected to DDR_CH0 channel of the SoC. By default, LPDDR4X is supported in i.MX 93 SBC. The i.MX 91 SoC supports only LPDDR4. LPDDR4 part U9 is placed on Top side of the SBC. To customize the LPDDR4/4X memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 93 or i.MX 91 Pico ITX SBC supports 16GB eMMC as default boot and storage device. This is directly connected to eMMC controller of the i.MX 93 or i.MX 91 SoC and operates at 1.8V (IO supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory (U2) is physically located on Top side of the SBC. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD connector

The i.MX 93 or i.MX 91 Pico ITX SBC supports Micro SD slot which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J26) is directly connected to the uSDHC2 controller of the i.MX 93 or i.MX 91 SoC. The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 93 Pico ITX SBC supports configurable I/O voltage levels for uSDHC2 lines through SD2_VSELECT. If SD2_VSELECT is set to low, then 3.3V IO level is selected for uSDHC2 lines. If SD2_VSELECT is set to high, then 1.8V IO level is selected for uSDHC2 lines. The Micro-SD Connector is physically located on bottom side of the i.MX 93 or i.MX 91 Pico ITX SBC as shown below.

Figure 4: Micro SD Card Connector

2.5.4 SPI Flash

The i.MX 93 or i.MX 91 Pico ITX SBC supports SPI Flash through i.MX 93 or i.MX 91 SoC's SPI4 interface. This SPI interface signals are connected to SPI Flash "IS25WP016D-JNLE" and operating at 1.8V Level.

Note: SPI4 is shared between Wi-Fi/BT module to support IEEE802.15.4 and OSM. If Wi-Fi/BT is required, SPI Flash is not supported. If SPI Flash is required, Wi-Fi/BT module will be made DNP.

2.6 Boot Media Setting

i.MX 93 or i.MX 91 SoC boot process begins at Power on Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. i.MX 93 or i.MX 91 SoC Boot ROM code uses the state of the internal register BOOT_MODE [3:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device.

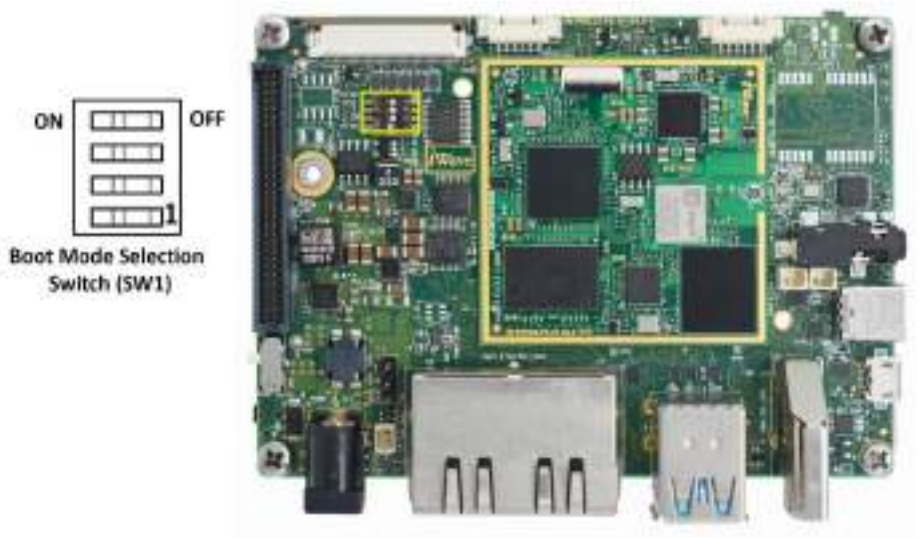

Figure 5: Boot Media Switch

Table 3: Boot Media Settings

Boot Media	Pin number	SW1 (4 Position Switch)	Pin number	SW1 (4 Position Switch)
		POS1		POS2
From Internal fuses	1	ON	2	ON
eMMC	1	ON	2	OFF
Serial Download mode	1	OFF	2	ON
SD Boot	1	OFF	2	OFF

2.7 Network & Communication

2.7.1 Wi-Fi and Bluetooth Interface

The i.MX 93 or i.MX 91 Pico ITX SBC is integrated with Murata's "LBES5PL2EL-SMP" based Wi-Fi+Bluetooth module. LBES5PL2EL-SMP module is complained with IEEE802.11a/b/g/n/ac/ax, SISO, Bluetooth specification v5.3 and IEEE802.15.4. It supports standard SDIO3.0 interface for WLAN, UART interfaces support for Bluetooth is Host Controller Interface (HCI) and SPI interface optionally supports for IEEE802.15.4. Connection to a host processor is through SDIO and High-Speed UART interfaces. The i.MX 93 or i.MX 91 Pico ITX SBC uses processor's UART8 interface for Bluetooth and SD3 interface for Wi-Fi. In the SBC, antenna pins of LBES5PL2EL-SMP Bluetooth and Wi-Fi is connected to J1 connector and optionally connected to J5 connector in the SBC.

Note: SPI4 is shared between Wi-Fi/BT module to support IEEE802.15.4 and OSM. If Wi-Fi/BT is required, SPI Flash is not supported. If SPI Flash is required, Wi-Fi/BT module will be made DNP.

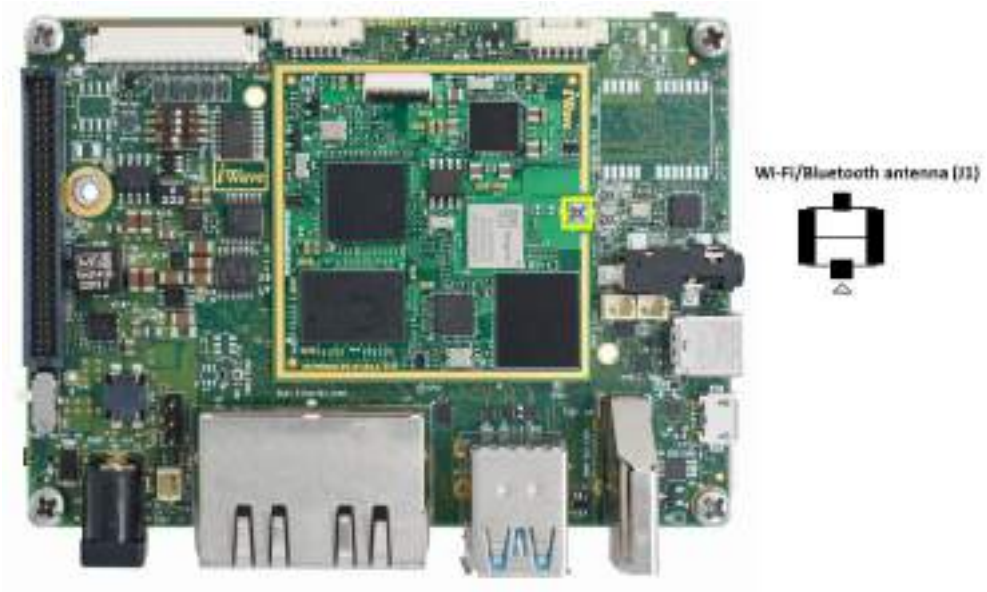

Figure 6: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata.

Antenna Part Number - : 2042811100 from Molex

2.7.2 Gigabit Ethernet Interface

The i.MX 93 or i.MX 91 Pico ITX SBC supports Dual Ethernet Port interface through dual external Ethernet PHY from Atheros, Qualcomm which supports 10/100/1000Mbps Ethernet.

The Ethernet PHY AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary Smart EEE. The Smart EEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

The Ethernet PHY's output signals GBE0 and GBE1 are directly connected to RJ45 Magjack (J17), Left & Right connector respectively. Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. The RJ45 Magjack combo connector is physically located at the top of the board as shown below.

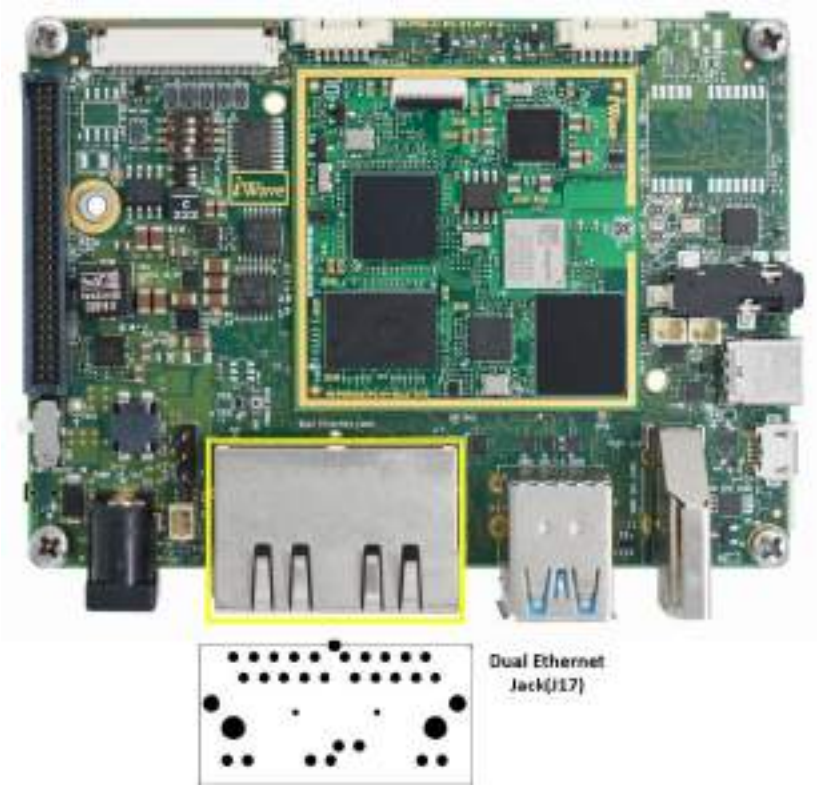

Figure 7: Dual RJ45 Magjack

2.7.3 USB2.0 OTG Interface

The i.MX 93 or i.MX 91 Pico ITX SBC supports USB2.0 OTG interface. This USB2.0 signals is muxed between USB2.0 Micro AB connector (J14) and M.2 key B connector(J28). USB2.0 Micro AB connector or M.2 key B connector can be selected by making the select pin of the USB switch high or low using 3 pin header(J27).

This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status.

This USB2.0 OTG connector is physically located at the top of the board as shown below.

Figure 8: USB OTG Connector

Figure 9: USB Switch Header

Table 4: USB Switch Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC	VCC_1V8	O, 1V8 Power	1V8 Supply Voltage.
2	S	USB2.0_SWITCH	I, 1V8	USB Select pin. High – USB OTG will be selected (default)

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Low – USB through M.2 Connector can be supported
3	GND	GND	Power	Ground.

2.7.4 GNSS Module (Optional)

The i.MX 93 or i.MX 91 Pico ITX SBC optionally supports u-blox's "NEO-M8Q-01A" based GNSS module. The NEO-M8Q-01A module is built on the exceptional performance of the u-blox M8 GNSS engine in the industry proven NEO form factor. It utilizes concurrent reception of up to three GNSS systems (GPS/Galileo together with BeiDou or GLONASS) for more reliable positioning.

The NEO-M8Q-01A provides high sensitivity and minimal acquisition times while maintaining low system power. The NEO-M8Q-01A combines a high level of robustness and integration capability along with flexible connectivity options via USB, I2C UART and SPI.

The i.MX 93 or i.MX 91 Pico ITX SBC makes use of the UART2 interface. The Antenna pin of the module can be connected to the J2 Antenna connector through an Active or Passive Path as per the requirement.

Figure 10: GNSS Antenna Connector

Connector Part Number: 734120110 from Molex.

Antenna Part Number : TBD

2.7.5 USB2.0 Host Port

The i.MX 93 or i.MX 91 Pico ITX SBC supports either USB Type C connector (J12) or top port of Dual stack USB2.0 Type A connector (J19) for OTG as Host only support.

The selection between USB Type C connector and top port of dual stack USB2.0 Type A connector can be done by setting the 4th bit of Boot media switch (SW1) to appropriate position. If the 4th bit of Board configuration switch (SW1) is set to OFF position, then USB Type C connector can be used. If the 4th bit of Board configuration switch (SW1) is set to ON position, then top port of dual stack USB2.0 Type A connector can be used.

Figure 11: USB2.0 Host-Top Port & type-C Connector

i.MX 93 or i.MX 91 SBC directly supports bottom port of dual stack USB2.0 Type A connector (J19).

Figure 12: USB2.0 Host-Bottom Port

2.7.6 CAN Interface

The i.MX 93 or i.MX 91 Pico ITX SBC supports Flexible Control Area Network (FLEXCAN) Port. The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol, and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads.

CAN1 of i.MX 93 or i.MX 91 SoC is connected to MCP2562FD-E/SN CAN Transceiver and CANL & CANH of the transceiver are connected to J23 (CAN1) Header which is placed on bottom side of the Board.

Number of Pins : 6

Connector Part Number : 532610671 from Molex

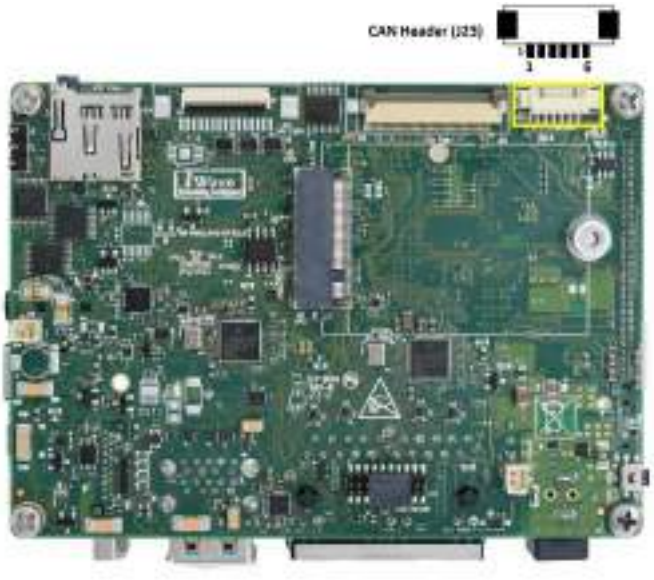

Figure 13: CAN Header

Table 5: CAN Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V_CAN0	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	NC.
3	CANL	CAN0_L	IO, DIFF	CAN Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN0_H	IO, DIFF	CAN High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.8 Serial Interface Features

2.8.1 Debug UART Interface

The i.MX 93 or i.MX 91 Pico ITX SBC supports debug interface through i.MX 93 or i.MX 91 SoC's UART1 interface. This UART1 signals from the SoC is connected to Debug UART header(J13) through 1.8V to 3.3V level Translator. This Debug UART header can be used for Debug purpose, which is physically located at the top of the board as shown below.

Number of Pins : 3

Connector Part number : M20-9990345 from Harwin

USB to UART Cable : TTL-232R-RPI from FTDI

Figure 14: Debug UART Header

Table 6: Debug UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	TX	UART1_RXD	O, 3.3V CMOS	UART interface Receive signal.
2	RX	UART1_TXD(BOOT_MODE0)	I, 3.3V CMOS	UART interface Transmit signal.
3	GND	GND	Power	Ground.

2.8.2 RS232 Data UART Interface

The i.MX 93 or i.MX 91 Pico ITX SBC supports RS232 with hardware flow control (CTS/RTS) through i.MX 93 SoC's UART5 interface. By default, this UART5 signals from the SoC is connected to "MAX3232" RS-232 Line Driver and Receiver via 1.8V to 3.3V level Translator. The RS232 Signals are connected from MAX3232 to RS232 Header(J1), which is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 532610671 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

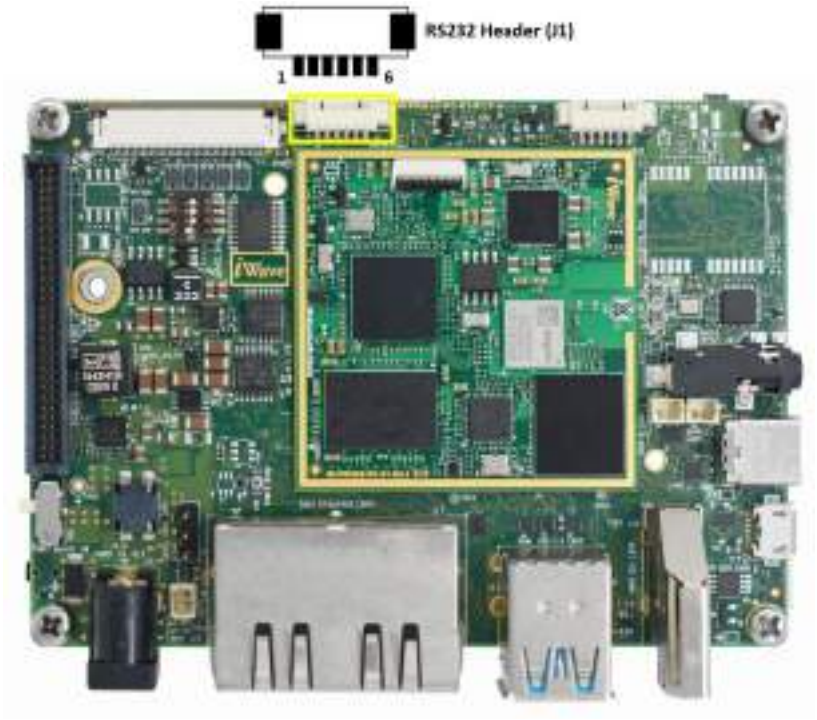

Figure 15: RS232 Header

Table 7: RS232 Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS	RS232_CTS	O, RS232	RS232 interface Clear to Send signal.
3	VCC	VCC_3V3	O, 3.3V Power	NC *Optional 3.3V Supply Voltage.*
4	TXD	RS232_RXD	I, RS232	RS232 interface Receive signal.
5	RXD	RS232_TXD	O, RS232	RS232 interface Transmit signal.
6	RTS	RS232_RTS	I, RS232	RS232 interface Ready to Send signal.

2.9 Audio/Video Features

2.9.1 MIPI CSI Interface (Not available in i.MX 91)

The i.MX 93 Pico ITX SBC supports one 2-lane MIPI CSI-2 camera input complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2. It supports up to 2 Rx data lanes (plus 1 Rx clock lane) and 80 Mbps -1.5 Gbps per lane data rate in high-speed operation. It also supports 10 Mbps data rate in low power operation.

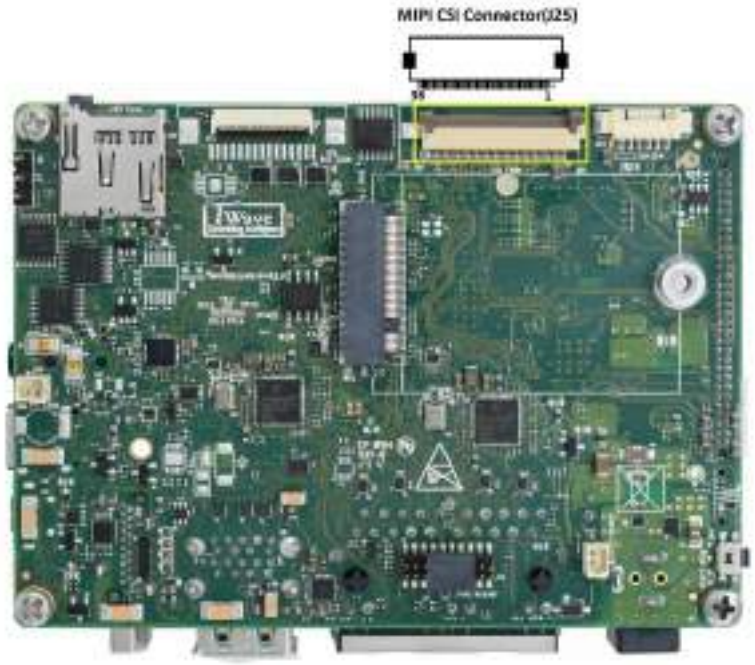

Figure 16: 36 pin MIPI CSI Connector

Number of Pins : 36

Connector Part : FH12A-36S-0.5SH(55) from Hirose Electric Co Ltd

Table 8: MIPI CSI Connector Pinouts

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
2	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
3	CAM0_CSI_D0+	MIPI_CSI1_D0_P	I, MIPI	MIPI CSI differential data lane 0 positive.
4	CAM0_CSI_D0-	MIPI_CSI1_D0_N	I, MIPI	MIPI CSI differential data lane 0 negative.
5	GND	GND	Power	Ground.
6	CAM0_CSI_D1+	MIPI_CSI1_D1_P	I, MIPI	MIPI CSI differential data lane 1 positive.
7	CAM0_CSI_D1-	MIPI_CSI1_D1_N	I, MIPI	MIPI CSI differential data lane 1 negative.
8	GND	GND	Power	Ground.

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
9	CAM0_CSI_D2+	NC	I, MIPI	MIPI CSI differential data lane 2 positive.
10	CAM0_CSI_D2-	NC	I, MIPI	MIPI CSI differential data lane 2 negative.
11	CAM0_RST#	CAM_RST(GPIO_IO23)	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal
12	CAM0_CSI_D3+	NC	I, MIPI	MIPI CSI differential data lane 3 positive.
13	CAM0_CSI_D3-	NC	I, MIPI	MIPI CSI differential data lane 3 negative.
14	GND	GND	Power	Ground.
15	CAM0_CSI_CLK+	MIPI_CSI1_CLK_P	I, MIPI	MIPI CSI differential Clock positive.
16	CAM0_CSI_CLK-	MIPI_CSI1_CLK_N	I, MIPI	MIPI CSI differential Clock negative.
17	GND	GND	Power	Ground.
18	CAM0_I2C_CLK	I2C7_SCL(GPIO_IO07)	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI Camera.
19	CAM0_I2C_DAT	I2C7_SDA(GPIO_IO06)	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI Camera.
20	CAM0_ENA#	NC	I, 1.8V CMOS	NC.
21	MCLK	NC	I, 1.8V CMOS	NC.
22	CAM1_ENA#	NC	I, MIPI/10K PU	NC.
23	CAM1_I2C_CLK	I2C7_SCL(GPIO_IO07)	I, 1.8V OD/ 4.7K PU	I2C clock Optional
24	CAM1_I2C_DAT	I2C7_SDA(GPIO_IO06)	IO, 1.8V OD/ 4.7K PU	I2C Data Optional
25	GND	GND	Power	Ground.
26	CAM1_CSI_CLK+	NC	I, MIPI	NC.
27	CAM1_CSI_CLK-	NC	I, MIPI	NC.
28	GND	GND	Power	Ground.
29	CAM1_CSI_D0+	NC	-	NC.
30	CAM1_CSI_D0-	NC	-	NC.
31	CAM1_RST#	NC	I, MIPI/10K PU	NC.
32	CAM1_CSI_D1+	NC	-	NC.
33	CAM1_CSI_D1-	NC	-	NC.
34	GND	GND	Power	Ground.
35	CAM0_GPIO	NC	-	NC.
36	CAM1_GPIO	NC	-	NC.

2.9.2 LVDS Interface (Not available in i.MX 91)

The i.MX 93 SoC has LVDS Display Bridge which provides connectivity to relevant devices-Displays with LVDS receivers, arranging the data as required by the external display receiver and by LVDS display standards.

The i.MX 93 Pico ITX SBC supports 40-pin LVDS display connector(J4) which is located at top side of the board as shown.

Number of Pins : 40

Connector Part : 541044033 from Molex

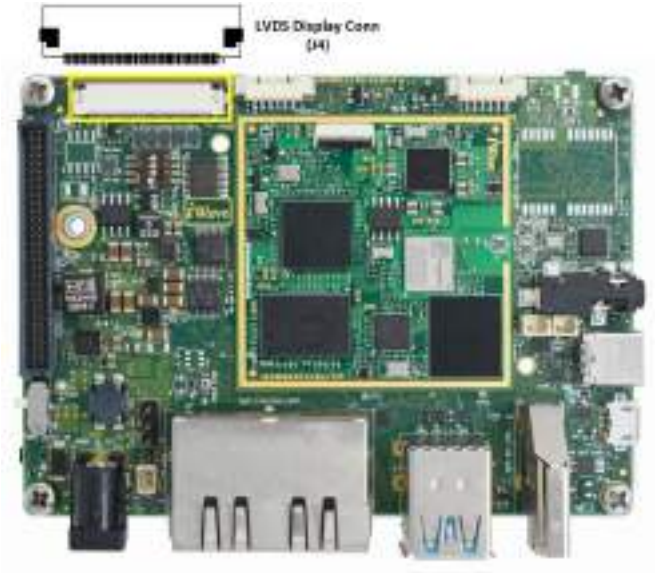

Figure 17: 40 pin LVDS Display Connector

Table 9: 40 Pin LVDS Display Connector Pinout

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	NC1	-	-	NC
2	VDD1	VCC_3V3	Power	3.3V Supply Voltage
3	VDD2	VCC_3V3	Power	3.3V Supply Voltage
4	NC2	-	-	NC
5	NC3	-	-	NC
6	NC4	-	-	NC
7	NC5	-	-	NC
8	LV0N-	LVDS0_D0_N	O, LVDS	LVDS Channel0 negative
9	LV0N+	LVDS0_D0_P	O, LVDS	LVDS Channel0 positive
10	GND1	GND	Power	Ground
11	LV1N-	LVDS0_D1_N	O, LVDS	LVDS Channel1negative
12	LV1N+	LVDS0_D1_P	O, LVDS	LVDS Channel1 positive
13	GND2	GND	Power	Ground
14	LV2N-	LVDS0_D2_N	O, LVDS	LVDS Channel2negative
15	LV2N+	LVDS0_D2_P	O, LVDS	LVDS Channel2 positive
16	GND3	GND	Power	Ground

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
17	LVCLK-	LVDS0_CLK_N	O, LVDS	LVDS Channel0 clock negative
18	LVCLK+	LVDS0_CLK_P	O, LVDS	LVDS Channel0 clock positive
19	GND4	GND	Power	Ground
20	LV3N-	LVDS0_D3_N	O, LVDS	LVDS Channel3 negative
21	LV3N+	LVDS0_D3_P	O, LVDS	LVDS Channel3 positive
22	GND5	GND	Power	Ground
23	LED_GND1	GND	Power	Ground
24	LED_GND2	GND	Power	Ground
25	LED_GND3	GND	Power	Ground
26	NC6	-	-	NC
27	LED_PWM	TPM4(GPIO_IO05)	O, 1.8V	PWM control signal
28	LED_EN	LVDS_BL_EN(IO_07)	O, 1.8V	Backlight Enable signal
29	NC7	-	-	NC
30	NC8	-	-	NC
31	LED_VCC1	VCC_12V_LVDS	Power	12V Supply Voltage
32	LED_VCC2	VCC_12V_LVDS	Power	12V Supply Voltage
33	LED_VCC3	VCC_12V_LVDS	Power	12V Supply Voltage
34	NC9	-	-	NC
35	BIST	-	-	NC
36	NC10	-	-	NC
37	NC11	-	-	NC
38	NC12	-	-	NC
39	NC13	-	-	NC
40	NC14	-	-	NC

2.9.3 USB Touch Connector

The i.MX 93 or i.MX 91 Pico ITX SBC supports a 6 Pin USB touch connector (J3). This connector can be used as general-purpose touch connector using USB interface.

Figure 18: USB Touch Connector

Number of Pins : 6

Connector Part :532610671 from Molex

Table 10: USB Touch Header Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	1	VBUS_HOST_TP	Power	Supply Voltage.
2	2	USB_HUB1OUT_DM	IO, USB	Differential USB Negative.
3	3	USB_HUB1OUT_DP	IO, USB	Differential USB Positive.
4	4	NC	-	NC.
5	5	GND	Power	Ground.
6	6	NC	-	NC.

2.9.4 MIPI DSI Interface (Not available in i.MX 91)

The i.MX 93 SoC supports one 4-lane MIPI DSI display with data supplied by the LCDIF Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2. It is capable of resolutions achievable with a 200 MHz pixel clock and active pixel rate of 140 Mpixel/s with 24-bit RGB. Support 80 Mbps—1.5 Gbps data rate per lane in high-speed operation.

The i.MX 93 Pico ITX SBC supports 39pin, 4-lane MIPI DSI Display Connector(J21) which is located at top side of the board as shown.

Number of Pins : 39

Connector Part : 5025983993 from Molex

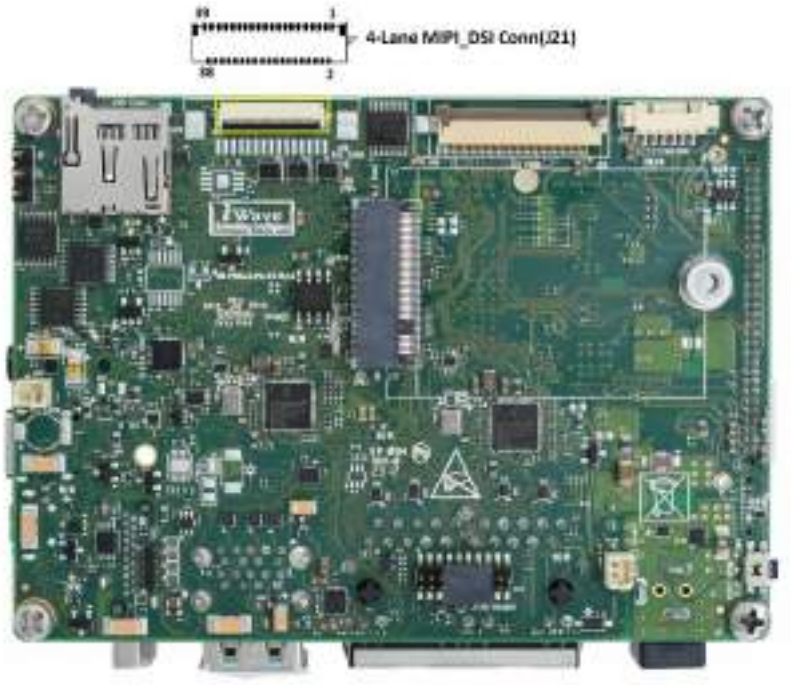

Figure 19: 4 Lane MIPI DSI Connector

Table 11: 4-Lane MIPI DSI Connector Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.
4	VBAT	VCC_3V3_TFT0	Power	3.3V Supply Voltage.
5	VBAT	VCC_3V3_TFT0	Power	3.3V Supply Voltage.
6	VBAT	VCC_3V3_TFT0	Power	3.3V Supply Voltage.
7	VBAT	VCC_3V3_TFT0	Power	3.3V Supply Voltage.
8	VBAT	VCC_3V3_TFT0	Power	3.3V Supply Voltage.
9	GND	GND	Power	Ground.
10	OTPV	NC	-	NC.
11	NC1	NC	-	NC.
12	GND	GND	Power	Ground.
13	D3P	MIPI_DSI1_D3_P	O, MIPI	MIPI DSI differential data lane 3 positive
14	D3N	MIPI_DSI1_D3_N	O, MIPI	MIPI DSI differential data lane 3 negative
15	GND	GND	Power	Ground.
16	D0P	MIPI_DSI1_D0_P	O, MIPI	MIPI DSI differential data lane 0 positive
17	D0N	MIPI_DSI1_D0_N	O, MIPI	MIPI DSI differential data lane 0 negative
18	GND	GND	Power	Ground.
19	DKP	MIPI_DSI1_CLK_P	O, MIPI	MIPI DSI differential Clock positive
20	DKN	MIPI_DSI1_CLK_N	O, MIPI	MIPI DSI differential Clock negative
21	GND	GND	Power	Ground.
22	D1P	MIPI_DSI1_D1_P	O, MIPI	MIPI DSI differential data lane 1 positive
23	D1N	MIPI_DSI1_D1_N	O, MIPI	MIPI DSI differential data lane 1 negative
24	GND	GND	Power	Ground.
25	D2P	MIPI_DSI1_D2_P	O, MIPI	MIPI DSI differential data lane 2 positive
26	D2N	MIPI_DSI1_D2_N	O, MIPI	MIPI DSI differential data lane 2 negative
27	GND	GND	Power	Ground.
28	RESX	OSM_GPIO_B5(GPIO_IO 26)	O, 1,8V CMOS /10k PU	*Display reset. Active low. OSM_GPIO_A1(SPI3_MISO_GPIO_IO09) is optionally connected.*
29	VDDIO	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Display IO Circuit.
30	VCI	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for Display Circuit.
31	NC2	NC	NA	NA.
32	GND	GND	Power	Ground.
33	TP_AVDD_3P3V	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for Touch driver

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Circuit.
34	TP_DVDD_1P8V	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Touch IO Circuit.
35	TP_SDA	I2C7_SDA(GPIO_IO06)	IO, 1.8V CMOS	I2C Data for Capacitive Touch
36	TP_SCL	I2C7_SCL(GPIO_IO07)	O, 1.8V CMOS	I2C Clock for Capacitive Touch
37	TP_RESET	OSM_GPIO_A1(SPI3_MISO_GPIO_IO09)	O, 1.8V CMOS, 10K PU	RESET for Capacitive Touch
38	TP_INT	OSM_GPIO_A2(SPI3_MOSI_GPIO_IO10)	I 1.8V CMOS	Interrupt from Capacitive Touch
39	GND	GND	Power	Ground.

2.9.5 2-Lane MIPI DSI Display Connector (Optional)

The i.MX 93 Pico ITX SBC optionally supports 2-lane MIPI DSI Display.

Number of Pins: 15

Connector Part : 1-84952-5 from TE Connectivity AMP Connectors

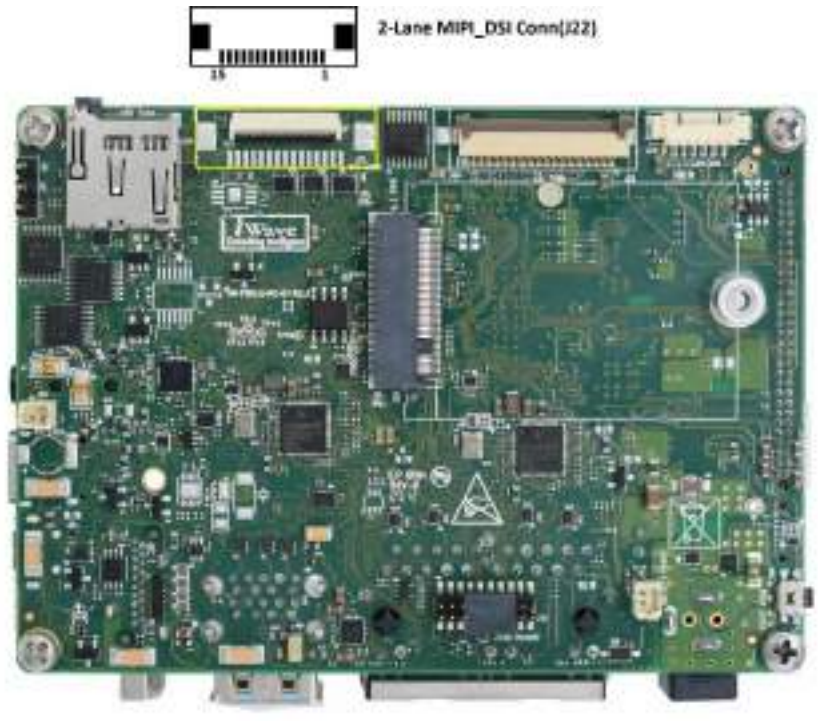

Figure 20: MIPI DSI 2-Lane display Connector (Optional)

Table 12: Optional 2-Lane MIPI DSI Connector Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	DATA1-	MIPI_DSI1_D1_N	O, MIPI	MIPI DSI differential data lane 1negative

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
3	DATA1+	MIPI_DSI1_D1_P	O, MIPI	MIPI DSI differential data lane 1 positive
4	GND	GND	Power	Ground.
5	CLK-	MIPI_DSI1_CLK_N	O, MIPI	MIPI DSI differential Clock negative
6	CLK+	MIPI_DSI1_CLK_P	O, MIPI	MIPI DSI differential Clock positive
7	GND	GND	Power	Ground.
8	DATA0-	MIPI_DSI1_D0_N	O, MIPI	MIPI DSI differential data lane 0negative
9	DATA0+	MIPI_DSI1_D0_P	O, MIPI	MIPI DSI differential data lane 0 positive
10	GND	GND	Power	Ground.
11	SCL	I2C7_SCL(GPIO_IO07)	I,1.8V CMOS/4.7K PU	I2C Clock.
12	SDA	I2C7_SDA(GPIO_IO06)	IO,1.8V CMOS/4.7K PU	I2C Data
13	GND5	GND	Power	Ground.
14	VCC1	VCC_3V3	Power	3.3V Supply Voltage.
15	VCC2	VCC_3V3	Power	3.3V Supply Voltage.

2.9.6 I2S Audio Interface

The i.MX 93 or i.MX 91 Pico ITX SBC supports Audio IN/OUT through SoC's SAI1 interface which can support I2S format. This four wire I2S signals from the SoC is connected to I2S Audio Codec "SGTL5000" to support CTIA configuration Headphone Stereo output and Mono Mic input through Single 3.5mm audio Jack (J9). The Audio IN/OUT Jack is physically located at the top of the board as shown below.

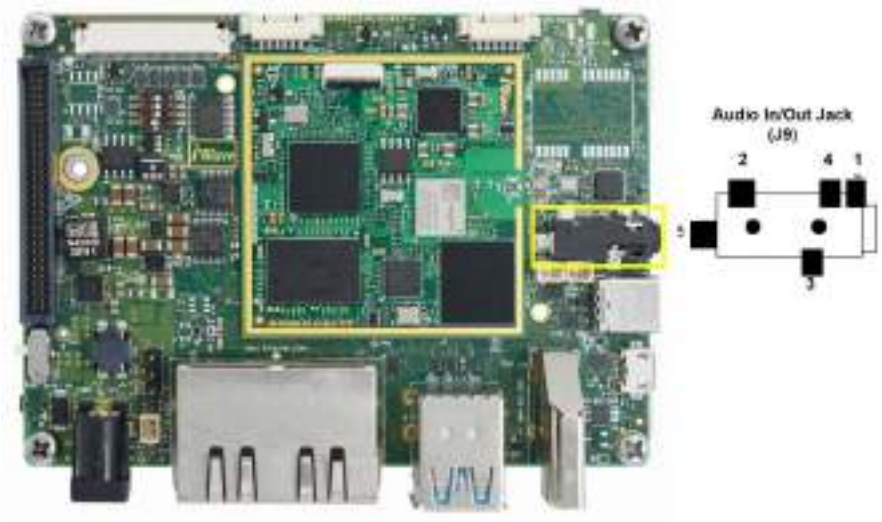

Figure 21: Audio IN/OUT Jack

The i.MX 93 or i.MX 91 Pico ITX SBC supports 3W Audio Amplifier. The LINEOUT signals from "SGTL5000" are connected to an Audio Amplifier. The Output signals from the Amplifier is connected to two Speaker Headers (J10) and (J11). The Speaker Headers is physically located at the top of the board as shown below.

Number of Pins : 2

Connector Part : 10114829-10102LF from Molex

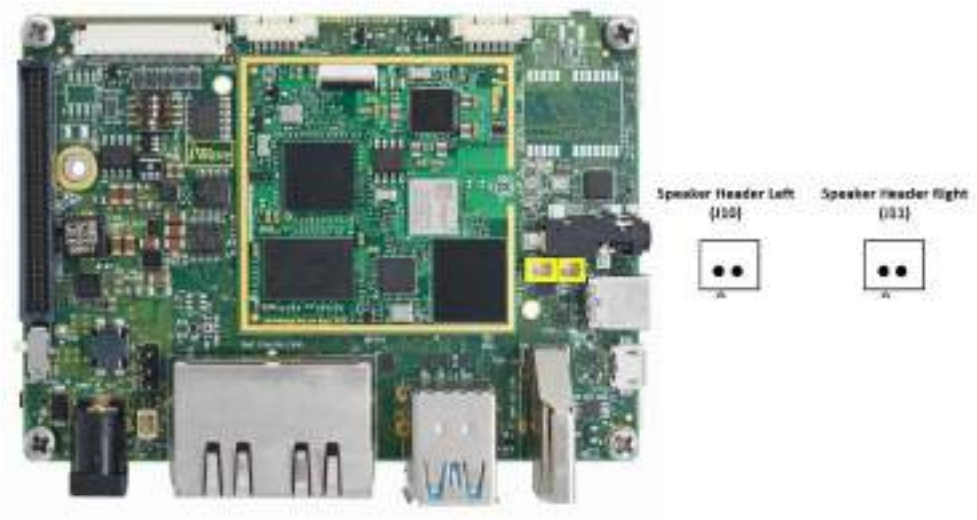

Figure 22: Speaker Headers

Table 13: Speaker Header(J10) Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	SPL+	SPKR_L+	O, Analog Audio	Speaker Left Positive.
2	SPL-	SPKR_L-	O, Analog Audio	Speaker Left Negative.

Table 14: Speaker Header(J11) Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	SPR+	SPKR_R+	O, Analog Audio	Speaker Right Positive.
2	SPR-	SPKR_R-	O, Analog Audio	Speaker Right Negative.

2.10 M.2 Key-B Connector

The i.MX 93 or i.MX 91 Pico ITX SBC supports M.2 B key-B socket. M.2 B key-B socket is the Next Generation Form Factor (NGFF) which is designed to support multiple modules and make the M.2 more suitable in application like solid-state storage, WWAN. The M.2 Key B Connector USB 2.0, I2C and SMBus. The M.2 Key-B Connector (J28) is placed at the bottom side of the board.

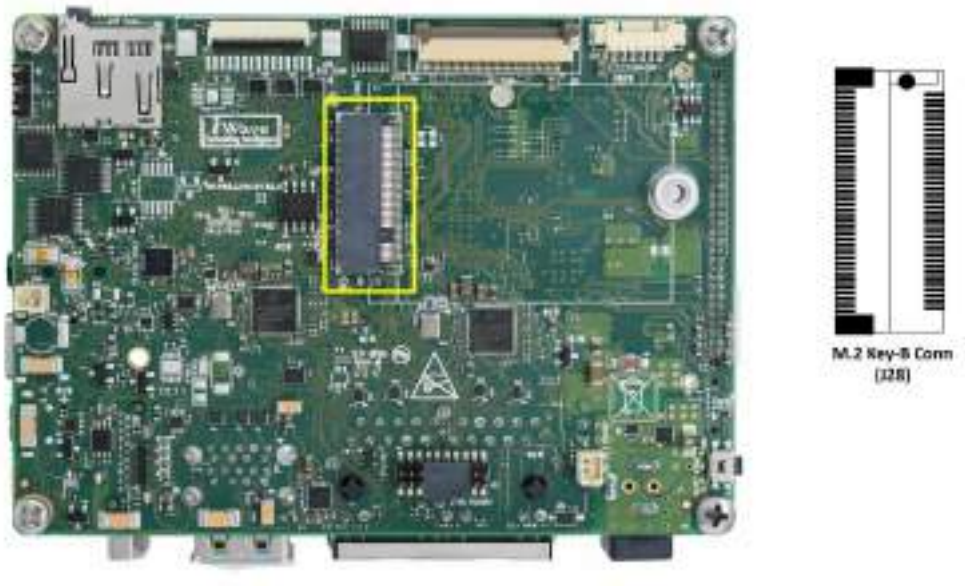

Figure 23: M.2 Key B Connector

Table 15: M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	OSM_GPIO_B1(GPIO_IO16)	O, 1.8V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	OSM_USBA_OTG1_DP	IO, USB	USB2.0 PortA Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	NC	NC	NC.
9	USB_D-	OSM_USBA_OTG1_DM	IO, USB	USB2.0 PortA Data Minus.
10	GPIO9(LED1#/DAS_DSS#) (I)(0/3.3V)	M.2_LED	O, 3.3V CMOS	Provide status indicators via LED.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	OSM_GPIO_C4(GPIO_IO22)	IO, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel1 Clock
21	CONFIG_0	M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	OSM_GPIO_C5(GPIO1_IO10_PDM_B1)	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	NC	NC	NC.
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	NC	NC	NC.
25	DPR (O) (0/1.8V)	CAM_PWR_EN(GPIO_IO24)	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	NC	NC	NC.
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	NC	NC	NC.
29	PERN1/USB30_RX-/SSIC_RX-	NC	NC	NC.
30	UIM-RESET (I)	NC	NC	NC
31	PERP1/USB30_RX+/SSIC_RX+	NC	NC	NC.
32	UIM-CLK (I)	NC	NC	NC
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	NC	NC	NC
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NC	NC.
36	UIM-PWR (I)	NC	NC	NC

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NC	NC.
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8 V)	NC	NC	NC.
41	PERN0/SATA_B+	NC	NC	NC.
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	NC	NC	NC.
43	PERP0/SATA_B-	NC	NC	NC.
44	GPIO2_(ALERT# /GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	NC	NC	NC.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/ UIM_RST2) (I/O)(0/1.8V)	NC	NC	NC.
47	PETN0/SATA_A-	NC	NC	NC.
48	GPIO4(TX_BLK/GNSS_1/ UIM_PWR2)(I/O)(0/1.8V)	NC	NC	NC.
49	PETP0/SATA_A+	NC	NC	NC.
50	PERST# (O)(0/3.3V)	NC	NC	NC.
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	NC	NC	NC.
53	REFCLKN	NC	NC	NC.
54	PEWAKE# (I/O)(0/3.3V)	NC	NC	NC.
55	REFCLKP	NC	NC	NC.
56	MFG_DATA	I2C7_SDA(GPIO_IO06)	IO, 3.3V CMOS	NC. *Optionally I2C Data is connected.*
57	GND	GND	Power	Ground.
58	MFG_CLOCK	I2C7_SCL(GPIO_IO07)	O, 1.8V CMOS	NC. *Optionally I2C Clock is connected.*
59	ANTCTL0 (I)(0/1.8 V)	NC	NC	NC.
60	COEX3 (I/O)(0/1.8V)	NC	NC	NC.
61	ANTCTL1 (I)(0/1.8 V)	NC	NC	NC.
62	COEX_TXD (O)(0/1.8V)	NC	NC	NC.
63	ANTCTL2 (I)(0/1.8 V)	NC	NC	NC.
64	COEX_RXD (I)(0/1.8V)	NC	NC	NC.
65	ANTCTL3 (I)(0/1.8 V)	NC	NC	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
66	SIM_DETECT (I)	NC	NC	NC
67	RESET# (O)(0/1.8V)	CAM_RST(GPIO_IO23)	I, 1.8V 10K PU	M.2 Reset Signal *Optionally available*
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK	I, 32.768kHz Clock Supply	*Note: Optionally connected 32.768kHz Clock output*
69	CONFIG_1	M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

Below are the steps for Inserting an M.2 Key B Module to the i.MX 93 Pico ITX SBC M.2 Connector

Step 1: Move the Module against housing Chamber.

Step 2: Rotate the Module to 25 Degree and insert until the bottom of the module surface reaches the ramp.

Step 3: Rotate the Module to horizontal Position by hand

Step 4: Fix the module with M3 x4 Screw

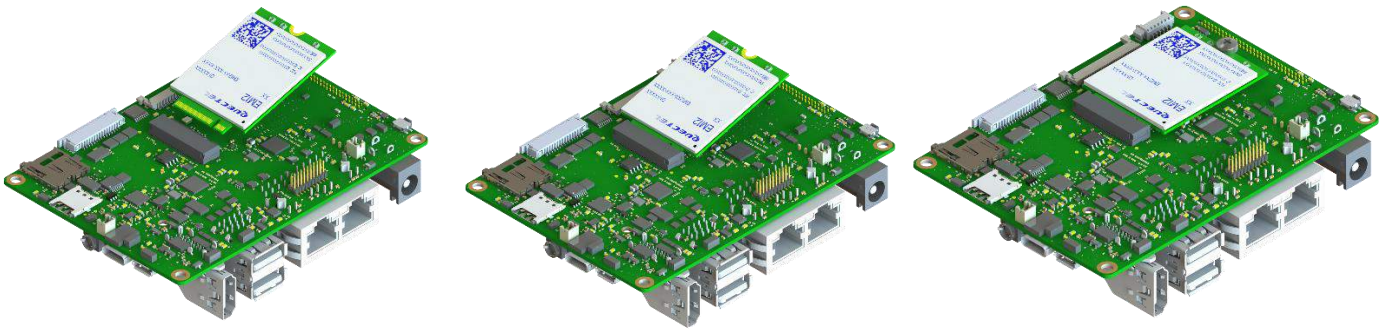

Figure 24: M.2 Module Insertion Guide

2.11 Expansion Connector

The interfaces which are available at 60 Pin Expansion connector are explained in the following section. This Expansion Connector (J6) is physically located at the top of the SBC as shown below.

Number of Pins : 60

Connector Part : TFC-130-01-L-D-A from Samtech

Figure 25: Expansion Connector

Table 16: Expansion Connector Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	TAMPER0	TAMPER0/B16	I, 1.8V Power	Tamper Signal. *ADC_0 signal is available optionally*
2	NC	-	-	NC.
3	TAMPER1	TAMPER1/F14	I, 1.8V Power	Tamper Signal. *ADC_1 signal is available optionally*
4	NC	-	-	Tamper Signal. *ADC signal is available optionally*
5	GND	-	Power	Ground
6	GND	-	Power	Ground
7	UART8_RXD	GPIO_IO13/N21	I, 1.8V CMOS	Optional *By default, connected to BT module*
8	NC	-	-	NC.
9	UART8_TXD	GPIO_IO12/N20	O, 1.8V CMOS	Optional *By default, connected to BT module*
10	NC	-	-	NC.
11	UART8_RTS	GPIO_IO15/P21	O, 1.8V CMOS	Optional *By default, connected to BT module*
12	GND	-	Power	Ground

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
13	UART8_CTS	GPIO_IO14/P20	I, 1.8V CMOS	Optional *By default, connected to BT module*
14	NC	-	-	NC.
15	GND	-	Power	Ground
16	NC	-	-	NC.
17	NC	-	-	NC.
18	GND	-	Power	Ground
19	NC	-	-	NC.
20	NC	-	-	NC.
21	NC	-	-	NC.
22	NC	-	-	NC.
23	NC	-	-	NC.
24	GND	-	Power	Ground
25	GND	-	Power	Ground
26	NC	-	-	NC.
27	NC	-	-	NC.
28	NC	-	-	NC.
29	NC	-	-	NC.
30	GND	-	Power	Ground
31	I2C3_SCL(GPIO_IO29)	GPIO_IO29/Y21	O,OD CMOS,1.8V	I2C3 Clock
32	NC	-	-	NC.
33	I2C3_SDA(GPIO_IO28)	GPIO_IO28/W20	IO,OD CMOS,1.8V	I2C3 Data
34	NC	-	-	NC.
35	NC	-	-	NC.
36	NC	-	-	NC.
37	TPM4(GPIO_IO05)	GPIO_IO05/L18	O, 1.8V CMOS	PWM Signal. Also connected to LVDS Connector.
38	NC	-	-	NC.
39	LVDS_BL_EN(IO_07)	-	O, 1.8V CMOS	GPIO Also connected to LVDS Connector.
40	NC	-	-	NC.
41	NC	-	-	NC.
42	NC	-	-	NC.
43	CAN2_TX(GPIO_IO25)	GPIO_IO25/V21	O, 1.8V	CAN Transmitter
44	NC	-	-	NC.
45	CAN2_RX(GPIO_IO27)	GPIO_IO27/W21	I,1.8V	CAN Receiver
46	NC	-	-	NC.
47	NC	-	-	NC
48	NC	-	-	NC.
49	NC	-	-	NC
50	NC	-	-	NC.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
51	GND	-	Power	Ground
52	NC	-	-	NC.
53	VCC_5V	-	Power	5V Supply Voltage
54	NC	-	-	NC.
55	VCC_3V3	-	Power	3.3V Supply Voltage
56	VCC_1V8	-	Power	1.8V Supply Voltage
57	VCC_3V3	-	Power	3.3V Supply Voltage
58	VCC_12V	-	Power	12V Supply Voltage
59	GND	-	Power	NC.
60	GND	-	Power	Ground

*Note: Refer GPIO Column under **"i.MX 93 or i.MX 91 Pin Multiplexing on Expansion Connector** for details on GPIO options available from Expansion connector.*

2.12 Other Features

2.12.1 Fan Header

The i.MX 93 or i.MX 91 Pico ITX SBC supports a Fan Header to connect cooling Fan if required. This Fan Header (J18) is physically located at the top of the board as shown below.

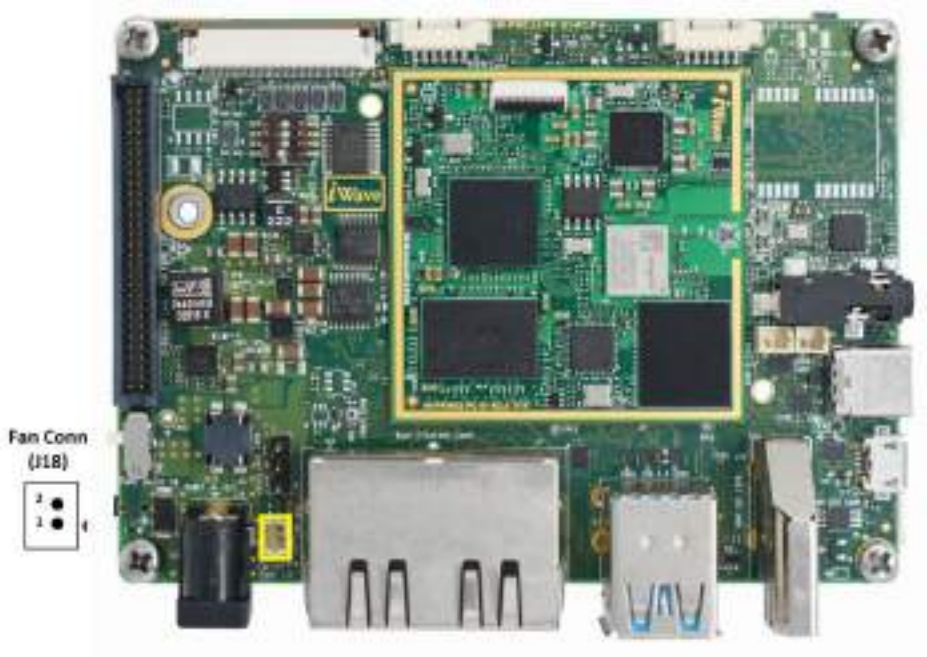

Figure 26: Fan Connector

Number of Pins : 2

Connector Part :10114829-10102LF from Amphenol ICC (FCI)

Table 17: Fan Connector Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN. *Note: Optionally connected to 12V Power.*
2	GND	Power	Ground.

Note: Contact iWave support team if 12V Power Support is required for FAN Header support is required.

2.12.2 RTC Controller with RTC Battery Header

The i.MX 93 or i.MX 91 Pico ITX SBC supports external RTC Controller “PCF85263” for Real time clock support. This external RTC Controller IC is connected to i.MX 93 SoC through I2C7 Interface and operates at 3.3V voltage level.

The i.MX 93 or i.MX 91 Pico ITX SBC supports external RTC cell. The SBC supports 2pin connector for backup battery or coin cell connection. The 2pin RTC (J29) battery connector is physically located on bottom side of the SBC as shown below.

Note: RTC cannot be used as wake-up source, as a result RTC alarm won't work.

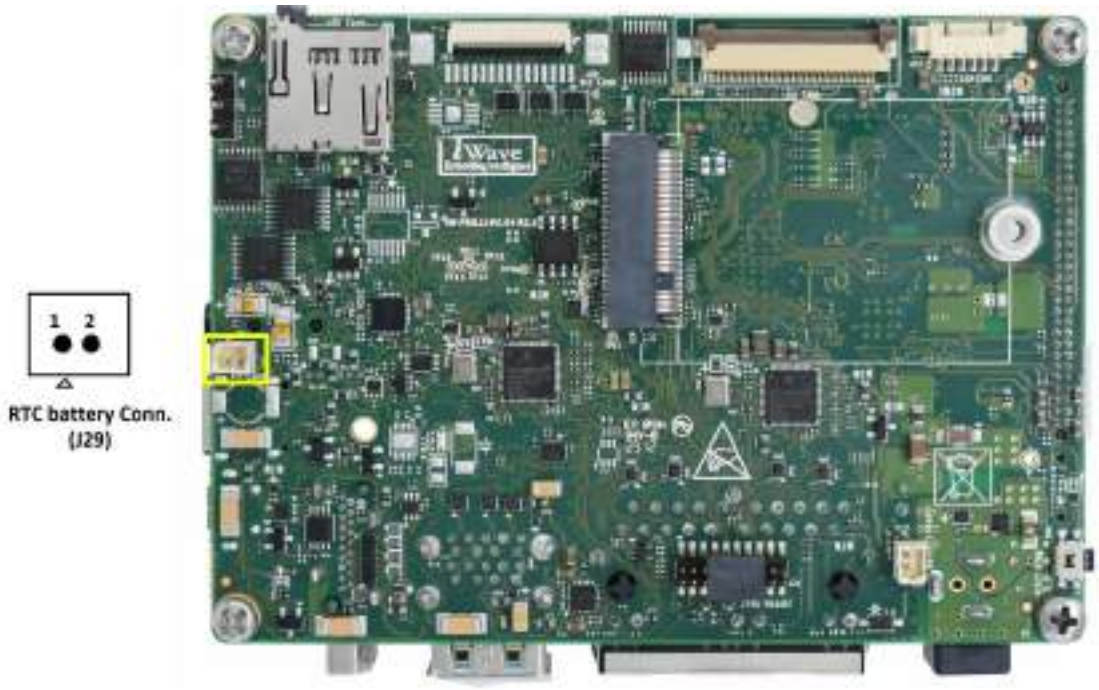

Figure 27: RTC Battery Connector

Number of Pins : 2

Connector Part : 10114829-10102LF from Amphenol ICC (FCI)

Table 18: RTC Battery Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VRTC_3V0	I, Power	+3V Power Input to RTC Controller
2	GND	Power	Ground.

Note: Contact iWave support team if External RTC Controller support is required.

2.12.3 JTAG Interface (Optional)

The i.MX 93 or i.MX 91 Pico ITX SBC supports JTAG interface for CPU debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security.

JTAG Header (J31) is physically located on bottom side of the board.

Number of Pins - 20

Connector Part - 62132021021 from Wruth Electronics.

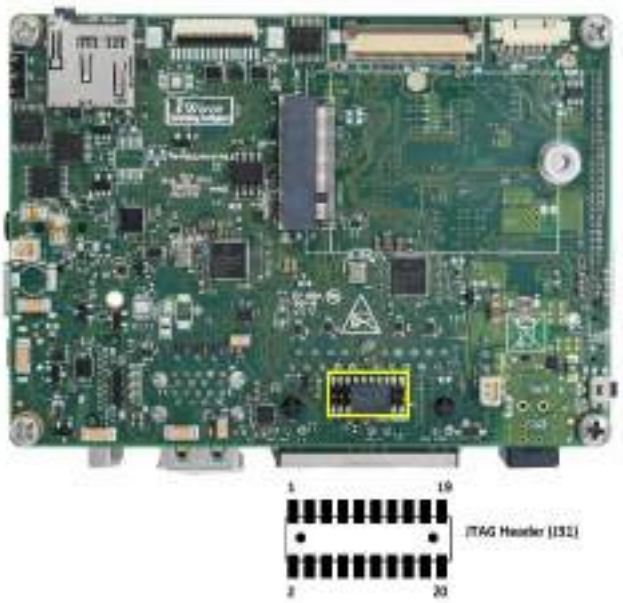

Figure 28: JTAG Header

Table 19: JTAG Header Pin Assignment

Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_1V8	-	O, 1.8V Power	VTREF Voltage Reference.
2	VCC_1V8	-	O, 1.8V Power	Supply Voltage.
3	JTAG_NTRST	POR_B/A16	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	-	Power	Ground.
5	GPIO3_IO28(JTAG_TDI)	DAP_TDI/W1	I, 1.8V CMOS	JTAG test data input. By default, 10K PU is mounted to read board configuration.
6	GND	-	Power	Ground.
7	GPIO3_IO29(JTAG_TMS)	DAP_TMS_SWDIO/W2	I, 1.8V CMOS/ 10K PU	JTAG test mode select. By default, 10K PD is mounted to read board configuration.
8	GND	-	Power	Ground.
9	GPIO3_IO30(JTAG_TCK)	DAP_TCLK_SWCLK/Y1	I, 1.8V CMOS/ 10K PD	JTAG test Clock. By default, 10K PD is mounted to read board configuration.
10	GND	-	Power	Ground.
11	-	-	-	10K PD is mounted.
12	GND	-	Power	Ground.
13	GPIO3_IO31(JTAG_TDO)	DAP_TDO_TRACESWO/Y2	O, 1.8V CMOS	JTAG test data output. By default, 10K PD is mounted to read board configuration.
14	GND	-	Power	Ground.
15	-	-	-	10K PU is mounted.

Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
16	GND	-	Power	Ground.
17	-	-	-	10K PU is mounted.
18	GND	-	Power	Ground.
19	-	-	-	10K PD is mounted.
20	GND	-	Power	Ground.

2.12.4 Power ON/OFF Switch

The i.MX 93 or i.MX 91 Pico ITX SBC has power ON/OFF switch (SW3) to control the Main power Input ON/OFF functionality. The Power ON/OFF switch is physically located at the top of the board as shown below.

Figure 29: Power ON/OFF Switch

2.12.5 Reset Switch

The i.MX 93 or i.MX 91 Pico ITX SBC supports Push button switch (SW4) to reset the i.MX 93 CPU. Reset signal is directly connected from Reset Push button switch. This Reset Push button switch (SW4) is physically located at the bottom of the board as shown below.

Figure 30: Reset Switch

2.12.6 CPU ON/OFF Switch

The i.MX 93 or i.MX 91 Pico ITX SBC supports Push button switch (SW2) for ON OFF the i.MX 93 CPU. ON/OFF is directly connected from ON/OFF Push button switch. This ON/OFF Push button switch (SW2) is physically located at the top of the board as shown below.

Figure 31: CPU ON/OFF Switch

2.13 i.MX 93 or i.MX 91 Pin Multiplexing on Expansion Connector

The i.MX 93 or i.MX 91 SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 93 or i.MX 91 SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 93 or i.MX 91 SoC pin connections to the Expansion connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 93 or i.MX 91 Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SBC for iWave's BSP reusability and to have compatible SBCs in future for upgradability.

Table 20: i.MX 93 or i.MX 91 SoC IOMUX for Expansion Connector interfaces

Interface/ Function	Expansion Connector Pin Number	i.MX 93 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
CAN2	43	V21	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]
	45	W21	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]
PWM	37	L17	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]
I2C3	33	W20	gpio2.IO[28]	i2c3.SDA						flexio1.FLEXIO[28]
	31	Y21	gpio2.IO[29]	i2c3.SCL						flexio1.FLEXIO[29]
UART8	7	N21	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]
	9	N20	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
	11	P21	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]
	13	P20	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 93 or i.MX 91 Pico ITX SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The i.MX 93 or i.MX 91 Pico ITX SBC supports 7V to 24V external power and uses on board voltage regulators for internal power management. By default, it supports to work with 12V power input. 12V power input from an external power supply is connected to the i.MX 93 Pico ITX SBC (J20). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. The Power Jack is physically placed at the top of the board as shown below.

Figure 32: Power Input Jack

Table 21: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[1]	2.8V	3V	3.3V	±20mV

[1] The i.MX 93 or i.MX 91 Pico ITX SBC uses this voltage as backup power source to PMIC RTC controller when VCC is off.

3.2 Power Consumption

Table 22: i.MX 93 Pico ITX SBC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Boot time Power consumption		
While booting	VCC_12V	0.197A/2.364W
Run Mode Power Consumption		
Play Audio	VCC_12V	0.135A/1.62W
Camera Streaming in MIPI	VCC_12V	0.23A/2.76W
Camera Streaming in LVDS	VCC_12V	0.759A/9.108W
Play Video run in LVDS(Gplay)	VCC_12V	0.737A/8.844W
Play Video run in MIPI(Gplay)	VCC_12V	0.249A/2.988W
Ping Bluetooth	VCC_12V	TBD
Ping Wifi	VCC_12V	0.149A/1.788W
Ping Ethernet (Eth0) at 1000Mbps	VCC_12V	0.176A/2.112W
Ping Ethernet (Eth1) at 1000Mbps	VCC_12V	0.177A/2.124W
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_12V	0.207A/2.484W
eMMC to USB2.0 x 2 Host file transfer	VCC_12V	0.255A/3.06W
eMMC to USB2.0 x1 OTG Host file transfer	VCC_12V	0.236A/2.832W
eMMC to USB 2.0 x 1 Host (Type C) file transfer	VCC_12V	0.23A/2.76W
eMMC to Micro SD file transfer	VCC_12V	0.21A/2.52W
File Transfer - Transfer the 1MB files in storage devices	VCC_12V	0.32A/3.84W
Dhrystone	VCC_12V	0.153A/1.836W
Bluetooth file transfer	VCC_12V	TBD
Wi-Fi file transfer	VCC_12V	0.218A/2.616W
Ethernet Streaming (Video Play)	VCC_12V	0.847A/10.164W
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1MB files in storage devices • Run the dry2 application on background • Ping Wifi • Camera Streaming • Play Video	VCC_12V	1.02A/12.24W
Low Power Mode Power Consumption		
System Idle Mode	VCC_12V	0.105A/1.26W
Deep Sleep Mode	VCC_12V	0.067A/0.804W
RTC power when no VCC_12V supply is provided	VRTC_3V0	0.04uA/0.12uW

[1] Power consumption measurements have been done in iWave's i.MX 93 based Pico ITX SBC with iWave's iW-PRHDZ-SC-01-R2.0-REL0.1-Linux6.1.1 BSP.

Table 23: i.MX 91 Pico ITX SBC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Audio	VCC_12V	TBD
Ping Bluetooth	VCC_12V	TBD
Ping Wi-Fi	VCC_12V	TBD
Ping Ethernet (Eth0) at 1000Mbps	VCC_12V	TBD
Ping Ethernet (Eth1) at 1000Mbps	VCC_12V	TBD
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_12V	TBD
eMMC to USB2.0 file transfer	VCC_12V	TBD
eMMC to USB2.0 OTG file transfer	VCC_12V	TBD
eMMC to Micro SD file transfer	VCC_12V	TBD
File Transfer - Transfer the 1GB files in storage devices	VCC_12V	TBD
Dhrystone	VCC_12V	TBD
Bluetooth file transfer	VCC_12V	TBD
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background • Ethernet Streaming (Video Play) • Ping Wifi • Ping Bluetooth	VCC_12V	TBD
Low Power Mode Power Consumption		
System Idle Mode.	VCC_12V	TBD
Deep Sleep Mode.	VCC_12V	TBD
RTC power when no VCC_12V supply is provided	VRTC_3V0	TBD

[1] Power consumption measurements have been done in iWave's i.MX 91 based Pico ITX SBC with iWave's iW-PRHDZ-SC-01-R2.0-REL0.1-Linux6.1.1 BSP.

3.3 EnvironmentalCharacteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 93 or i.MX 91 Pico ITX SBC.

Table 24: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2] For more information on Thermal solution & Heat sink refer the following section.

3.3.2 Heat Sink

For any highly integrated SBC, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink or Fan Sink must be used. Always need to remember that more effective thermal solution will give more performance out of the CPU.

Note: iWave supports Heat Sink Solution for i.MX 93 or i.MX 91 Pico ITX SBC. For more information on Heat Sink& Fan Sink contact iWave support team. Do not Power On the i.MX 93 or i.MX 91 Pico ITX SBC without a proper thermal solution.

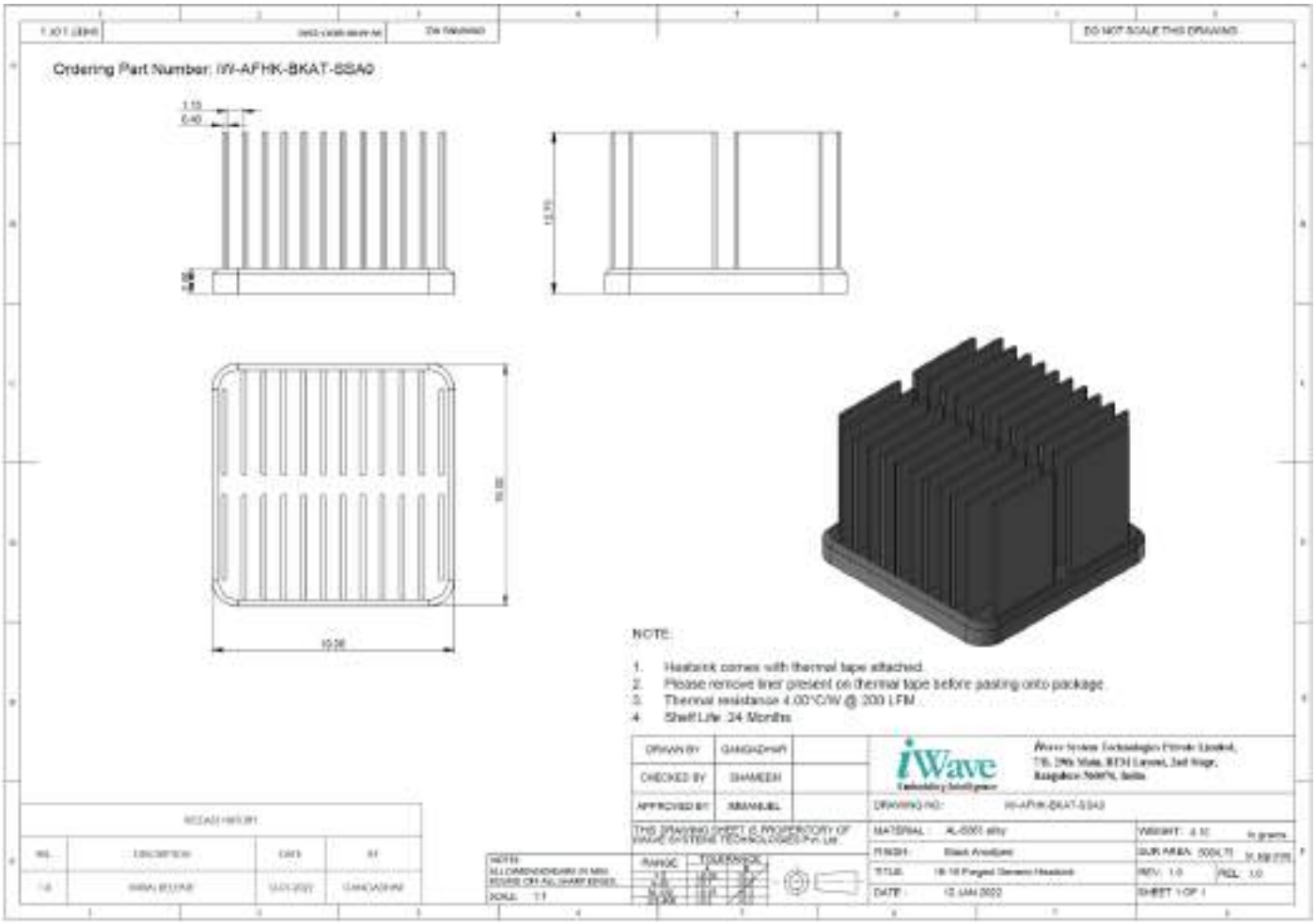

Figure 33: Mechanical dimension of Heat Sink

3.3.3 RoHS Compliance

iWave's i.MX 93 or i.MX 91 Pico ITX SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.4 Electrostatic Discharge

iWave's i.MX 93 or i.MX 91 Pico ITX SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.4 MechanicalCharacteristics

3.4.1 i.MX 93 or i.MX 91 Pico ITX SBC Mechanical Dimensions

i.MX 93 or i.MX 91 Pico ITX SBC PCB size is 100mm x 72mm x 1.2mm. Pico ITX SBC mechanical dimension is shown below. (All dimensions are shown in mm)

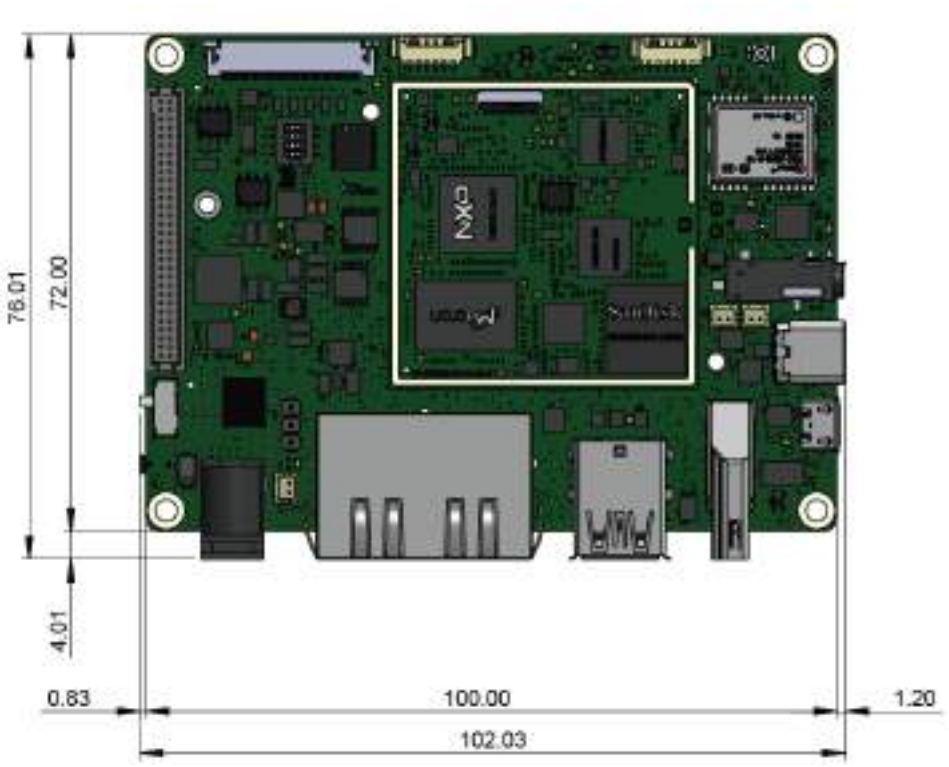

Figure 34: Mechanical Dimensions of i.MX 93 or i.MX 91 Pico ITX SBC Top View

The i.MX 93 or i.MX 91 Pico ITX SBC PCB thickness is 1.2mm±0.15mm, top side maximum height component is 16.40mm (HDMI Connector), followed by Dual Ethernet Connector (16.40mm). In bottom side maximum height component is JTAG connector (5.91mm) followed by M.2 SMT spacer (3.99mm).

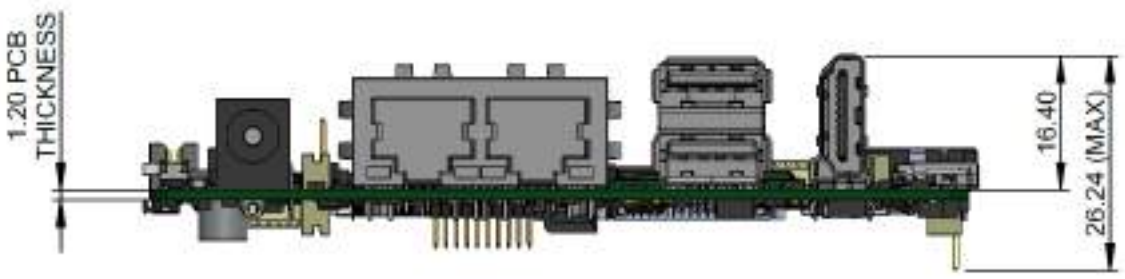

Figure 35: Mechanical Dimensions of i.MX 93 or i.MX 91 Pico ITX SBC Side View-1

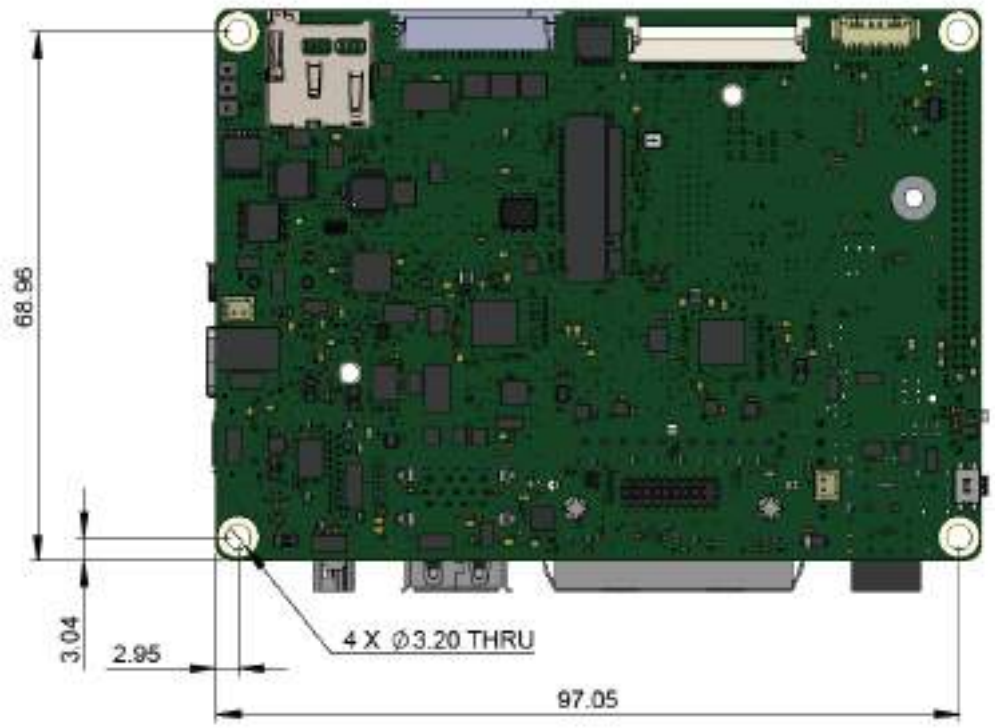

Figure 36: Mechanical Dimensions of i.MX 93 or i.MX 91 Pico ITX SBC Bottom View

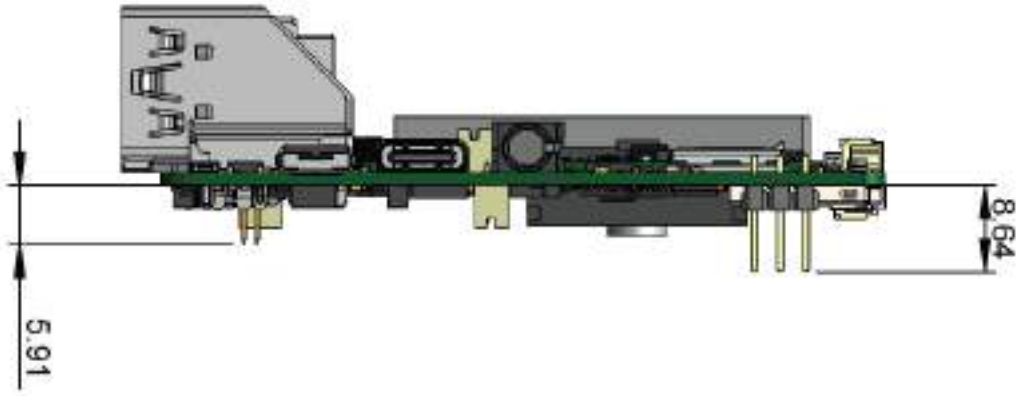

Figure 37: Mechanical Dimensions of i.MX 93 or i.MX 91 Pico ITX SBC Side View-2

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 93 or i.MX 91 Pico ITX SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 25: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G50S - i.MX 9352 R2.0 SBC (Industrial grade)-With Wi-Fi		
iW-G50S- OL93-4L002G-E016G-BIA	i.MX9352 Dual, 2GB LPDDR4X, 16GB eMMC-With Wi-Fi, BT	-40°C to 85°C
Rainbow G50S - i.MX 9352 R2.0 (Industrial grade) SBC- Without Wi-Fi		
iW-G50S- OL93-4L002G-E016G-BIB	i.MX9352 Dual, 2GB LPDDR4X, 16GB eMMC-Without Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 91 R2.0 SBC (Industrial grade)- With Wi-Fi, BT		
iW-G50S- OL91-4L002G-E016G-BIA	i.MX 91, 2GB LPDDR4, 16GB eMMC-With Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 91 R2.0 SBC (Industrial grade)- Without Wi-Fi, BT		
iW-G50S- OL91-4L002G-E016G-BIB	i.MX 91, 2GB LPDDR4, 16GB eMMC-Without Wi-Fi, BT	-40°C to 85°C

Important Note:

** Part Numbers mentioned in the above table are Pre-production silicon part numbers.*

** Some of the above-mentioned Part Numbers are subject to MOQ purchase. Please contact iWave for further details.*

** For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.*