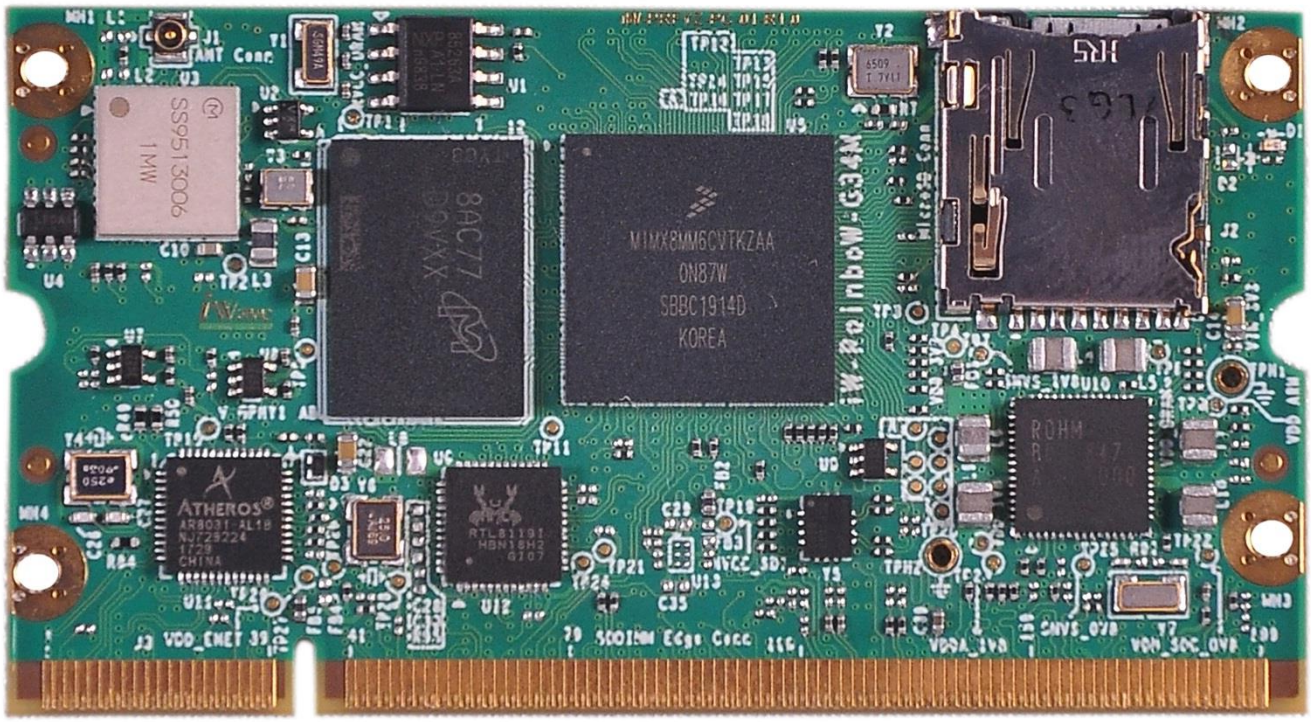
iW-RainboW-G34M/G37M
i.MX 8M Mini & i.MX 8M Nano SODIMM
System On Module
Hardware User Guide



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1.2	08th June 2022	Made common User Guide for i.MX 8M Mini & i.MX 8M Nano SOMs

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the SODIMM SOM based on the NXP's i.MX 8M Mini or i.MX 8M Nano Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM from a Hardware Systems perspective.

1.2 SODIMM SOM Overview

The SODIMM ("Small outline dual in line memory module") is a versatile small form factor computer Module definition targeting application that require low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies, GBE and single channel MIPI display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 8M Mini or i.MX 8M Nano SoC based SODIMM System on Module is rich with i.MX 8M Mini or i.MX 8M Nano features along with On SOM LPDDR4, eMMC, Ethernet PHY and comes in compact 67.6mm x 37mm form factor. The Module PCB has 200 edge fingers that mate with a low profile 200 pin 0.5mm pitch right angle connector.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit

Acronyms	Abbreviations
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OTG	On-The-Go
PCB	Printed Circuit Sheet
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SODIMM	Small outline dual in line memory module
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SODIMM SOM.

1.5 References

- IMX8MMIEC_Revx.x.pdf
- IMX_8M_Mini_RM_Revx.x.pdf
- IMX8MNIEC_Revx.x.pdf
- IMX_8M_Nano_RM_Revx.x.pdf

1.6 Important Note

In this document, wherever i.MX 8M Mini or i.MX 8M Nano SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_9)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO1_9*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8M Mini or i.MX 8M Nano SODIMM SOM features and Hardware architecture with high level block diagram.

2.1 i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Block Diagram

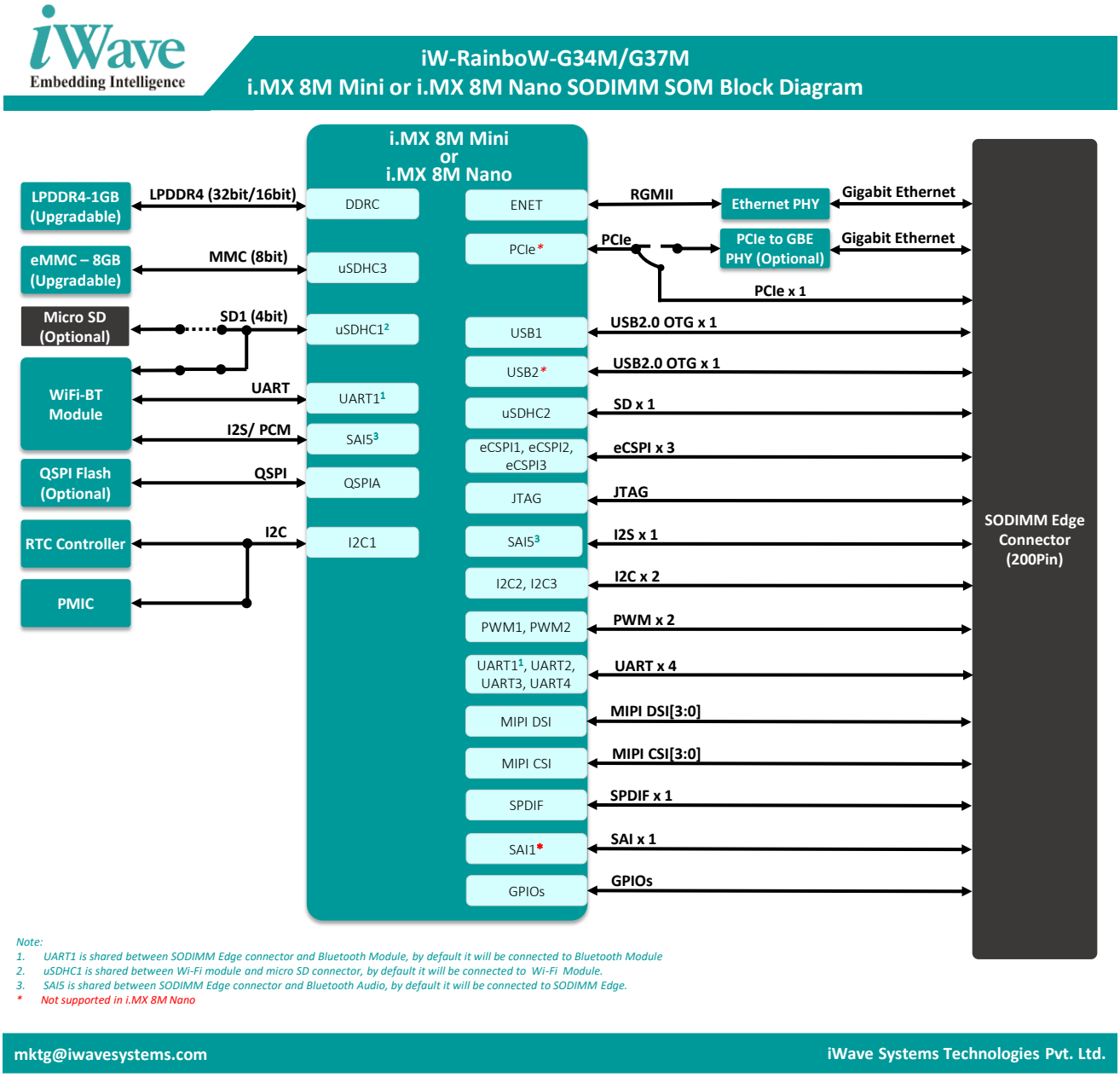

Figure 1: i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Block Diagram

2.2 i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Features

i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports the following features.

SoC

- i.MX 8M Mini Q/QL/D/DL/S/SL Processor[1]:
  - i.MX 8M Mini Quad : 4 x Cortex- A53, 1 x Cortex-M4
  - i.MX 8M Mini Quad Lite : 4 x Cortex- A53, 1 x Cortex-M4 (VPU not supported)
  - i.MX 8M Mini Dual : 2 x Cortex- A53, 1 x Cortex-M4
  - i.MX 8M Mini Dual Lite : 2 x Cortex- A53, 1 x Cortex-M4 (VPU not supported)
  - i.MX 8M Mini Solo : 1 x Cortex- A53, 1 x Cortex-M4
  - i.MX 8M Mini Solo Lite : 1 x Cortex- A53, 1 x Cortex-M4 (VPU not supported)

- i.MX 8M Nano Q/QL/D/DL/S/SL Processor[1]:
  - i.MX 8M Nano Quad : 4 x Cortex- A53, 1 x Cortex-M7
  - 7i.MX 8M Nano Quad Lite : 4 x Cortex- A53, 1 x Cortex-M7 (GPU not supported)
  - i.MX 8M Nano Dual : 2 x Cortex- A53, 1 x Cortex-M7
  - i.MX 8M Nano Dual Lite : 2 x Cortex- A53, 1 x Cortex-M7 (GPU not supported)
  - i.MX 8M Nano Solo : 1 x Cortex- A53, 1 x Cortex-M7
  - i.MX 8M Nano Solo Lite : 1 x Cortex- A53, 1 x Cortex-M7 (GPU not supported)

Power

- BD71847AMWV PMIC

Memory

- LPDDR4 - 1GB (Expandable up to 8GB)[2,3]
- eMMC Flash - 8GB (Expandable)[3]
- Micro SD slot (Optional)[4]
- QSPI Flash (Optional)

Other On-SOM Features

- WiFi 802.11a/b/g/n/ac + Bluetooth 5.0 Module[4,5]
- Gigabit Ethernet PHY Transceiver
- PCIe to Ethernet PHY (Optional)[6]
- RTC Controller

SODIMM PCB Edge Interfaces

- Gigabit Ethernet x 1 Port (Mini optionally support x 2) [6]
- PCIe x 1 Port (Not supported in Nano)[6]

- SD (4bit) x 1 Port
- USB 2.0 OTG x 1 Port
- USB 2.0 Host x 1 Port (Not available in Nano)
- MIPI CSI x 1 Channel
- MIPI DSI x 1 Channel
- SAI/I2S (Audio Interface) x 1 Port
- Data UART (with CTS & RTS) x 2 Port (One is optional)
- Data UART (without CTS & RTS) x 2 Port (One port is used as Debug Port)
- SAI x 1 (Not available in Nano)
- eCSPI x 3 Port
- I2C x 2 Port
- SPDIF x 1
- JTAG x 1
- PWM x 2 Port
- Power & Management Signals

General Specification

- Power Supply : 3V3, 4A
- Form Factor : 67.6mm X 37mm

1. *There are six configurations of i.MX 8M Mini or i.MX 8M Nano Processor supported by NXP, hence in this document i.MX 8M Mini or i.MX 8M Nano Q/QL/D/DL/S/SL is used to represent either of one based on SOM Part Number.*
2. *The i.MX 8M Mini SoC can support up to 8GB RAM and i.MX 8M Nano SoC can support up to 2GB (32Gb) RAM.*
3. *Memory Size will differ based on iWave's SOM Product Part Number.*
4. *uSDHC1 is shared between Wi-Fi module and micro SD connector, by default it will be connected to Wi-Fi Module. So, on SOM microSD will be an optional feature.*
5. *UART1 interface of i.MX 8M Mini or i.MX 8M Nano is connected to On SOM Bluetooth module in the default configuration. One more UART can be supported with CTS and RTS in SODIMM Edge if Bluetooth is not supported.*
6. *In i.MX 8M Mini SODIMM SOM, PCIe interface signals are connected to both SODIMM PCB Edge Connector and PCIe to Ethernet controller to support 2nd Gigabit Ethernet Port, by default PCIe is connected to SODIMM Edge.*

2.3 i.MX 8M Mini or i.MX 8M Nano SoC

iW-RainboW-G34M i.MX 8M Mini SODIMM SOM can support different i.MX 8M Mini SoCs from NXP. The i.MX 8M Mini Family consists of six processors: i.MX 8M Mini Quad, Quad Lite, Dual, Dual Lite, Solo, Solo Lite. The Major difference between i.MX 8M Mini SoCs are:

- i.MX 8M Mini Quad : 4 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Quad Lite : 4 x Cortex- A53, 1 x Cortex-M4 (VPU not supported)
- i.MX 8M Mini Dual : 2 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Dual Lite : 2 x Cortex- A53, 1 x Cortex-M4 (VPU not supported)
- i.MX 8M Mini Solo : 1 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Solo Lite : 1 x Cortex- A53, 1 x Cortex-M4 (VPU not supported)

The i.MX 8M Mini Family supports ARM Cortex-A53 Core @ 1.6 GHz, ARM Cortex-M4F Core @ 400 MHz, 1080p, VPU, and dual fail over-ready display controllers, 1× 1080p display, including MIPI-DSI. Memory interfaces supporting LPDDR4, DDR4, DDR3L, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, RAW NAND and SD, and a wide range of peripheral I/Os such as PCIe 2.0 provide wide flexibility.

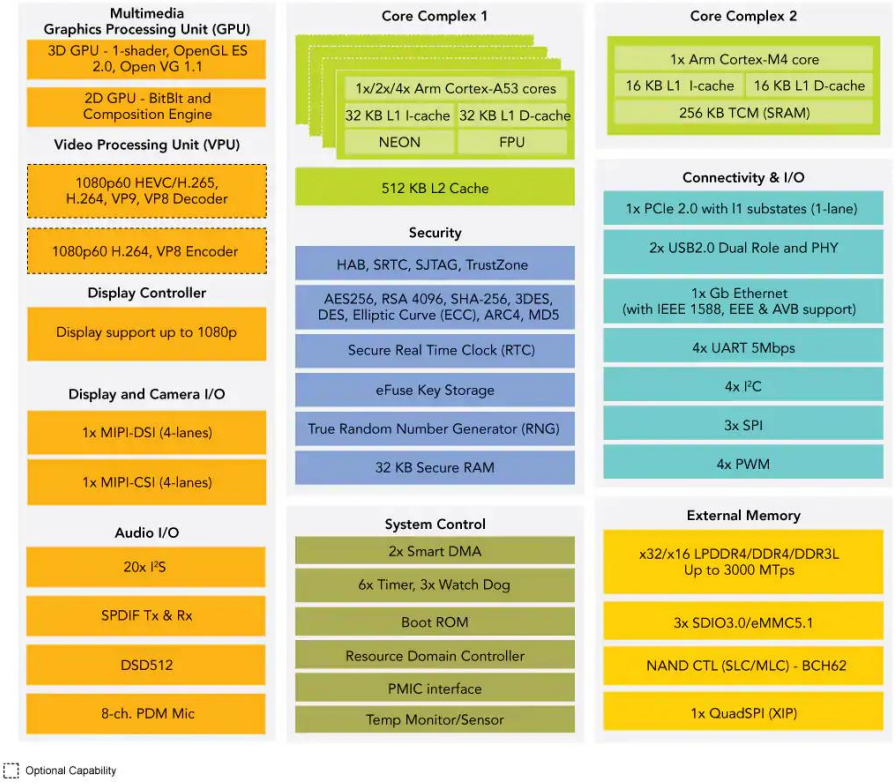

Figure 2: i.MX 8M Mini Block Diagram

Similarly, the iW-RainboW-G37M i.MX 8M Nano SODIMM SOM can support different i.MX 8M Nano SoCs from NXP. The i.MX 8M Nano Family also consists of six processors: i.MX 8M Nano Quad, Quad Lite, Dual, Dual Lite, Solo, Solo Lite. The Major difference between i.MX 8M Nano SoCs are:

- i.MX 8M Nano Quad : 4 x Cortex- A53, 1 x Cortex-M7 (VPU not supported)
- i.MX 8M Nano Quad Lite : 4 x Cortex- A53, 1 x Cortex-M7 (GPU & VPU not supported)
- i.MX 8M Nano Dual : 2 x Cortex- A53, 1 x Cortex-M7(VPU not supported)
- i.MX 8M Nano Dual Lite : 2 x Cortex- A53, 1 x Cortex-M7 (GPU & VPU not supported)
- i.MX 8M Nano Solo : 1 x Cortex- A53, 1 x Cortex-M7(VPU not supported)
- i.MX 8M Nano Solo Lite : 1 x Cortex- A53, 1 x Cortex-M7 (GPU & VPU not supported)

The i.MX 8M Nano Family supports ARM Cortex-A53 Core @ 1.4 GHz, ARM Cortex-M7 Core @ 600 MHz, 1080p, and dual fail over-ready display controllers, 1× 1080p display, including MIPI-DSI. Memory interfaces supporting LPDDR4, DDR4, DDR3L, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, RAW NAND and SD, and a wide range of peripheral I/Os.

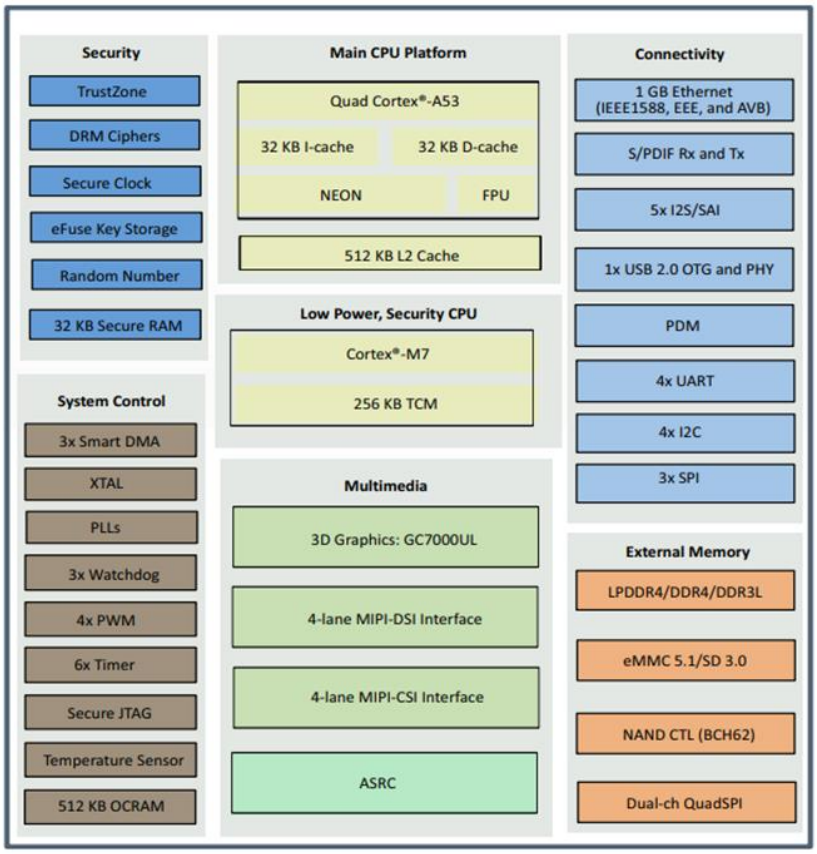

Figure 3: i.MX 8M Nano Block Diagram

Note: The i.MX 8M Mini or i.MX 8M Nano processors offers numerous advanced features, please refer the latest i.MX 8M Mini or i.MX 8M Nano Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 BD71847AMWV PMIC

i.MX 8M Mini or i.MX 8M Nano SODIMM SOM uses Rohm's BD71847AMWV PMIC for on-SOM Power management. The BD71847AMWV is a Power Management Integrated Circuit (PMIC) designed specifically for powering single-core, dual-core, and quad-core SoC's such as NXP-i.MX 8M Mini or i.MX 8M Nano.

The BD71847AMWV is a power management integrated circuit (PMIC) features six high efficiency buck converters and six linear regulators (LDOs) for powering the processor, memory and miscellaneous peripherals. Built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed 1MHz I2C after start up offering flexibility for different system states. The BD71847AMWV (U10) comes in 56pin 7x7 QFN Package and placed on Top side of SOM.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX 8M Mini SODIMM SOM supports 1GB RAM using 32bit LPDDR4 IC and i.MX 8M Nano SODIMM SOM supports 1GB RAM using 16bit LPDDR4 IC. The DDR controller of SoC supports LPDDR4 clock up to 1.5 GHz in Mini and up to 1.6GHz in Nano. The LPDDR4 IC (U6) placed on Top side of the SOM. The RAM size can be expandable up to maximum of 8GB in Mini and up to 2GB in Nano. To customize the LP4DDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports 8GB eMMC as default boot device and storage device. This is connected to eMMC0 version 5.1v controller of the i.MX 8M Mini or i.MX 8M Nano SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash (U16) memory is physically located on bottom side of the SODIMM SOM. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD Connector (Optional)

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM optionally supports Micro SD slot which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J2) is directly connected to the USDHC1 controller of the i.MX 8M Mini or i.MX 8M Nano SoC. The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports configurable I/O voltage levels (3.3V/1.8V) for USDHC1 lines through gpio GPIO1_3. If GPIO1_3 is set to low, then 3.3V IO level is selected for uSDHC1 lines. If GPIO4_3 is set to high, then 1.8V IO level is selected for uSDHC1 lines. The micro SD Connector is physically located on Top side of the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM as shown below.

Note: In default configuration USDHC1 is used for on board Wi-Fi module. Contact iWave Support team if microSD feature is required.

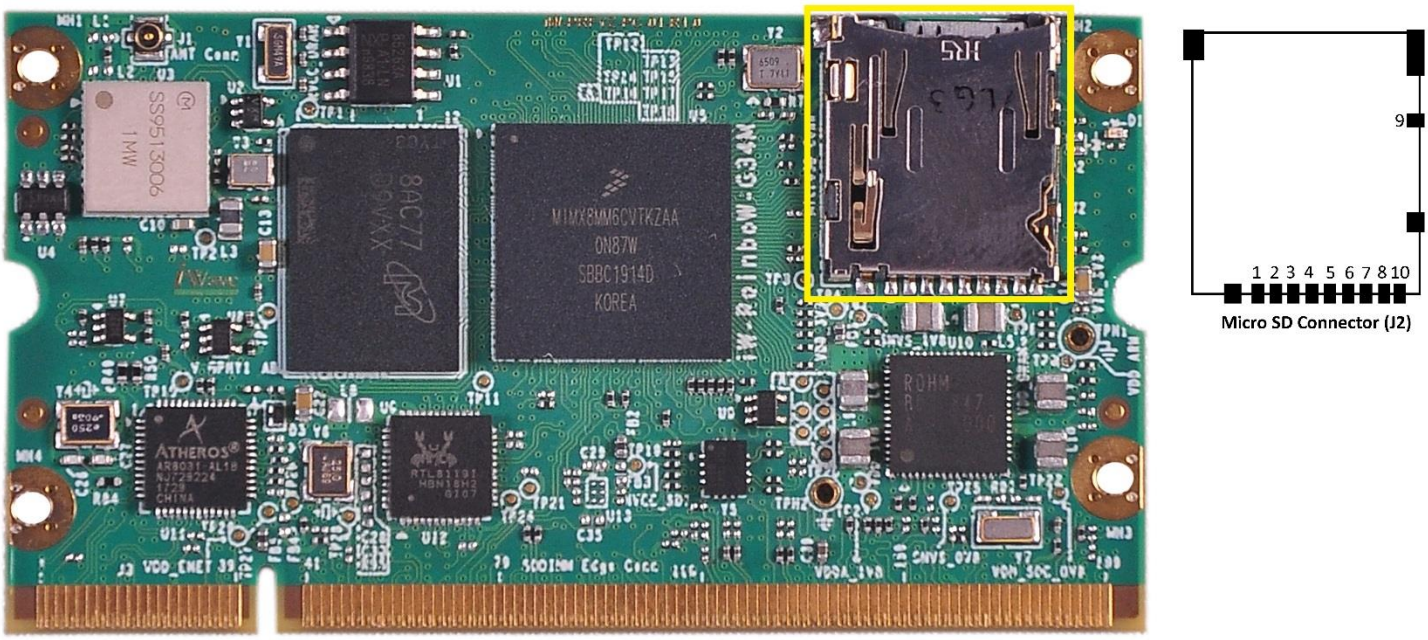

Figure 4: Micro SD Connector

2.5.4 QSPI Flash (Optional)

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM optionally supports 2MB QSPI Flash and can be used as optional boot device. This is connected to QSPI_A controller of the i.MX 8M Mini or i.MX 8M Nano processor and operates at 1.8V Voltage levels. The QSPI flash (U14) is physically located on Bottom side of the SODIMM SOM. The QSPI Flash size can be expandable. For customised QSPI Flash support, contact iWave

2.6 RTC Controller

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports external RTC Controller “PCF85263” On-SOM for Real time clock support. This external RTC Controller IC (U1) is connected to i.MX 8M Mini or i.MX 8M Nano SoC through I2C1 Interface and operates at 3.3V voltage level. In SOM power off condition, this device will take power from SODIMM PCB Edge- Pin No. 183 (VRTC_3V0) coin cell power input and continues to keep the current time.

2.7 Wi-Fi and Bluetooth Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM is integrated with Murata's "LBEE5HY1MW" based Wi-Fi & Bluetooth module. The LBEE5HY1MW module is a very high-performance module based on Cypress CYW43455 combo chipset which supports WiFi IEEE 802.11a/b/g/n/ac + Bluetooth 5.0 BR/EDR/LE standard.

The LBEE5HY1MW module utilizes highly optimized IEEE 802.11 Bluetooth coexistence protocols and supports single stream 1x1 IEEE 802.11 a/b/g/n/ac mode providing up to 390Mbps. The LBEE5HY1MW module features small form factor when integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive switch, Power Management. The LBEE5HY1MW module need external Antenna but it requires a 32.768 kHz clock for sleep operation.

The LBEE5HY1MW module (U3) provides Secure Digital Input Output (SDIO) for interfacing with the host controller for Wi-Fi and UART interface for Bluetooth. The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM uses SoC's UART1 interface for Bluetooth and USDHC1 interface for Wi-Fi in default configuration. In i.MX 8M Mini or i.MX 8M Nano SODIMM SOM, antenna pin of Wi-Fi & Bluetooth module is connected to J1 Connector.

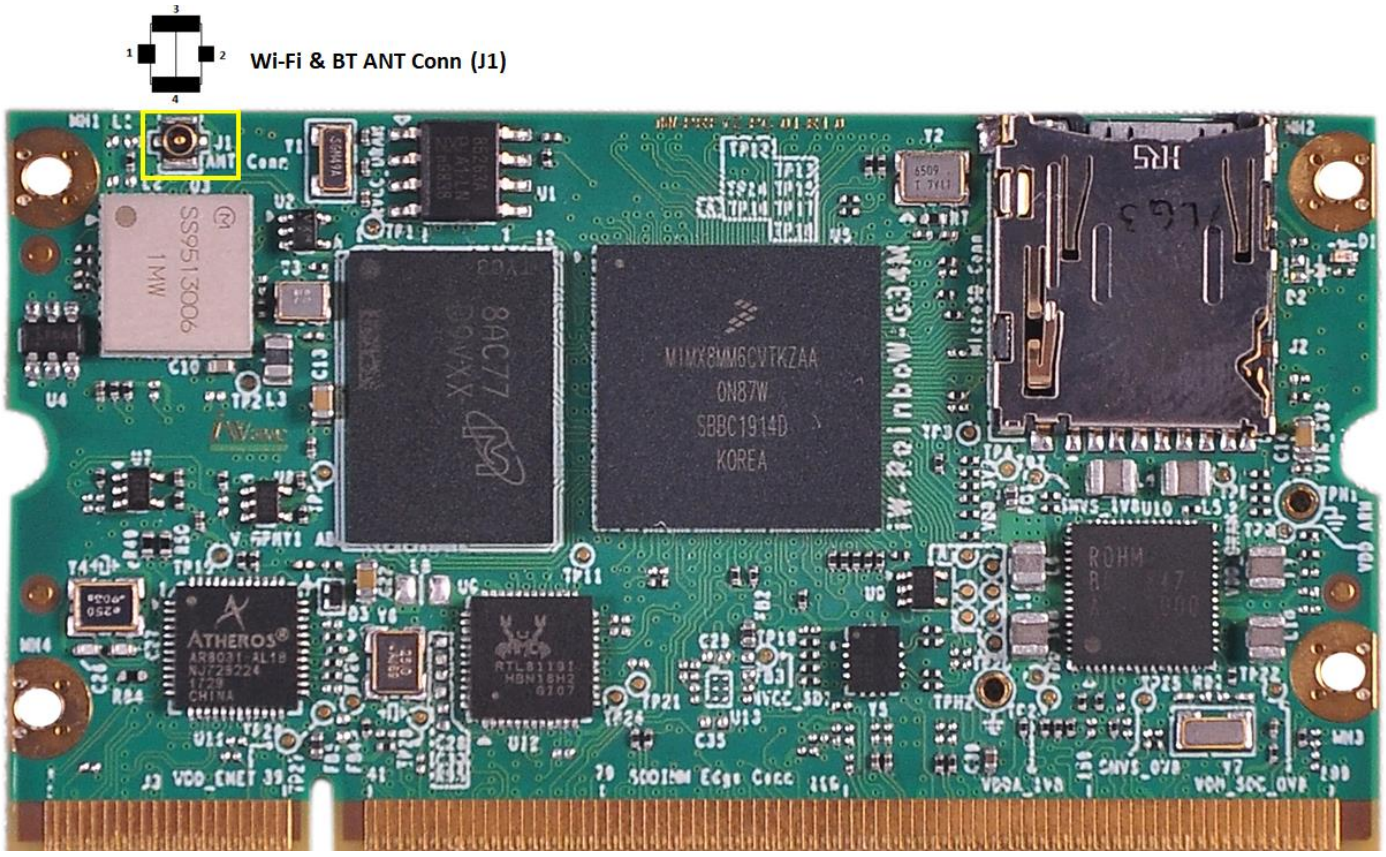

Figure 5: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata Electronics.

Antenna Part Number - : 2042811100 from Molex/ FXP830.24.0100B from Taoglas Limited

Note: The LBEE5HY1MW module supports operating temperature -30°C to 85°C with the default module's firmware. To set the module temperature to industrial grade in firmware, please contact iWave.

2.8 SODIMM PCB Edge Connector

i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Supports JEDEC Physical Standard 200pin SODIMM PCB edge connector for interfaces expansion. The interfaces which are available at SODIMM Edge connector are explained in the following sections.

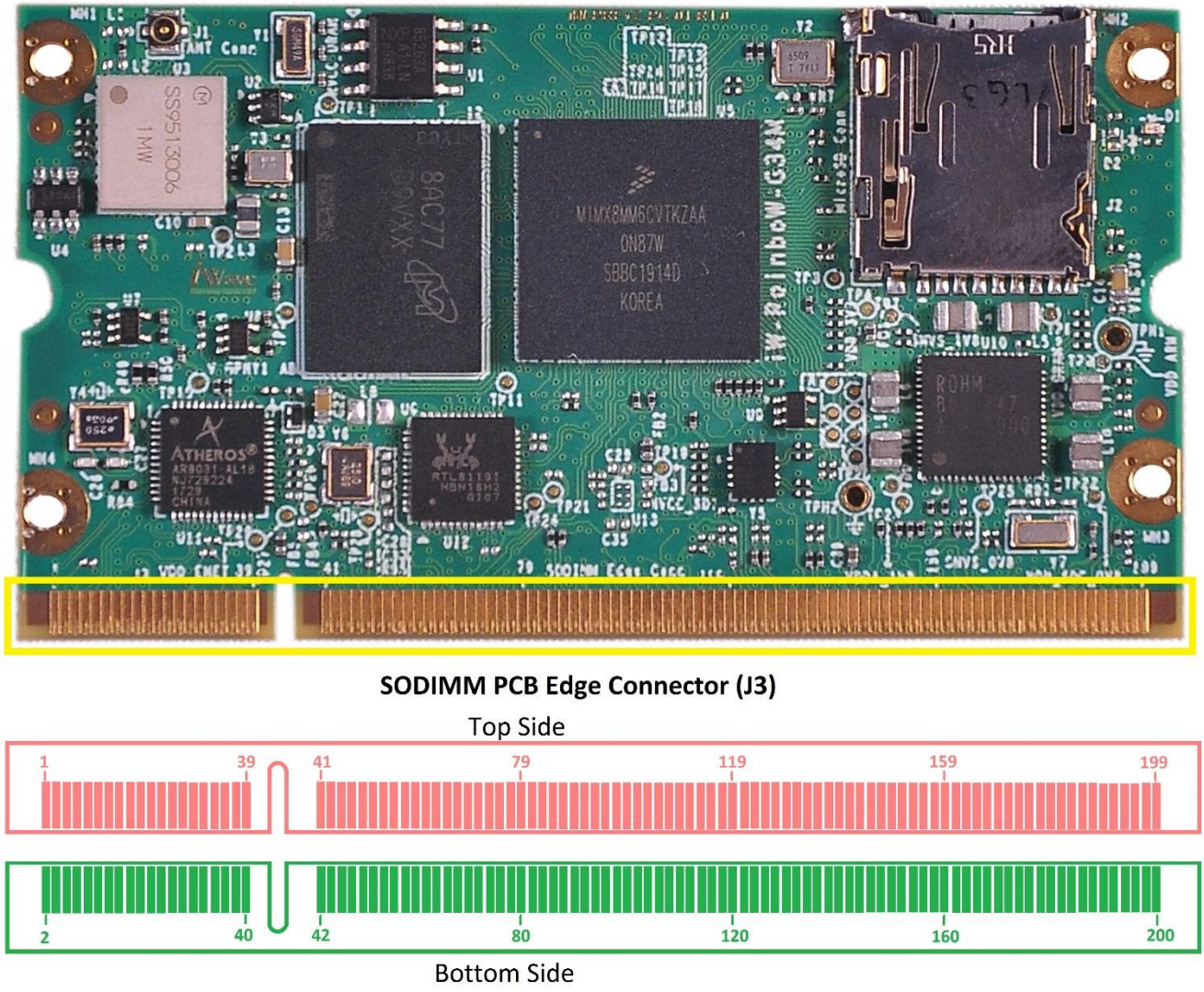

Figure 6: SODIMM Edge Connector

Number of Pins - : 200

Connector Part - : Not Applicable (On Board PCB Edge connector)

Mating Connector - : 1473005-1 from TE Connectivity

Table 3: SODIMM Edge Connector Pinouts

Signal	SODIMM Pin (Top)	SODIMM Pin (Bottom)	Signal
GND	1	2	GPHY1_ATXRXM
VDVDH_GPHY1*	3	4	GPHY1_ATXRXP
GND	5	6	GPHY1_BTXRXM
UART3_RXD	7	8	GPHY1_BTXRXP
UART3_TXD	9	10	NC
GPHY1_LINK_LED2	11	12	GPHY1_ACTIVITY_LED1
GND	13	14	GPHY1_CTXRXM
GPHY1_DTXRXM	15	16	GPHY1_CTXRXP
GPHY1_DTXRXP	17	18	I2C3_SCL*
I2C3_SDA*	19	20	VIN_3V3
NC	21	22	NC
NC	23	24	NC
NC	25	26	NC
GND	27	28	NC
NC	29	30	GPHY2_ACTIVITY_LED1 (NC in Nano) *
NC	31	32	VIN_3V3
GPHY2_LINK_LED2 (NC in Nano) *	33	34	GPHY2_ATXRXM (NC in Nano) *
GPHY2_BTXRXM (NC in Nano) *	35	36	GPHY2_ATXRXP (NC in Nano) *
GPHY2_BTXRXP (NC in Nano) *	37	38	UART2_CTS_B(SAI3_RXC)
USB2_OTG_OC(GPIO1_15)	39	40	GND
Key			Key
GND	41	42	GPHY2_CTXRXM (NC in Nano) *
GPHY2_DTXRXM (NC in Nano) *	43	44	GPHY2_CTXRXP (NC in Nano) *
GPHY2_DTXRXP (NC in Nano) *	45	46	VIN_3V3
SAI1_RXD0 (NC in Nano)	47	48	MIPI_DSI_DATA0_N
VDVDH_GPHY2 (NC in Nano) *	49	50	MIPI_DSI_DATA0_P
GND	51	52	MIPI_DSI_DATA1_N
MIPI_DSI_DATA2_N	53	54	MIPI_DSI_DATA1_P
MIPI_DSI_DATA2_P	55	56	MIPI_DSI_DATA3_N
MIPI_DSI_CLK_N	57	58	MIPI_DSI_DATA3_P
MIPI_DSI_CLK_P	59	60	VIN_3V3
SAI5_RX_DATA0(SAI5_RXD0)	61	62	ECSPI2_SS0
ECSPI2_MISO	63	64	GPIO_CLK(SAI5_MCLK)
GND	65	66	ECSPI2_SCLK
SAI5_TX_DATA0(SAI5_RXD3)	67	68	SAI1_RXD2 (NC in Nano)
NC	69	70	ECSPI2_MOSI
GPIO1_6	71	72	VIN_3V3
GPIO1_7	73	74	SAI1_RXC (NC in Nano)
UART2_RTS_B(SAI3_RXD)	75	76	USB1_OTG_OC(GPIO1_13)

Signal	SODIMM Pin (Top)	SODIMM Pin (Bottom)	Signal
USB1_ID	77	78	USB1_OTG_PWR(GPIO1_12)
GND	79	80	ECSPI1_SCLK
USB1_DP	81	82	CLKOUT1
USB1_DN	83	84	CLKOUT2
CLKIN1	85	86	NC
CLKIN2	87	88	VIN_3V3
SAI5_TX_SYNC(SAI5_RXD1)	89	90	SAI5_TX_BCLK(SAI5_RXD2)
SAI5_RX_BCLK(SAI5_RXC)	91	92	SAI5_RX_SYNC(SAI5_RXFS)
NC	93	94	ECSPI1_MISO
GND	95	96	ECSPI1_MOSI
ECSPI1_SS0	97	98	UART1_TXD*
UART1_RXD*	99	100	UART1_CTS_B*
UART1_RTS_B*	101	102	UART2_TX(SAI3_TXC)
UART2_RX(SAI3_TXFS)	103	104	SAI1_RXFS (NC in Nano)
SD2_CD_B	105	106	VIN_3V3
SD2_DATA0	107	108	SD2_CMD
SD2_CLK	109	110	NC
SD2_DATA1	111	112	SD2_DATA2
GND	113	114	SD2_DATA3
I2C2_SDA	115	116	I2C2_SCL
UART4_RXD	117	118	UART4_TXD
NC	119	120	NC
BCONFIG_1(GPIO5_1)*	121	122	NC
SAI1_RXD5 (NC in Nano)	123	124	VIN_3V3
PWM2_OUT(I2C4_SCL)	125	126	BCONFIG_0(GPIO1_9)*
PCIE_TXP (NC in Nano)	127	128	PCIE_RXP (NC in Nano)
PCIE_TXN (NC in Nano)	129	130	PCIE_RXN (NC in Nano)
GND	131	132	GPIO_RESET(GPIO5_2)
W_DISABLE(GPIO1_11)	133	134	PCIE_WAKE_B(GPIO1_10)
PCIE_REFCLK_DP (NC in Nano)	135	136	GPIO1_1
PCIE_REFCLK_DM (NC in Nano)	137	138	PWM1_OUT(I2C4_SDA)
USB2_ID (NC in Nano)	139	140	USB2_OTG_PWR(GPIO1_14)
USB_OTG2_VBUS (NC in Nano)	141	142	VIN_3V3
SAI1_TXFS (NC in Nano)	143	144	SAI1_RXD7 (NC in Nano)
SAI1_MCLK (NC in Nano)	145	146	GPIO1_8
GPIO1_5	147	148	SAI1_RXD3 (NC in Nano)
SAI1_RXD4 (NC in Nano)	149	150	MIPI_CSI_CLK_N
GND	151	152	MIPI_CSI_CLK_P
I2C3_SCL	153	154	SAI1_TXD7 (NC in Nano)
I2C3_SDA	155	156	SAI1_TXD0 (NC in Nano)
SAI1_TXC (NC in Nano)	157	158	SAI1_RXD1 (NC in Nano)

Signal	SODIMM Pin (Top)	SODIMM Pin (Bottom)	Signal
MIPI_CSI_DATA1_N	159	160	VIN_3V3
MIPI_CSI_DATA1_P	161	162	MIPI_CSI_DATA2_N
SAI1_TXD4 (NC in Nano)	163	164	MIPI_CSI_DATA2_P
SAI1_TXD5 (NC in Nano)	165	166	SAI1_TXD1 (NC in Nano)
SAI1_TXD2 (NC in Nano)	167	168	MIPI_CSI_DATA0_N
GND	169	170	MIPI_CSI_DATA0_P
SAI1_TXD6 (NC in Nano)	171	172	MIPI_CSI_DATA3_N
SAI1_TXD3 (NC in Nano)	173	174	MIPI_CSI_DATA3_P
SAI1_RXD6 (NC in Nano)	175	176	SPDIF_EXT_CLK
SPDIF_RX	177	178	SPDIF_TX
ON_OFF	179	180	VIN_3V3
ECSPI3_SS0(UART2_TXD)	181	182	BOOT_MODE0
VRTC_3V0	183	184	BOOT_MODE1
GND	185	186	GND
n_RST_OUT	187	188	USB2_DP (NC in Nano)
ECSPI3_SCLK(UART1_RXD)	189	190	USB2_DN (NC in Nano)
JTAG_TDO	191	192	VIN_3V3
JTAG_TRST_B(BOOT_MODE2)	193	194	ECSPI3_MOSI(UART1_TXD)
JTAG_TDI	195	196	ECSPI3_MISO(UART2_RXD)
JTAG_TCK	197	198	GND
JTAG_TMS	199	200	USB_OTG1_VBUS

** Optional feature, by default not supported.*

2.8.1 Gigabit Ethernet

The i.MX 8M Mini SODIMM SOM supports two Gigabit Ethernet capable ports (GBE0) and (GBE1) on SODIMM PCB Edge connector where GBE1 port is optional in default SOM configuration. The i.MX 8M Nano SODIMM SOM supports single Gigabit Ethernet port (GBE0) on SODIMM Edge connector.

In that, First Ethernet Gigabit Ethernet0 (GBE0) port of SODIMM PCB Edge connector is supported through i.MX 8M Mini or i.MX 8M Nano SoC's ENET controller. The MAC is integrated in the i.MX 8M Mini or i.MX 8M Nano SoC ENET and connected to the external Gigabit Ethernet PHY "AR8031" from Atheros/Qualcomm on SOM through RGMII interface. The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. i.MX 8M Mini or i.MX 8M Nano SODIMM SOM also supports Link and Activity indication LED control signals for GBE0 port to SODIMM PCB Edge connector.

For more details on GBE0 pinouts on SODIMM PCB Edge connector, refer below Table:

SODIMM Pin No.	SOIDMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
2	GPHY1_ATXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
4	GPHY1_ATXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.
6	GPHY1_BTXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.
8	GPHY1_BTXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
14	GPHY1_CTXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
16	GPHY1_CTXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
15	GPHY1_DTXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.
17	GPHY1_DTXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
3	VDVDH_GPHY1	NA	NC	NC.
11	GPHY1_LINK_LED2	NA	O, 3.3V CMOS	Gigabit Ethernet link status LED.
12	GPHY1_ACTIVITY_LED1	NA	O, 3.3V CMOS	Gigabit Ethernet activity status.

Second Ethernet Gigabit Ethernet1 (GBE1) port of SODIMM PCB Edge connector is supported on SOM through PCIe to Ethernet controller "RTL8119" from Realtek. This Ethernet controller is interfaced with i.MX 8M Mini SoC using PCIe Lane. This controller combines IEEE 802.3 compliant MAC and Ethernet transceiver. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. It also supports Link and Activity indication LED control signals to SODIMM PCB Edge connector.

Note: In i.MX 8M Mini SODIMM SOM, PCIe lane signals are having option to connect to PCIe to Ethernet controller and SODIMM PCB Edge Connector. By default, PCIe lane signals are connected to SODIMM PCB Edge Connector. So GBE1 port is optional in default SOM configuration.

For more details on GBE1 pinouts on SODIMM PCB Edge connector, refer below Table (Applicable for Mini only):

SODIMM Pin No.	SOIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
34	GPHY2_ATXRXM	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 negative.
36	GPHY2_ATXRXP	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 positive.
35	GPHY2_BTXRXM	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 negative.
37	GPHY2_BTXRXP	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 positive.
42	GPHY2_CTXRXM	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 negative.
44	GPHY2_CTXRXP	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 positive.
43	GPHY2_DTXRXM	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 negative.
45	GPHY2_DTXRXP	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 positive.
49	VDVDH_GPHY2	NA	NC	NC.
33	GPHY2_LINK_LED2	NA	O, 3.3V CMOS	Ethernet Activity status LED.
30	GPHY2_ACTIVITY_LED1	NA	O, 3.3V CMOS	1000Mbps Ethernet link status LED

Note: PCIe is not supported in i.MX 8M Nano SODIMM SOM. So, 2nd Ethernet is also not supported.

2.8.2 PCIe Interface (Not available in Nano)

The i.MX 8M Mini SoC supports single Lane PCI Express -2.0 channels. In i.MX 8M Mini SODIMM SOM PCIe lane is directly connected to SODIMM Edge connector by default and optionally connected to On-SOM PCIe to Ethernet controller. 100MHz external clock oscillator output is connected to SoC & SODIMM PCB Edge for PCIe reference clock. Also, PCIe wake is supported on SODIMM PCB Edge connector from i.MX 8M Mini SoC IO GPIO1_10.

Note: PCIe differential transmitter lines are ac coupled on SOM itself. Also, PCIe differential clock lines from external clock oscillator are having On-SOM termination resistors and so no external termination is required.

For more details on PCIe pinouts on SODIMM PCB Edge connector, refer below table (Applicable only for Mini):

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
135	PCIE_REFCLK_DP	NA	O, PCIe	PCIe Clock Positive. *Note: This signal is coming from 100MHz External Oscillator in SOM.* *100MHz Clock Oscillator output for PCIe Clock Positive is optionally connected to On-SOM PCIe to Ethernet controller through resistor and default not populated.*
137	PCIE_REFCLK_DM	NA	O, PCIe	PCIe Clock Negative. *Note: This signal is coming from 100MHz External Oscillator in SOM.* *100MHz Clock Oscillator output for PCIe Clock Negative is optionally connected to On-SOM PCIe to Ethernet controller through resistor and default not populated.*
128	PCIE_RXP	PCIE_RXN_P/B19	I, PCIe	PCIe Receive Positive. *Note: PCIe Receiver Positive is optionally connected to On-SOM PCIe to Ethernet controller through resistor and default not populated*
130	PCIE_RXN	PCIE_RXN_N/A19	I, PCIe	PCIe Receive Negative. *Note: PCIe Receiver Negative is optionally connected to On-SOM PCIe to Ethernet controller through resistor and default not populated*
127	PCIE_TXP	PCIE_TXN_P/B20	O, PCIe / 0.1uF AC Couple	PCIe Transmit Positive. *Note: PCIe Transmitter Positive is optionally connected On-SOM PCIe to Ethernet controller*

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
				through capacitor and default not populated.
129	PCIE_TXN	PCIE_TXN_N/A20	O, PCIe / 0.1uF AC Couple	PCIe Transmit Negative. *Note: PCIe Transmitter Negative is optionally connected On-SOM PCIe to Ethernet controller through capacitor and default not populated.*
134	PCIE_WAKE_B(GPIO1_10)	GPIO1_IO10/AD10	O, 3.3V CMOS	PCIe Wake.

2.8.3 SD Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports 4bit SD interface over SODIMM PCB Edge connector which can be used to connect SD card as Mass storage or optional boot device. uSDHC2 controller of the i.MX 8M Mini or i.MX 8M Nano SoC is used to support SODIMM SD interface. It supports 1-bit or 4-bit transfer mode for SD/SDIO and works up to UHS-I mode @ up to 208 MHz. The I/O voltage level of USDHC2 lines can be set to 1.8V or 3.3V based on PMIC configuration through SoC signal GPIO1_4. If GPIO1_4 is set to low, then 3.3V IO level is selected for uSDHC2 lines. If GPIO1_4 is set to high, then 1.8V IO level is selected for uSDHC2 lines.

For more details on SD pinouts on SODIMM PCB Edge connector, refer below Table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
108	SD2_CMD	SD2_CMD/W24	IO, 1.8/3.3V CMOS/10K PU	SD command.
105	SD2_CD_B	SD2_CD_B/AA26	I, 3.3V/CMOS	SD Card Detect.
109	SD2_CLK	SD2_CLK/W23	O, 1.8/3.3V CMOS	SD Clock.
107	SD2_DATA0	SD2_DATA0/AB23	IO, 1.8/3.3V CMOS/10K PU	SD data 0.
111	SD2_DATA1	SD2_DATA1/AB24	IO, 1.8/3.3V CMOS/10K PU	SD data 1.
112	SD2_DATA2	SD2_DATA2/V24	IO, 1.8/3.3V CMOS/10K PU	SD data 2.
114	SD2_DATA3	SD2_DATA3/V23	IO, 1.8/3.3V CMOS/10K PU	SD data 3.

2.8.4 USB Interface

The i.MX 8M Mini SoC supports two USB2.0 OTG while i.MX 8M Nano SoC supports single USB2.0 OTG. The available USB controllers of the i.MX 8M Mini or i.MX 8M Nano is connected to SODIMM OTG pins.

For more details on USB1 2.0 pinouts near SODIMM edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
81	USB1_DP	USB1_DP/B22	IO, USB	USB Port1 Data Positive. *Note: Same signal is optionally connected to SODIMM Edge Pin No. 188 USB2 Data Positive for USB 2.0 OTG through resistor and default not populated.*
83	USB1_DN	USB1_DN/A22	IO, USB	USB Port1 Data Negative. *Note: Same signal is optionally connected to SODIMM Edge Pin No.190 USB2 Data* Negative *for USB 2.0 OTG through resistor and default not populated.*
78	USB1_OTG_PWR(GPIO1_12)	GPIO1_IO12/AB10	IO, 3.3V CMOS	USB Port1 Power Enable
200	USB_OTG1_VBUS	NA	I, 5V Power	USB1 host power detection, when this port is used as a device.
77	USB1_ID	NA	I, 3.3V CMOS/PU 10K	USB1 OTG ID.
76	USB1_OTG_OC(GPIO1_13)	GPIO1_IO13/AD9	I, 3.3V CMOS	USB Port1 Over Current Indicator.

For more details on USB2 2.0 pinouts near SODIMM edge connector, refer below table (Not available in Nano):

SODIMM Pin No.	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
188	USB2_DP	USB2_DP/B23	IO, USB	USB Port2 Data Positive.
190	USB2_DN	USB2_DN/A23	IO, USB	USB Port2 Data Negative.
140	USB2_OTG_PWR(GPIO1_14)	GPIO1_IO14/AC9	IO, 3.3V CMOS	USB Port2 Power Enable
141	USB_OTG2_VBUS	NA	I, 5V Power	USB2 host power detection, when this port is used as a device.
139	USB2_ID	NA	I,3.3V CMOS/PU 10K	USB2 OTG ID.
39	USB2_OTG_OC(GPIO1_15)	GPIO1_IO15/AB9	I, 3.3V CMOS	USB Port2 Over Current Indicator.

2.8.5 MIPI CSI Camera

The i.MX 8M Mini or i.MX 8M Nano SOIDMM SOM supports one 4-lane MIPI CSI 2.0 serial camera interface on SODIMM PCB Edge connector, which operates up to a maximum bit rate of 1.5 Gbps. The i.MX 8M Mini or i.MX 8M Nano SoC is compliant to D-PHY specification v1.2 and MIPI CSI2 Specification v1.3 except for C-PHY feature. The D-PHY interface Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The D-PHY interface Controller takes care of all packet formatting details and transmission over the MIPI bus.

For more details on MIPI CSI pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
152	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P/B16	I, MIPI	MIPI CSI differential Clock positive.
150	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N/A16	I, MIPI	MIPI CSI differential Clock negative.
170	MIPI_CSI_DATA0_P	MIPI_CSI_D0_P/B14	I, MIPI	MIPI CSI differential data lane 0 positive.
168	MIPI_CSI_DATA0_N	MIPI_CSI_D0_N/A14	I, MIPI	MIPI CSI differential data lane 0 negative.
161	MIPI_CSI_DATA1_P	MIPI_CSI_D1_P/B15	I, MIPI	MIPI CSI differential data lane 1 positive.
159	MIPI_CSI_DATA1_N	MIPI_CSI_D1_N/A15	I, MIPI	MIPI CSI differential data lane 1 negative.
164	MIPI_CSI_DATA2_P	MIPI_CSI_D2_P/B17	I, MIPI	MIPI CSI differential data lane 2 positive.
162	MIPI_CSI_DATA2_N	MIPI_CSI_D2_N/A17	I, MIPI	MIPI CSI differential data lane 2 negative.
174	MIPI_CSI_DATA3_P	MIPI_CSI_D3_P/B18	I, MIPI	MIPI CSI differential data lane 3 positive.
172	MIPI_CSI_DATA3_N	MIPI_CSI_D3_N/A18	I, MIPI	MIPI CSI differential data lane 3 negative.
153	I2C3_SCL	I2C3_SCL/ E10	O, 3.3V OD/ 4.7K PU	I2C Clock for MIPI Camera.
155	I2C3_SDA	I2C3_SDA/ F10	IO, 3.3V OD/ 4.7K PU	I2C Data for MIPI Camera.
147	GPIO1_5	GPIO1_IO05/AF12	O, 3.3V CMOS	MIPI Camera Reset signal

2.8.6 MIPI DSI Display Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports one four lane MIPI DSI display interfaces on SODIMM PCB Edge connector. i.MX 8M Mini or i.MX 8M Nano SoC's MIPI DSI controller with integrated D-PHY is directly connected to SODIMM PCB Edge connector.

The i.MX 8M Mini or i.MX 8M Nano SoC MIPI DSI complies to standard Specification for Display Serial Interface Version 1.01 or 11 The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The D-PHY interface of the DSI Host Controller Core supports Protocol-to-PHY Interface (PPI) in 1.0Gbps / 1.5Gbps MIPI DPHY and it Supports pixel format: 16bpp, 18bpp packed, 18bpp loosely packed (3-byte format), and 24bpp.

For more details on DSI pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
59	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P/B11	O, MIPI	MIPI DSI differential Clock positive
57	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N/A11	O, MIPI	MIPI DSI differential Clock negative
50	MIPI_DSI_DATA0_P	MIPI_DSI_D0_P/B9	O, MIPI	MIPI DSI differential data lane 0 positive
48	MIPI_DSI_DATA0_N	MIPI_DSI_D0_N /A9	O, MIPI	MIPI DSI differential data Lane 0 negative
54	MIPI_DSI_DATA1_P	MIPI_DSI_D1_P/B10	O, MIPI	MIPI DSI differential data lane 1 positive
52	MIPI_DSI_DATA1_N	MIPI_DSI_D1_N/A10	O, MIPI	MIPI DSI differential data lane 1 negative
55	MIPI_DSI_DATA2_P	MIPI_DSI_D2_P/B12	O, MIPI	MIPI DSI differential data lane 2 positive
53	MIPI_DSI_DATA2_N	MIPI_DSI_D2_N/A12	O, MIPI	MIPI DSI differential data lane 2 negative
58	MIPI_DSI_DATA3_P	MIPI_DSI_D3_P/B13	O, MIPI	MIPI DSI differential data lane 3 positive
56	MIPI_DSI_DATA3_N	MIPI_DSI_D3_N/A13	O, MIPI	MIPI DSI differential data lane 3 negative
153	I2C3_SCL	I2C3_SCL/ E10	O, 3.3V OD/ 4.7K PU	I2C Clock for Display.
155	I2C3_SDA	I2C3_SDA/ F10	IO, 3.3V OD/ 4.7K PU	I2C Data for Display.
132	GPIO_RESET(GPIO5_2)	SAI3_MCLK/ AD6	O, 3.3V CMOS	This GPIO is used for Display reset *Note: This signal is used as GPIO reset for Carrier Peripherals*
136	GPIO 1_1	GPIO1_IO01/ AF14	O, 3.3V CMOS	Used for Display Touch reset
146	GPIO1_8	GPIO1_IO08/AG10	I, 3.3V CMOS	Used for Display Touch Interrupt

2.8.7 Audio Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports one I2S interface on SODIMM Edge connector from SoC's SAI5 channel. In i.MX 8M Mini or i.MX 8M Nano SODIMM SOM SAI5 channel is directly connected to SODIMM Edge connector by default and optionally connected to On-SOM Wi-fi module. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits and Supports graceful restart after FIFO error.

In i.MX 8M Mini or i.MX 8M Nano SODIMM SOM the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on Audio Interface pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
64	GPIO_CLK(SAI5_MCLK)	SAI5_MCLK/AD15	O,3.3V CMOS/33E Series	Master Clock for Audio codec
89	SAI5_TX_SYNC(SAI5_RXD1)	SAI5_RXD1/AC14	O, 3.3V CMOS	SAI5 Transmitter Frame Sync *Note: SAI5_TX_SYNC is optionally connected to On-SOM Wi-fi module through resistor and default not populated.*
67	SAI5_TX_DATA0(SAI5_RXD3)	SAI5_RXD3/AC13	O, 3.3V CMOS	SAI5 Transmit Data Lane 0 *Note: SAI5_TX_DATA0 is optionally connected to On-SOM Wi-fi module through resistor and default not populated.*
61	SAI5_RX_DATA0(SAI5_RXD0)	SAI5_RXD0/AD18	I, 3.3V CMOS	SAI5 Receive Data Lane 0 *Note: SAI5_TX_DATA0 is optionally connected to On-SOM Wi-fi module through resistor and default not populated.*
90	SAI5_TX_BCLK(SAI5_RXD2)	SAI5_RXD2/AD13	O, 3.3V CMOS/ 33E Series	SAI5 Transmitter Bit Clock *Note: SAI5_TX_BCLK is optionally connected On-SOM Wi-fi module through resistor and default not populated.*

2.8.8 UART Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports four UART channels where two UART1 & UART2 are with CTS and RTS and two UART3 & UART4 are without. The i.MX 8M Mini or i.MX 8M Nano SoC's UART2, UART3, UART4 are connected to SODIMM Edge connector whereas UART1 is optionally connected to the SODIMM Edge connector. By default, UART1 is connected to on SOM Bluetooth module. UART1, UART2 & UART3 can be used for any data communication. UART4 of the SoC is connected to SODIMM Edge connector and used as Debug UART.

For more details on UART pinouts on SODIMM PCB Edge connector, refer below table:

SOIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
98	NC	NA	NA	Default NC. *Note: Optionally connect to UART1_TXD.This pin is optionally connected to i.MX 8M Mini or i.MX 8M Nano SoC's UART1_TX(SAI2_RXFS) through 1.8V to 3.3V voltage translator and default not populated. UART1_TX(SAI2_RXFS) is by default connected to On -SOM Bluetooth.*
99	NC	NA	NA	Default NC. *Note: Optionally connect to UART1_RXD. This pin is optionally connected to i.MX 8M Mini or i.MX 8M Nano SoC's UART1_RX(SAI2_RXC) through 1.8V to 3.3V voltage translator and default not populated. UART1_RX(SAI2_RXC) is by default connected to On -SOM Bluetooth.*
101	NC	NA	NA	Default NC. *Note: Optionally connect to UART1_RTS_B. This pin is optionally connected to i.MX 8M Mini or i.MX 8M Nano SoC's UART1_RTS_B(SAI2_RXD0) through 1.8V to 3.3V voltage translator and default not populated. UART1_RTS_B(SAI2_RXD0) is by default connected to On -SOM Bluetooth.*
100	NC	NA	NA	Default NC. *Note: Optionally connect to UART1_CTS_B. This pin is optionally connected to i.MX 8M Mini or i.MX 8M Nano SoC's UART1_CTS_B(SAI2_TXFS) through*

SOIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
				1.8V to 3.3V voltage translator and default not populated. UART1_CTS_B(SAI2_TXFS) is by default connected to On -SOM Bluetooth.
102	UART2_TX(SAI3_TXC)	SAI3_TXC/AG6	O, 3.3V CMOS	UART2 Transmitter.
103	UART2_RX(SAI3_TXFS)	SAI3_TXFS/AC6	I, 3.3V CMOS	UART2 Receiver.
75	UART2_RTS_B(SAI3_RXD)	SAI3_RXD/AF7	I, 3.3V CMOS	UART2 Request to Send.
38	UART2_CTS_B(SAI3_RXC)	SAI3_RXC/AG7	O, 3.3V CMOS	UART2 Clear to Send.
9	UART3_TXD	UART3_TXD/D18	O, 3.3V CMOS	UART3 Transmitter
7	UART3_RXD	UART3_RXD/E18	I, 3.3V CMOS	UART3 Receiver.
118	UART4_TXD	UART4_TXD/F18	O, 3.3V CMOS	Debug UART Transmitter.
117	UART4_RXD	UART4_RXD/F19	I, 3.3V CMOS	Debug UART Receiver.

2.8.9 SPI Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports 3 Enhanced Configurable SPI interface ECSPI1, ECSPI2, ECSPI3 on SODIMM PCB Edge connector. The i.MX 8M Mini or i.MX 8M Nano SoC's Enhanced Configurable Serial Peripheral Interface (ECSPI) module is full-duplex, synchronous with data rate up to 52 Mbit/s, four-wire serial communication block and Master/Slave configurable with maximum clock speed of 20MHz.

For more details on ECSPI1 pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
97	ECSPI1_SS0	ECSPI1_SS0/B6	O, 3.3V CMOS	SPI1 Chip Select 0
80	ECSPI1_SCLK	ECSPI1_SCLK/D6	O, 3.3V CMOS/ 33E Series	SPI1 Clock
94	ECSPI1_MISO	ECSPI1_MISO/A7	I, 3.3V CMOS	SPI1 Master In Slave Out
96	ECSPI1_MOSI	ECSPI1_MOSI/B7	O, 3.3V CMOS	SPI1 Master Out Slave In

For more details on ECSPI2 pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
62	ECSPI2_SS0	ECSPI2_SS0/A6	O, 3.3V CMOS	SPI2 Chip Select 0
66	ECSPI2_SCLK	ECSPI2_SCLK/E6	O, 3.3V CMOS/ 33E Series	SPI2 Clock
63	ECSPI2_MISO	ECSPI2_MISO/A8	I, 3.3V CMOS	SPI2 Master In Slave Out
70	ECSPI2_MOSI	ECSPI2_MOSI/B8	O, 3.3V CMOS	SPI2 Master Out Slave In

For more details on ESPI3 pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
181	ECSPI3_SS0(UART2_TXD)	UART2_TXD/E15	O, 3.3V CMOS	SPI3 Chip Select 0

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
189	ECSPI3_SCLK(UART1_RXD)	UART1_RXD/E14	O, 3.3V CMOS/ 33E Series	SPI3 Clock
196	ECSPI3_MISO(UART2_RXD)	UART2_RXD/F15	I, 3.3V CMOS	SPI3 Master In Slave Out
194	ECSPI3_MOSI(UART1_TXD)	UART1_TXD/F13	O, 3.3V CMOS	SPI3 Master Out Slave In

2.8.10 I2C Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports two I2C interface on SODIMM PCB Edge connector. i.MX 8M Mini or i.MX 8M Nano SoC's I2C2 & I2C3 interfaces are connected to SODIMM PCB Edge connector for I2C whereas i.MX 8M Mini or i.MX 8M Nano SoC's I2C1 interface is connected to On-SOM peripherals (PMIC with slave address 0x4B & RTC Controller with slave address 0x51).

For more details on I2C Interface pinouts on SODIMM PCB edge connector, refer the below table.

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
116	I2C2_SCL	I2C2_SCL/D10	O, 3.3V OD/ 4.7K PU	I2C2 Serial Clock for General Purpose
115	I2C2_SDA	I2C2_SDA/D9	IO, 3.3V OD/ 4.7K PU	I2C2 Serial Data for General Purpose.
153	I2C3_SCL	I2C3_SCL / E10	O, 3.3V OD/ 4.7K PU	I2C3 Serial Clock for General Purpose. *Note: I2C3_SCL is optionally connected to SODIMM Edge Pin No. 18 through resistor and default not populated*
155	I2C3_SDA	I2C3_SDA / F10	IO, 3.3V OD/ 4.7K PU	I2C3 Serial Data for General Purpose. *Note: I2C3_SDA is optionally connected to SODIMM Edge Pin No. 19 through resistor and default not populated*

2.8.11 JTAG Interface

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports JTAG interface for SoC debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG).

For more details on JTAG pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
193	NC	JTAG_TRST_B/C27	I, 3.3V CMOS/ 10K PU	JTAG test reset signal. *Note: By default, do not connect to JTAG_TRST_B*

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
195	JTAG_TDI	JTAG_TDI/E27	I, 3.3V CMOS/ 10K PU	JTAG test data input.
199	JTAG_TMS	JTAG_TMS/F27	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
197	JTAG_TCK	JTAG_TCK/F26	I, 3.3V CMOS/ 10K PD	JTAG test Clock.
191	JTAG_TDO	JTAG_TDO/E26	O, 3.3V CMOS/ 10K PU	JTAG test data output.

2.8.12 GPIO Interface

The i.MX 8M Mini or i.MX 8M Nano SOM supports GPIOs on SODIMM PCB Edge connector in i.MX 8M Mini or i.MX 8M Nano SODIMM Development platform's default configuration. Most of the i.MX 8M Mini or i.MX 8M Nano SoC Pins which are connected to SODIMM Edge connector can be configured as GPIO with interrupt capable (if not used as other interface) The i.MX 8M Mini or i.MX 8M Nano SoC's GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

For more details on GPIO Interface pinouts on SODIMM PCB edge connector, refer the below table.

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
71	GPIO1_6	GPIO1_IO06/AG11	IO, 3.3V CMOS	General Purpose Input/Output 0.
92	SAI5_RX_SYNC(SAI5_RXFS)	SAI5_RXFS/AB15	IO, 3.3V CMOS	General Purpose Input/Output 1.
91	SAI5_RX_BCLK(SAI5_RXC)	SAI5_RXC/AC15	IO, 3.3V CMOS	General Purpose Input/Output 2.
74	SAI1_RXC (NC in Nano)	SAI1_RXC/AF16	IO, 3.3V CMOS	General Purpose Input/Output 3.
157	SAI1_TXC (NC in Nano)	SAI1_TXC/AC18	IO, 3.3V CMOS	General Purpose Input/Output 4.
73	GPIO1_7[1]	GPIO1_IO07/AF11	IO, 3.3V CMOS	General Purpose Input/Output 5.
104	SAI1_RXFS (NC in Nano) [1]	SAI1_RXFS/AG16	IO, 3.3V CMOS	General Purpose Input/Output 6.
143	SAI1_TXFS (NC in Nano) [1]	SAI1_TXFS/AB19	IO, 3.3V CMOS	General Purpose Input/Output 7.
145	SAI1_MCLK (NC in Nano) [1]	SAI1_MCLK/ AB18	IO, 3.3V CMOS	General Purpose Input/Output 8.

[1]*Note: These signals are default configured as input GPIOs (General Purpose Input/Output).*

2.8.13 SPDIF Interface

The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF is composed of two parts: SPDIF Receiver and SPDIF Transmitter. As the SPDIF internal data width is 24-bit.

For more details on SPDIF pinouts on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
176	SPDIF_ETX_CLK	SPDIF_EXT_CLK/AF8	O, 3.3V CMOS	Sony/Philips Digital Interface Clock.
178	SPDIF_TX	SPDIF_TX/AF9	O, 3.3V CMOS	Sony/Philips Digital Interface Transmit.
177	SPDIF_RX	SPDIF_RX/AG9	I, 3.3V CMOS	Sony/Philips Digital Interface Receive.

Note: iWave has not tested SPDIF interface in the present BSP, if needed will support in future BSP versions. In the present BSP the above SPDIF signals are configured as input GPIOs (General Purpose Input/Output).

2.8.14 Boot Setting

i.MX 8M Mini or i.MX 8M Nano SoC boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. i.MX 8M Mini SoC Boot ROM code uses the state of the internal register BOOT_MODE [1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device. i.MX 8M Mini SODIMM SOM boot media is fixed as eMMC flash by On-SOM GPIO setting in hardware. In i.MX 8M Nano SODIMM SOM boot media can be changed using BOOT_MODE [1:0]

Note: Contact iWave if different boot media support is required other than eMMC flash for i.MX 8M Mini SOM

i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports two boot mode signals on SODIMM Edge Connector. BOOT_MODE is initialized by sampling the BOOT_MODE0 and BOOT_MODE1 inputs on the rising edge of POR_B. These Boot mode selection signals are connected to SODIMM Edge connector and desired boot mode must be set from the carrier board as explained in the below table.

Table 4: i.MX 8M Mini Boot Mode Pin Settings Truth Table

BOOT_MODE [1] (SODIMM Edge Pin 184)	BOOT_MODE [0] (SODIMM Edge Pin 182)	Boot Type	Description
1	0	Internal Boot Mode	In this mode, i.MX 8M Mini boots from the boot media selected by Boot media GPIO pin's settings. By default, eMMC is selected as boot media in i.MX 8M Mini SODIMM SOM hardware.
0	0	Boot From eFuses	In this mode, i.MX 8M Mini boots from the boot media selected by i.MX 8M Mini eFUSE settings.

			Note: i.MX 8M Mini eFuse setting is not modified by iWave from silicon shipped value.
0	1	Serial Downloader Mode	In this mode, i.MX 8M Mini boot media can be Programmed through its USB OTG interface using UUU tool supported by NXP.

Table 5: i.MX 8M Nano Boot Mode Pin Settings Truth Table

BOOT_MODE [1] (SODIMM Edge Pin 184)	BOOT_MODE [0] (SODIMM Edge Pin 182)	Boot Type	Description
0	0	Boot from internal fuses	In this mode, i.MX 8M Nano boots from internal efuses *Note: i.MX 8M Nano eFuse setting is not modified by iWave from silicon shipped value.*
0	1	Serial Downloader Mode	In this mode, i.MX 8M Nano boot media can be Programmed through its USB OTG interface using UUU tool supported by NXP.
1	0	eMMC Boot	In this mode, i.MX 8M Nano boots from eMMC.
1	1	SD Boot (USDHC2)	In this mode, i.MX 8M Nano boots from SD Card (USDHC2)

For more details on i.MX 8M Mini or i.MX 8M Nano SoC's BOOTMODE pins on SODIMM PCB Edge connector, refer below table:

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
182	BOOT_MODE0	BOOT_MODE0/ G26	I, 3.3V CMOS/ 10K PU	Boot Mode Select bit0. *Important Note: This pin is directly connected to i.MX 8M Mini or i.MX 8M Nano SoC's BOOT_MODE0 pin with On-SOM pullup and so don't add any external pullup in carrier board on this pin.* *Make sure to use this pin in carrier board to select desired boot mode by driving only low if required.*
184	BOOT_MODE1	BOOT_MODE1/ G27	I, 3.3V CMOS/ 10K PU	Boot Mode Select bit1. *Important Note: This pin is directly connected to i.MX 8M Mini or i.MX 8M Nano SoC's BOOT_MODE1 pin with On-*

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
				SOM pullup and so don't add any external pullup in carrier board on this pin. *Make sure to use this pin in carrier board to select desired boot mode by driving only low if required.*

2.8.15 Management Pins

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports Management pins for Reset button input and Power button input.

i.MX 8M Mini or i.MX 8M Nano SODIMM SOM supports reset button input(n_RST_OUT) on SODIMM Edge connector. Reset button input from SODIMM Edge connector is the active low signal which is connected to BD71847AMWV PMIC's PWRON_B pin in i.MX 8M Mini or i.MX 8M Nano SODIMM SOM. Once PWRON_B becomes low PMIC will reset the i.MX 8M Mini or i.MX 8M Nano SoC by making POR_B input signal to the SoC low.

i.MX 8M Mini or i.MX 8M Nano SODIMM SOM also supports Power button input (POWER_BTN#) on SODIMM PCB Edge connector which is the active low signal and connected to i.MX 8M Mini or i.MX 8M Nano SoC's ONOFF pin. This pin can be used to On/Off the i.MX 8M Mini or i.MX 8M Nano SoC by connecting push button in the carrier board. When the board power is On, a button press between 750ms to 5s will send an interrupt to core to request software to bring down the i.MX 8M Mini or i.MX 8M Nano safely (if software supports). Otherwise, button press greater than 5s results in a direct hardware power down which is applicable when software is unable to power Off the device. When the i.MX 8M Mini or i.MX 8M Nano SoC power supply is Off, a button presses greater in duration than 750ms asserts an output signal to request power from a power IC to power up the i.MX 8M Mini or i.MX 8M Nano SoC.

For more details on supported Management Signals pinouts on SODIMM PCB Edge connector and corresponding pin description, refer the below table.

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
187	n_RST_OUT	NA	I,3.3V CMOS 100K PU	RESET Input to SOM. *Note: This will restart the power cycle of SOM.* Active low reset button input. *Important Note: This reset input is connected to BD71847AMWV PMIC's PWRON_B Pin with On-SOM pullup and so don't add any external pullup in carrier board on this pin.*
179	ON_OFF	NA	I, 3.3V CMOS 100K PU	Power ON/OFF Input to SOM.

2.8.16 Miscellaneous Signals

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM PCB Edge Connector includes the remaining signals from i.MX 8M Mini or i.MX 8M Nano SoC which includes Board Configuration GPIOs, PWM Signals. These signals are Optionally connected to SODIMM Edge Connector through resistor but default not populated. For more details on these signals' pinout on SOIDMM Edge Connector, refer the below table.

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
126	BCONFIG_0(GPIO1_9) *	GPIO1_IO09 / AF10	IO, 3.3V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
121	BCONFIG_1(GPIO5_1) *	SAI3_TXD/ AF6	IO, 3.3V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
138	PWM1_OUT(I2C4_SDA)	I2C4_SDA/ E13	O, 3.3V CMOS	PWM1 Output.
125	PWM2_OUT(I2C4_SCL)	I2C4_SCL/ D13	O, 3.3V CMOS	PWM2 Output. *Note: I2C4_SCL is optionally connected for PCIe1_CLKREQ_B to enable SoC internal PCIe Reference clock through a resistor, but default not populated.*
47	SAI1_RXD0 (NC in Nano) [1]	SAI1_RXD0/ AG15	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 0 *Note: Termination will differ based on Boot configuration setting.*

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
158	SAI1_RXD1 (NC in Nano) [1]	SAI1_RXD1/ AF15	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 1 *Note: Termination will differ based on Boot configuration setting.*
68	SAI1_RXD2 (NC in Nano) [1]	SAI1_RXD2/ AG17	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 2 *Note: Termination will differ based on Boot configuration setting.*
148	SAI1_RXD3 (NC in Nano) [1]	SAI1_RXD3/ AF17	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 3 *Note: Termination will differ based on Boot configuration setting.*
149	SAI1_RXD4 (NC in Nano) [1]	SAI1_RXD4/ AG18	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 4 *Note: Termination will differ based on Boot configuration setting.*
123	SAI1_RXD5 (NC in Nano) [1]	SAI1_RXD5/ AF18	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 5 *Note: Termination will differ based on Boot configuration setting.*
175	SAI1_RXD6 (NC in Nano) [1]	SAI1_RXD6/ AG19	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 6 *Note: Termination will differ based on Boot configuration setting.*
144	SAI1_RXD7 (NC in Nano) [1]	SAI1_RXD7/ AF19	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 7 *Note: Termination will differ based on Boot configuration setting.*
156	SAI1_TXD0 (NC in Nano) [1]	SAI1_TXD0/ AG20	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Receive Data Lane 0 *Note: Termination will differ based on Boot configuration setting.*
166	SAI1_TXD1 (NC in Nano) [1]	SAI1_TXD1/ AF20	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Transmit Data Lane 1 *Note: Termination will differ based on Boot configuration setting.*
167	SAI1_TXD2 (NC in Nano) [1]	SAI1_TXD2/ AG21	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Transmit Data Lane 2 *Note: Termination will differ based on Boot configuration setting.*
173	SAI1_TXD3 (NC in Nano) [1]	SAI1_TXD3/ AF21	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Transmit Data Lane 3 *Note: Termination will differ based on Boot configuration setting.*
163	SAI1_TXD4 (NC in Nano) [1]	SAI1_TXD4/ AG22	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Transmit Data Lane 4 *Note: Termination will differ based on Boot configuration setting.*
165	SAI1_TXD5 (NC in Nano) [1]	SAI1_TXD5/ AF22	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Transmit Data Lane 5 *Note: Termination will differ based on Boot configuration setting.*
171	SAI1_TXD6 (NC in Nano) [1]	SAI1_TXD6/ AG23	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Transmit Data Lane 6

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
				Note: Termination will differ based on Boot configuration setting.
154	SAI1_TXD7 (NC in Nano) [1]	SAI1_TXD7/ AF23	IO, 3.3V CMOS/ 100K PD/4.7K PU	SAI1 Transmit Data Lane 7 *Note: Termination will differ based on Boot configuration setting.*

** Optional Feature*

[1]Important Note: The SAI1 signals which is having Boot configuration functionality in Funtion6 -BOOT_CFG[0:15] are also used for i.MX 8M Mini SoC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot media configurations.

2.8.17 Power and GND

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM works with single 3.3V power input (VCC) from SODIMM Edge connector and generates all other required powers internally On-SOM itself. i.MX 8M Mini or i.MX 8M Nano SODIMM coin cell power input (VDD_RTC) from SODIMM PCB Edge Connector to On-SOM RTC controller for real time clock.

SODIMM Pin No.	SODIMM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
20, 32, 46, 60, 72, 88, 106, 124, 142, 160, 180 & 192	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
1, 5, 13, 27, 40, 41, 51, 65, 79, 95, 113, 131, 151, 169, 185, 186, 198	GND	NA	Power	Ground.
183	VRTC_3V0	NA	I, 3V Power	3V coin cell input for RTC.

2.9 i.MX 8M Mini or i.MX 8M Nano Pin Multiplexing on SODIMM Edge

The i.MX 8M Mini or i.MX 8M Nano SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M Mini or i.MX 8M Nano SoC's IO pins can be configured as GPIO if required. The below tables provides the details of i.MX 8M Mini or i.MX 8M Nano SoC pin connections to the SODIMM edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M Mini or i.MX 8M Nano Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SODIMM SOM Edge connector for iWave's BSP reusability.

Table 6: i.MX 8M Mini SoC IOMUX for SODIMM Edge Connector interfaces

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Mini SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
MIPI CSI	150	A16	MIPI_CSI_CLK_N							MIPI_CSI_CLK_N
	152	B16	MIPI_CSI_CLK_P							MIPI_CSI_CLK_P
	168	A14	MIPI_CSI_D0_N							MIPI_CSI_D0_N
	170	B14	MIPI_CSI_D0_P							MIPI_CSI_D0_P
	159	A15	MIPI_CSI_D1_N							MIPI_CSI_D1_N
	161	B15	MIPI_CSI_D1_P							MIPI_CSI_D1_P
	162	A17	MIPI_CSI_D2_N							MIPI_CSI_D2_N
	164	B17	MIPI_CSI_D2_P							MIPI_CSI_D2_P
	172	A18	MIPI_CSI_D3_N							MIPI_CSI_D3_N
	174	B18	MIPI_CSI_D3_P							MIPI_CSI_D3_P
	153	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]		GPIO5_IO[18]
	155	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]		GPIO5_IO[19]
	147	AF12	GPIO1_IO[5]	M4_NMI				CCM_PMIC_READY		GPIO1_IO[5]
MIPI DSI	57	A11	MIPI_DSI_CLK_N							MIPI_DSI_CLK_N
	59	B11	MIPI_DSI_CLK_P							MIPI_DSI_CLK_P
	48	A9	MIPI_DSI_D0_N							MIPI_DSI_D0_N
	50	B9	MIPI_DSI_D0_P							MIPI_DSI_D0_P
	52	A10	MIPI_DSI_D1_N							MIPI_DSI_D1_N
	54	B10	MIPI_DSI_D1_P							MIPI_DSI_D1_P
	53	A12	MIPI_DSI_D2_N							MIPI_DSI_D2_N

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Mini SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	55	B12	MIPI_DSI_D2_P							MIPI_DSI_D2_P
	56	A13	MIPI_DSI_D3_N							MIPI_DSI_D3_N
	58	B13	MIPI_DSI_D3_P							MIPI_DSI_D3_P
	153	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]		GPIO5_IO[18]
	155	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]		GPIO5_IO[19]
	132	AD6	SAI3_MCLK	PWM4_OUT	SAI5_MCLK			GPIO5_IO[2]		GPIO5_IO[2]
	136	AF14	GPIO1_IO[1]	PWM1_OUT				XTALOSC_REF_CLK_24M	CCM_EXT_CLK2	GPIO1_IO[1]
	146	AG10	GPIO1_IO[8]	ENET1_1588_EVENT0_IN				USDHC2_RESET_B		GPIO1_IO[8]
Carrier SD Interface	105	AA26	USDHC2_CD_B					GPIO2_IO[12]		GPIO2_IO[12]
	109	W23	USDHC2_CLK					GPIO2_IO[13]		GPIO2_IO[13]
	108	W24	USDHC2_CMD					GPIO2_IO[14]		GPIO2_IO[14]
	107	AB23	USDHC2_DATA0					GPIO2_IO[15]		GPIO2_IO[15]
	111	AB24	USDHC2_DATA1					GPIO2_IO[16]		GPIO2_IO[16]
	112	V24	USDHC2_DATA2					GPIO2_IO[17]		GPIO2_IO[17]
	114	V23	USDHC2_DATA3					GPIO2_IO[18]	SRC_EARLY_RESET	GPIO2_IO[18]
PCIe	130	A19	PCIE_RXN_N							PCIE_RXN_N
	127	B19	PCIE_RXN_P							PCIE_RXN_P
	129	A20	PCIE_TXN_N							PCIE_TXN_N
	127	B20	PCIE_TXN_P							PCIE_TXN_P
	134	AD10	GPIO1_IO[10]	USB1_OTG_ID						GPIO1_IO[10]
	133	AC10	GPIO1_IO[11]	USB2_OTG_ID			USDHC3_VSELECT	CCM_PMIC_READY		GPIO1_IO[11]
ECSPI1	80	D6	ECSPI1_SCLK	UART3_RX				GPIO5_IO[6]		GPIO5_IO[6]
	96	B7	ECSPI1_MOSI	UART3_TX				GPIO5_IO[7]		GPIO5_IO[7]
	94	A7	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO[8]		GPIO5_IO[8]
	97	B6	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO[9]		GPIO5_IO[9]
ECSPI2	66	E6	ECSPI2_SCLK	UART4_RX				GPIO5_IO[10]		GPIO5_IO[10]
	70	B8	ECSPI2_MOSI	UART4_TX				GPIO5_IO[11]		GPIO5_IO[11]
	63	A8	ECSPI2_MISO	UART4_CTS_B				GPIO5_IO[12]		GPIO5_IO[12]
	62	A6	ECSPI2_SS0	UART4_RTS_B				GPIO5_IO[13]		GPIO5_IO[13]

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Mini SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
ECSPI3	189	E14	UART1_RX	ECSPI3_SCLK				GPIO5_IO[22]		GPIO5_IO[22]
	194	F13	UART1_TX	ECSPI3_MOSI				GPIO5_IO[23]		GPIO5_IO[23]
	196	F15	UART2_RX	ECSPI3_MISO				GPIO5_IO[24]		GPIO5_IO[24]
	181	E15	UART2_TX	ECSPI3_SS0				GPIO5_IO[25]		GPIO5_IO[25]
PWM	125	D13	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO[20]		GPIO5_IO[20]
	138	E13	I2C4_SDA	PWM1_OUT				GPIO5_IO[21]		GPIO5_IO[21]
I2C2	116	D10	I2C2_SCL	ENET1_1588_EVENT1_IN	USDHC3_CD_B			GPIO5_IO[16]		GPIO5_IO[16]
	115	D9	I2C2_SDA	ENET1_1588_EVENT1_OUT	USDHC3_WP			GPIO5_IO[17]		GPIO5_IO[17]
I2C3	153	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]		GPIO5_IO[18]
	155	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]		GPIO5_IO[19]
UART1 (Optional)	98	AC19	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA[1]	UART1_TX		GPIO4_IO[21]		GPIO4_IO[21]
	99	AB22	SAI2_RX_BCLK	SAI5_TX_BCLK		UART1_RX		GPIO4_IO[22]		GPIO4_IO[22]
	101	AC24	SAI2_RX_DATA[0]	SAI5_TX_DATA[0]		UART1_RTS_B		GPIO4_IO[23]		GPIO4_IO[23]
	100	AD23	SAI2_TX_SYNC	SAI5_TX_DATA[1]	SAI2_TX_DATA[1]	UART1_CTS_B		GPIO4_IO[24]		GPIO4_IO[24]
UART2	38	AG7	SAI3_RX_BCLK	GPT1_CLK	SAI5_RX_BCLK		UART2_CTS_B	GPIO4_IO[29]		GPIO4_IO[29]
	75	AF7	SAI3_RX_DATA[0]	GPT1_COMPARE1	SAI5_RX_DATA[0]		UART2_RTS_B	GPIO4_IO[30]		GPIO4_IO[30]
	103	AC6	SAI3_TX_SYNC	GPT1_CAPTURE2	SAI5_RX_DATA[1]	SAI3_TX_DATA[1]	UART2_RX	GPIO4_IO[31]		GPIO4_IO[31]
	102	AG6	SAI3_TX_BCLK	GPT1_COMPARE2	SAI5_RX_DATA[2]		UART2_TX	GPIO5_IO[0]		GPIO5_IO[0]
UART3	7	E18	UART3_RX	UART1_CTS_B	USDHC3_RESET_B			GPIO5_IO[26]		GPIO5_IO[26]
	9	D18	UART3_TX	UART1_RTS_B	USDHC3_VSELECT			GPIO5_IO[27]		GPIO5_IO[27]
UART4	117	F19	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B			GPIO5_IO[28]		GPIO5_IO[28]
	118	F18	UART4_TX	UART2_RTS_B				GPIO5_IO[29]		GPIO5_IO[29]
USB1 2.0 OTG	83	A22	USB1_DN							USB1_DN
	81	B22	USB1_DP							USB1_DP
	77	D22	USB1_ID							USB1_ID
	78	AB10	GPIO1_IO[12]	USB1_OTG_PWR				SDMA2_EXT_EVENT[1]		GPIO1_IO[12]
	76	AD9	GPIO1_IO[13]	USB1_OTG_OC				PWM2_OUT		GPIO1_IO[13]
	190	A23	USB2_DN							USB2_DN
	188	B23	USB2_DP							USB2_DP

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Mini SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
USB2 2.0 Host	140	AC9	GPIO1_IO[14]	USB2_OTG_PWR			USDHC3_CD_B	PWM3_OUT	CCM_CLKO1	GPIO1_IO[14]
	39	AB9	GPIO1_IO[15]	USB2_OTG_OC			USDHC3_WP	PWM4_OUT	CCM_CLKO2	GPIO1_IO[15]
SAI5 Audio	61	AD18	SAI5_RX_DATA[0]	SAI1_TX_DATA[2]				GPIO3_IO[21]		GPIO3_IO[21]
	89	AC14	SAI5_RX_DATA[1]	SAI1_TX_DATA[3]	SAI1_TX_SYNC	SAI5_TX_SYNC		GPIO3_IO[22]		GPIO3_IO[22]
	90	AD13	SAI5_RX_DATA[2]	SAI1_TX_DATA[4]	SAI1_TX_SYNC	SAI5_TX_BCLK		GPIO3_IO[23]		GPIO3_IO[23]
	67	AC13	SAI5_RX_DATA[3]	SAI1_TX_DATA[5]	SAI1_TX_SYNC	SAI5_TX_DATA[0]		GPIO3_IO[24]		GPIO3_IO[24]
	64	AD15	SAI5_MCLK	SAI1_TX_BCLK				GPIO3_IO[25]		GPIO3_IO[25]
JTAG	193	C27	CJTAG_TRST_B							CJTAG_TRST_B
	195	E27	CJTAG_TDI							CJTAG_TDI
	199	F27	CJTAG_TMS							CJTAG_TMS
	197	F26	CJTAG_TCK							CJTAG_TCK
	191	E26	CJTAG_TDO							CJTAG_TDO
GPIOs	71	AG11	GPIO1_IO[6]	ENET1_MDC				USDHC1_CD_B	CCM_EXT_CLK3	GPIO1_IO[6]
	73	AF11	GPIO1_IO[7]	ENET1_MDIO				USDHC1_WP	CCM_EXT_CLK4	GPIO1_IO[7]
	92	AB15	SAI5_RX_SYNC	SAI1_TX_DATA[0]				GPIO3_IO[19]		GPIO3_IO[19]
	91	AC15	SAI5_RX_BCLK	SAI1_TX_DATA[1]				GPIO3_IO[20]		GPIO3_IO[20]
	104	AG16	SAI1_RX_SYNC	SAI5_RX_SYNC				GPIO4_IO[0]		GPIO4_IO[0]
	74	AF16	SAI1_RX_BCLK	SAI5_RX_BCLK				GPIO4_IO[1]		GPIO4_IO[1]
	143	AB19	SAI1_TX_SYNC	SAI5_TX_SYNC				GPIO4_IO[10]		GPIO4_IO[10]
	157	AC18	SAI1_TX_BCLK	SAI5_TX_BCLK				GPIO4_IO[11]		GPIO4_IO[11]
	145	AB18	SAI1_MCLK	SAI5_MCLK	SAI1_TX_BCLK			GPIO4_IO[20]		GPIO4_IO[20]
	178	AF9	SPDIF1_OUT	PWM3_OUT				GPIO5_IO[3]		GPIO5_IO[3]
	177	AG9	SPDIF1_IN	PWM2_OUT				GPIO5_IO[4]		GPIO5_IO[4]
	176	AF8	SPDIF1_EXT_CLK	PWM1_OUT				GPIO5_IO[5]		GPIO5_IO[5]
SAI1 (Boot Config)	47	AG15	SAI1_RX_DATA[0]	SAI5_RX_DATA[0]	SAI1_TX_DATA[1]			GPIO4_IO[2]	BOOT_CFG[0]	GPIO4_IO[2]
	158	AF15	SAI1_RX_DATA[1]	SAI5_RX_DATA[1]				GPIO4_IO[3]	BOOT_CFG[1]	GPIO4_IO[3]
	68	AG17	SAI1_RX_DATA[2]	SAI5_RX_DATA[2]				GPIO4_IO[4]	BOOT_CFG[2]	GPIO4_IO[4]
	148	AF17	SAI1_RX_DATA[3]	SAI5_RX_DATA[3]				GPIO4_IO[5]	BOOT_CFG[3]	GPIO4_IO[5]
	149	AG18	SAI1_RX_DATA[4]	SAI6_TX_BCLK	SAI6_RX_BCLK			GPIO4_IO[6]	BOOT_CFG[4]	GPIO4_IO[6]
	123	AF18	SAI1_RX_DATA[5]	SAI6_TX_DATA[0]	SAI6_RX_DATA[0]	SAI1_RX_SYNC		GPIO4_IO[7]	BOOT_CFG[5]	GPIO4_IO[7]

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Mini SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	175	AG19	SAI1_RX_DATA[6]	SAI6_TX_SYNC	SAI6_RX_SYNC			GPIO4_IO[8]	BOOT_CFG[6]	GPIO4_IO[8]
	144	AF19	SAI1_RX_DATA[7]	SAI6_MCLK	SAI1_TX_SYNC	SAI1_TX_DATA[4]		GPIO4_IO[9]	BOOT_CFG[7]	GPIO4_IO[9]
	156	AG20	SAI1_TX_DATA[0]	SAI5_TX_DATA[0]				GPIO4_IO[12]	BOOT_CFG[8]	GPIO4_IO[12]
	166	AF20	SAI1_TX_DATA[1]	SAI5_TX_DATA[1]				GPIO4_IO[13]	BOOT_CFG[9]	GPIO4_IO[13]
	167	AG21	SAI1_TX_DATA[2]	SAI5_TX_DATA[2]				GPIO4_IO[14]	BOOT_CFG[10]	GPIO4_IO[14]
	173	AF21	SAI1_TX_DATA[3]	SAI5_TX_DATA[3]				GPIO4_IO[15]	BOOT_CFG[11]	GPIO4_IO[15]
	163	AG22	SAI1_TX_DATA[4]	SAI6_RX_BCLK	SAI6_TX_BCLK			GPIO4_IO[16]	BOOT_CFG[12]	GPIO4_IO[16]
	165	AF22	SAI1_TX_DATA[5]	SAI6_RX_DATA[0]	SAI6_TX_DATA[0]			GPIO4_IO[17]	BOOT_CFG[13]	GPIO4_IO[17]
	171	AG23	SAI1_TX_DATA[6]	SAI6_RX_SYNC	SAI6_TX_SYNC			GPIO4_IO[18]	BOOT_CFG[14]	GPIO4_IO[18]
	154	AF23	SAI1_TX_DATA[7]	SAI6_MCLK				GPIO4_IO[19]	BOOT_CFG[15]	GPIO4_IO[19]

Important Note: The SAI1 signals which is having Boot configuration functionality in Funtion6 -BOOT_CFG[0:15] are also used for i.MX 8M Mini SoC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot media configurations.

Table 7: i.MX 8M Nano SoC IOMUX for SODIMM Edge Connector interfaces

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Nano SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
MIPI CSI	150	A16	MIPI_CSI_CLK_N							MIPI_CSI_CLK_N
	152	B16	MIPI_CSI_CLK_P							MIPI_CSI_CLK_P
	168	A14	MIPI_CSI_D0_N							MIPI_CSI_D0_N
	170	B14	MIPI_CSI_D0_P							MIPI_CSI_D0_P
	159	A15	MIPI_CSI_D1_N							MIPI_CSI_D1_N
	161	B15	MIPI_CSI_D1_P							MIPI_CSI_D1_P
	162	A17	MIPI_CSI_D2_N							MIPI_CSI_D2_N
	164	B17	MIPI_CSI_D2_P							MIPI_CSI_D2_P
	172	A18	MIPI_CSI_D3_N							MIPI_CSI_D3_N
	174	B18	MIPI_CSI_D3_P							MIPI_CSI_D3_P
	153	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO[18]		GPIO5_IO[18]
	155	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO[19]		GPIO5_IO[19]

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Nano SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	147	AF12	GPIO1_IO[5]	M7_NMI				CCM_PMIC_READY		GPIO1_IO[5]
MIPI DSI	57	A11	MIPI_DSI_CLK_N							MIPI_DSI_CLK_N
	59	B11	MIPI_DSI_CLK_P							MIPI_DSI_CLK_P
	48	A9	MIPI_DSI_D0_N							MIPI_DSI_D0_N
	50	B9	MIPI_DSI_D0_P							MIPI_DSI_D0_P
	52	A10	MIPI_DSI_D1_N							MIPI_DSI_D1_N
	54	B10	MIPI_DSI_D1_P							MIPI_DSI_D1_P
	53	A12	MIPI_DSI_D2_N							MIPI_DSI_D2_N
	55	B12	MIPI_DSI_D2_P							MIPI_DSI_D2_P
	56	A13	MIPI_DSI_D3_N							MIPI_DSI_D3_N
	58	B13	MIPI_DSI_D3_P							MIPI_DSI_D3_P
	153	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO[18]		GPIO5_IO[18]
	155	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO[19]		GPIO5_IO[19]
	132	AD6	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		SPDIF1_OUT	GPIO5_IO[2]	SPDIF1_IN	GPIO5_IO[2]
	136	AF14	GPIO1_IO[1]	PWM1_OUT				REF_CLK_24M	CCM_EXT_CLK2	GPIO1_IO[1]
	146	AG10	GPIO1_IO[8]	ENET1_1588_EVENT0_IN	PWM1_OUT			USDHC2_RESET_B		GPIO1_IO[8]
Carrier SD Interface	105	AA26	USDHC2_CD_B					GPIO2_IO[12]		GPIO2_IO[12]
	109	W23	USDHC2_CLK	SAI5_RX_SYNC	ECSPI2_SCLK	UART4_RX	SAI5_MCLK	GPIO2_IO[13]		GPIO2_IO[13]
	108	W24	USDHC2_CMD	SAI5_RX_BCLK	ECSPI2_MOSI	UART4_TX	PDM_CLK	GPIO2_IO[14]		GPIO2_IO[14]
	107	AB23	USDHC2_DATA0	SAI5_RX_DATA0	I2C4_SDA	UART2_RX	PDM_BIT_STREAM0	GPIO2_IO[15]		GPIO2_IO[15]
	111	AB24	USDHC2_DATA1	SAI5_TX_SYNC	I2C4_SCL	UART2_TX	PDM_BIT_STREAM1	GPIO2_IO[16]		GPIO2_IO[16]
	112	V24	USDHC2_DATA2	SAI5_TX_BCLK	ECSPI2_SS0	SPDIF1_OUT	PDM_BIT_STREAM2	GPIO2_IO[17]		GPIO2_IO[17]
	114	V23	USDHC2_DATA3	SAI5_TX_DATA0	ECSPI2_MISO	SPDIF1_IN	PDM_BIT_STREAM3	GPIO2_IO[18]		GPIO2_IO[18]
ECSPI1	80	D6	ECSPI1_SCLK	UART3_RX	I2C1_SCL	SAI5_RX_SYNC		GPIO5_IO[6]		GPIO5_IO[6]
	96	B7	ECSPI1_MOSI	UART3_TX	I2C1_SDA	SAI5_RX_BCLK		GPIO5_IO[7]		GPIO5_IO[7]
	94	A7	ECSPI1_MISO	UART3_CTS_B	I2C2_SCL	SAI5_RX_DATA0		GPIO5_IO[8]		GPIO5_IO[8]

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Nano SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	97	B6	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI5_RX_DATA1	SAI5_TX_SYNC	GPIO5_IO[9]		GPIO5_IO[9]
ECSPI2	66	E6	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI5_RX_DATA2	SAI5_TX_BCLK	GPIO5_IO[10]		GPIO5_IO[10]
	70	B8	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI5_RX_DATA3	SAI5_TX_DATA0	GPIO5_IO[11]		GPIO5_IO[11]
	63	A8	ECSPI2_MISO	UART4_CTS_B	I2C4_SCL	SAI5_MCLK		GPIO5_IO[12]		GPIO5_IO[12]
	62	A6	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA			GPIO5_IO[13]		GPIO5_IO[13]
ECSPI3	189	E14	UART1_RX	ECSPI3_SCLK				GPIO5_IO[22]		GPIO5_IO[22]
	194	F13	UART1_TX	ECSPI3_MOSI				GPIO5_IO[23]		GPIO5_IO[23]
	196	F15	UART2_RX	ECSPI3_MISO		GPT1_COMPARE3		GPIO5_IO[24]		GPIO5_IO[24]
	181	E15	UART2_TX	ECSPI3_SS0		GPT1_COMPARE2		GPIO5_IO[25]		GPIO5_IO[25]
PWM	125	D13	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B	ECSPI2_MISO		GPIO5_IO[20]		GPIO5_IO[20]
	138	E13	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO[21]		GPIO5_IO[21]
I2C2	116	D10	I2C2_SCL	ENET1_1588_EVENT1_IN	USDHC3_CD_B	ECSPI1_MISO		GPIO5_IO[16]		GPIO5_IO[16]
	115	D9	I2C2_SDA	ENET1_1588_EVENT1_OUT	USDHC3_WP	ECSPI1_SS0		GPIO5_IO[17]		GPIO5_IO[17]
I2C3	153	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO[18]		GPIO5_IO[18]
	155	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO[19]		GPIO5_IO[19]
UART1 (Optional)	98	AC19	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA[1]	SAI2_RX_DATA1	UART1_TX	GPIO4_IO[21]	PDM_BIT_STREAM2	GPIO4_IO[21]
	99	AB22	SAI2_RX_BCLK	SAI5_TX_BCLK			UART1_RX	GPIO4_IO[22]	PDM_BIT_STREAM1	GPIO4_IO[22]
	101	AC24	SAI2_RX_DATA[0]	SAI5_TX_DATA[0]		SAI2_TX_DATA1	UART1_RTS_B	GPIO4_IO[23]	PDM_BIT_STREAM3	GPIO4_IO[23]
	100	AD23	SAI2_TX_SYNC	SAI5_TX_DATA[1]	SAI2_TX_DATA[1]	SAI2_TX_DATA1	UART1_CTS_B	GPIO4_IO[24]	PDM_BIT_STREAM2	GPIO4_IO[24]
UART2	38	AG7	SAI3_RX_BCLK	GPT1_CLK	SAI5_RX_BCLK	SAI2_RX_DATA1	UART2_CTS_B	GPIO4_IO[29]	PDM_CLK	GPIO4_IO[29]
	75	AF7	SAI3_RX_DATA[0]	GPT1_COMPARE1	SAI5_RX_DATA[0]	SAI3_TX_DATA1	UART2_RTS_B	GPIO4_IO[30]	PDM_BIT_STREAM1	GPIO4_IO[30]
	103	AC6	SAI3_TX_SYNC	GPT1_CAPTURE2	SAI5_RX_DATA[1]	SAI3_TX_DATA[1]	UART2_RX	GPIO4_IO[31]	PDM_BIT_STREAM3	GPIO4_IO[31]

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Nano SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	102	AG6	SAI3_TX_BCLK	GPT1_COMPARE2	SAI5_RX_DATA[2]	SAI2_TX_DATA1	UART2_TX	GPIO5_IO[0]	PDM_BIT_STREAM2	GPIO5_IO[0]
UART3	7	E18	UART3_RX	UART1_CTS_B	USDHC3_RESET_B	GPT1_CAPTURE2		GPIO5_IO[26]		GPIO5_IO[26]
	9	D18	UART3_TX	UART1_RTS_B	USDHC3_VSELECT	GPT1_CLK		GPIO5_IO[27]		GPIO5_IO[27]
UART4	117	F19	UART4_RX	UART2_CTS_B		GPT1_COMPARE1		GPIO5_IO[28]		GPIO5_IO[28]
	118	F18	UART4_TX	UART2_RTS_B		GPT1_CAPTURE1		GPIO5_IO[29]		GPIO5_IO[29]
USB1 2.0 OTG	83	A22	USB1_DN							USB1_DN
	81	B22	USB1_DP							USB1_DP
	77	D22	USB1_ID							USB1_ID
	78	AB10	GPIO1_IO[12]	USB1_OTG_PWR				SDMA2_EXT_EVENT[1]		GPIO1_IO[12]
	76	AD9	GPIO1_IO[13]	USB1_OTG_OC				PWM2_OUT		GPIO1_IO[13]
SAI5 Audio	61	AD18	SAI5_RX_DATA[0]				PDM_BIT_STREAM0	GPIO3_IO[21]		GPIO3_IO[21]
	89	AC14	SAI5_RX_DATA[1]			SAI5_TX_SYNC	PDM_BIT_STREAM1	GPIO3_IO[22]		GPIO3_IO[22]
	90	AD13	SAI5_RX_DATA[2]			SAI5_TX_BCLK	PDM_BIT_STREAM2	GPIO3_IO[23]		GPIO3_IO[23]
	67	AC13	SAI5_RX_DATA[3]			SAI5_TX_DATA[0]	PDM_BIT_STREAM3	GPIO3_IO[24]		GPIO3_IO[24]
	64	AD15	SAI5_MCLK					GPIO3_IO[25]		GPIO3_IO[25]
JTAG	193	C27	CJTAG_TRST_B							CJTAG_TRST_B
	195	E27	CJTAG_TDI							CJTAG_TDI
	199	F27	CJTAG_TMS							CJTAG_TMS
	197	F26	CJTAG_TCK							CJTAG_TCK
	191	E26	CJTAG_TDO							CJTAG_TDO
GPIOs	71	AG11	GPIO1_IO[6]	ENET1_MDC				USDHC1_CD_B	CCM_EXT_CLK3	GPIO1_IO[6]
	73	AF11	GPIO1_IO[7]	ENET1_MDIO				USDHC1_WP	CCM_EXT_CLK4	GPIO1_IO[7]
	92	AB15	SAI5_RX_SYNC					GPIO3_IO[19]		GPIO3_IO[19]
	91	AC15	SAI5_RX_BCLK				PDM_CLK	GPIO3_IO[20]		GPIO3_IO[20]
	178	AF9	SPDIF1_OUT	PWM3_OUT				GPIO5_IO[3]		GPIO5_IO[3]

Interface/ Function	SODIMM Edge Pin Number	i.MX 8M Nano SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	177	AG9	SPDIF1_IN	PWM2_OUT				GPIO5_IO[4]		GPIO5_IO[4]
	176	AF8	SPDIF1_EXT_CLK	PWM1_OUT				GPIO5_IO[5]		GPIO5_IO[5]
	140	AC9	GPIO1_IO[14]				USDHC3_CD_B	PWM3_OUT	CCM_CLKO1	GPIO1_IO[14]
	39	AB9	GPIO1_IO[15]				USDHC3_WP	PWM4_OUT	CCM_CLKO2	GPIO1_IO[15]
	134	AD10	GPIO1_IO[10]	USB1_OTG_ID	PWM3_OUT					GPIO1_IO[10]
	133	AC10	GPIO1_IO[11]	PWM2_OUT			USDHC3_VSELECT	CCM_PMIC_READY		GPIO1_IO[11]

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the ten VIN_3V3 pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VIN_3V3 that 3.15v to 3.45V range. 12 pins are allocated to VIN_3V3. The connector pin current rating is 0.5A per pin. This works out to 6A total for the 12 pins.

Table 8: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VIN_3V3[1]	3.15	3.3V	3.45V	±50mV
2	VCC_RTC[2]	2.8V	3V	3.3V	±20 mV

[1] *i.MX 8M Mini* or i.MX 8M *Nano SODIMM SOM is designed to work with VIN_3V3 input power rail from SODIMM Edge connector.*

[2] *i.MX 8M Mini* or i.MX 8M *Nano SODIMM SOM uses this voltage as backup power source to RTC controller when VCC is off. This power is an optional power and can be left open if RTC functionality is not required.*

3.1.1 Power Input Sequencing

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM's Power Input sequence requirement is explained below.

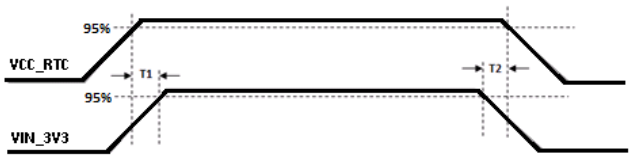

Figure 7: Power Input Sequencing

Table 9: Power Sequence Timing

Item	Description	Value
T1	VCC_RTC rise time to VIN_3V3 rise time	≥ 0 ms
T2	VIN_3V3 fall time to VRTC_3V0 fall time	≥ 0 ms

Important Note: All carrier board power supplies should be powered ON only after the SOM is powered ON completely. Also make sure that all Carrier board interface peripherals' power supply must be OFF if SOM is powered OFF, otherwise it can cause internal latch-up and malfunctions/bootup issues due to reverse current flows. NXP recommends customers to remove power (Voltage source) to all components on the board in the event of a processor reset.

3.2 Power Consumption

Table 10: i.MX 8M Mini SODIMM SOM Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Audio	VIN_3V3	0.454A/1.4982W
Play Video run in MIPI display (Gstreamer)	VIN_3V3	0.581A/1.9173W
Play Video run in MIPI display (Gplay)	VIN_3V3	0.625A/2.0625W
Camera Streaming	VIN_3V3	0.589A/1.9437W
Ping Bluetooth	VIN_3V3	0.532A/1.7556W
Ping Wi-Fi	VIN_3V3	0.562A/1.8546W
Ping Ethernet (1000 Mbps)	VIN_3V3	0.654A/2.1582W
Ping Ethernet (100 Mbps)	VIN_3V3	0.592A/1.9536W
Ping Ethernet (10 Mbps)	VIN_3V3	0.56A/1.848W
Ethernet Streaming (Video Play)	VIN_3V3	0.646A/2.1318W
eMMC to Carrier micro SD file transfer	VIN_3V3	0.616A/2.0328W
eMMC to USB2.0 file transfer	VIN_3V3	0.632A/2.0856W
eMMC to Mini PCIe file transfer	VIN_3V3	0.647A/2.1351W
Wi-fi file transfer	VIN_3V3	0.746A/2.4618W
Bluetooth file transfer	VIN_3V3	0.493A/1.6269W
GPU Processor -Graphics 3D Test	VIN_3V3	0.653A/2.1549W
Transfer the 1MB file between USB2.0, mini PCIe and Carrier SD with 1000 count	VIN_3V3	0.685A/2.2605W
Dhrystone	VIN_3V3	0.567A/1.8711W
Typical Maximum Power: Run the below during Maximum Power Test, • Run the video on MIPI display using Gplay • Run the Camera Streaming • Ethernet - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background • Run the Graphics (GPU) application on MIPI display	VIN_3V3	1.23A/4.059W
Low Power Mode Power Consumption		
System Idle Mode	VIN_3V3	0.356A/1.1748W
Deep Sleep Mode	VIN_3V3	0.097A/0.3201W
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	0.4µA/1.2µW

[1] Power consumption measurements have been done in iWave 's i.MX 8M Mini SoC (Quad 1GB) based SODIMM Development platform with iWave 's iW-RainboW-G34M_G37M-i.MX_8M_Mini_Nano_SODIMM_SOM-Linux5.10.72 BSP.

Table 11: i.MX 8M Nano SODIMM SOM Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Audio	VIN_3V3	0.307A/1.0131W
Play Video run in MIPI display (Gstreamer)	VIN_3V3	0.56A/1.848W
Play Video run in MIPI display (Gplay)	VIN_3V3	0.587A/1.9371W
Camera Streaming	VIN_3V3	0.498A/1.6434W
Ping Bluetooth	VIN_3V3	0.323A/1.0659W
Ping Wi-Fi	VIN_3V3	0.498A/1.6434W
Ping Ethernet (1000 Mbps)	VIN_3V3	0.476A/1.5708W
Ping Ethernet (100 Mbps)	VIN_3V3	0.377A/1.2441W
Ping Ethernet (10 Mbps)	VIN_3V3	0.35A/1.155W
Ethernet Streaming (Video Play)	VIN_3V3	0.689A/2.2737W
eMMC to Carrier micro SD file transfer	VIN_3V3	0.394A/1.3002W
Wi-fi file transfer	VIN_3V3	0.53A/1.749W
Bluetooth file transfer	VIN_3V3	0.313A/1.0329W
GPU Processor -Graphics 3D Test	VIN_3V3	0.62A/2.046W
Dhrystone	VIN_3V3	0.61A/2.013W
Typical Maximum Power: Run the below during Maximum Power Test, • Run the video on MIPI display using Gplay • Run the Camera Streaming • Ethernet - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background • Run the Graphics (GPU) application on MIPI display	VIN_3V3	0.98A/3.234W
Low Power Mode Power Consumption		
System Idle Mode	VIN_3V3	0.225A/0.7425W
Deep Sleep Mode	VIN_3V3	0.03A/0.099W
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	0.4µA/1.2µW

[1] Power consumption measurements have been done in iWave 's i.MX 8M Nano SoC (Quad 1GB) based SODIMM Development platform with iWave 's iW-RainboW-G34M_G37M-i.MX_8M_Mini_Nano_SODIMM_SOM-Linux5.10.72 BSP.

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3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Mini or i.MX 8M Nano SODIMM SOM.

Table 12: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2] The LBEE5HY1MW Wi-Fi & BT module supports operating temperature -30°C to 85°C with the default module's firmware. To set the module temperature to industrial grade in firmware, please contact iWave.

[3] If Micro SD connector has to be supported in i.MX 8M Mini or i.MX 8M *Nano SODIMM SOM, operating temperature range is -25°C to 85°C.*

[4] For more information on Thermal solution & Heat sink/ Heat Spreader refer the following section.

3.3.2 Heat Sink/ Heat Spreader

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique like Heat spreader, Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Note: iWave supports Heat Sink/ Heat Spreader Solution for i.MX 8M Mini or i.MX 8M *Nano SODIMM SOM SOM. For more information on Heat Sink/ Heat Spreader contact iWave support team. Do not Power On the SOM without a proper thermal solution.*

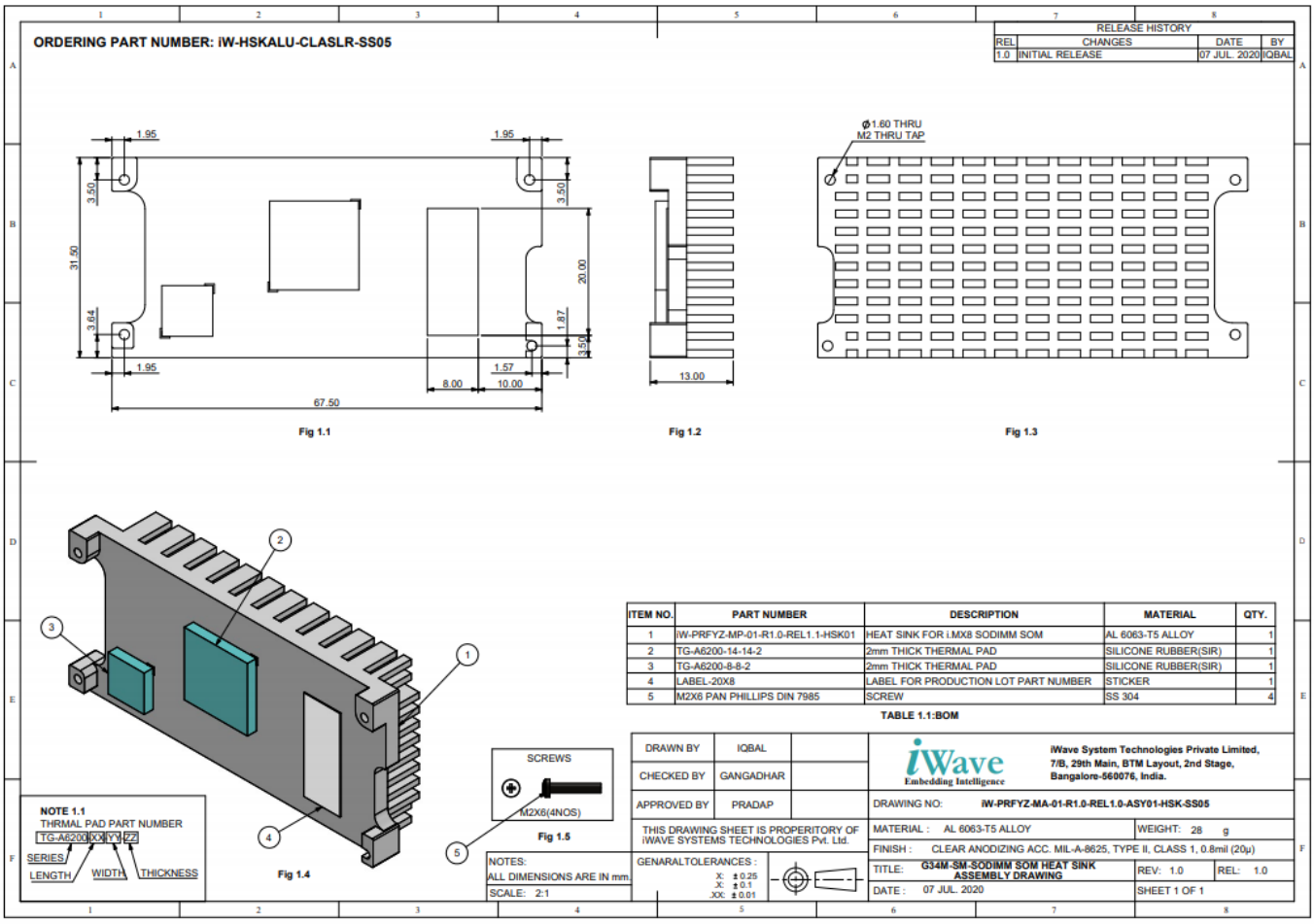

Figure 8: Mechanical dimension Heat Sink

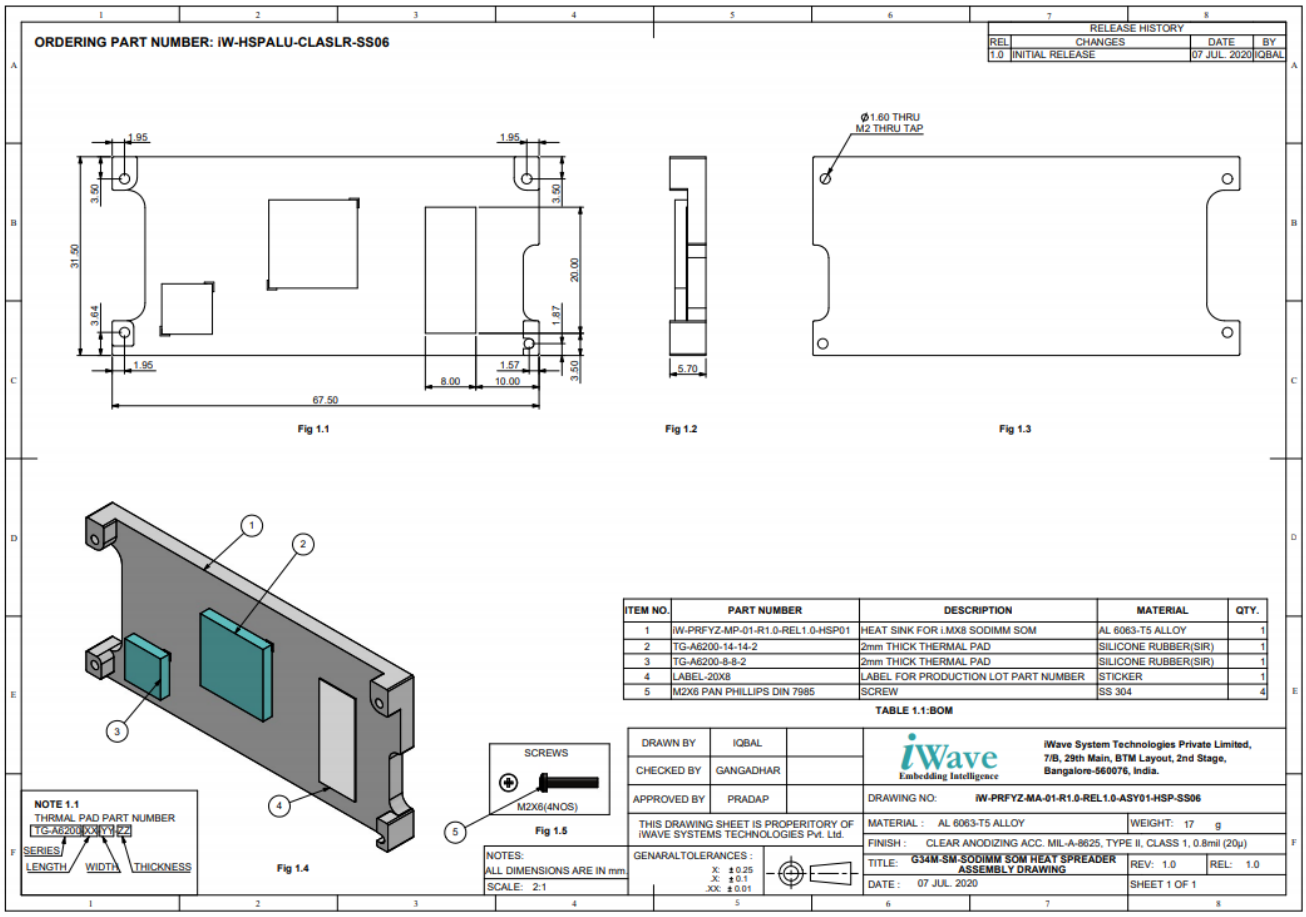

Figure 9: Mechanical dimension Heat Spreader

3.3.3 RoHS Compliance

iWave's i.MX 8M Mini or i.MX 8M Nano SODIMM SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.4 Electrostatic Discharge

iWave's i.MX 8M Mini or i.MX 8M Nano SODIMM SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Mechanical Dimensions

i.MX 8M Mini or i.MX 8M Nano SODIMM SOM PCB size is 67.6 mm x 37mm x 1mm. SODIMM SOM mechanical dimension is shown below. (All dimensions are shown in mm)

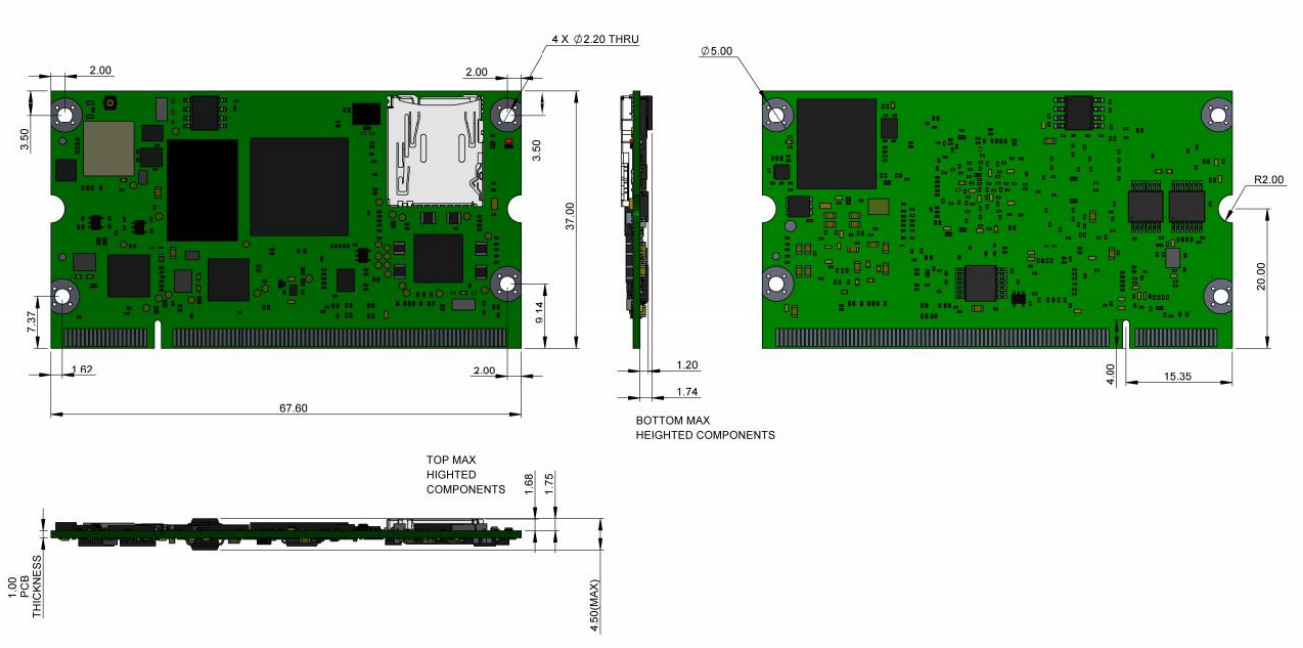

Figure 10: Mechanical dimension of i.MX 8M Mini or i.MX 8M Nano SODIMM SOM

The i.MX 8M Mini or i.MX 8M Nano SODIMM SOM PCB thickness is 1mm±0.1mm, top side maximum height component is 1.75mm (RTC Controller IC will be the maximum height on Top side followed by SD Connector(optional) (1.70mm) and bottom side maximum height component is QSPI (1.75mm) which is optional in default configuration hence U20 IC (1.20mm) will be the maximum height on bottom side in default configuration. Please refer the above figure which gives height details of the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8M Mini or i.MX 8M Nano SODIMM SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 13: i.MX 8M Mini SODIMM SOM Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G34M - i.MX 8M Mini SODIMM SOM (industrial grade) with Wi-Fi & 2xEthernet		
iW-G34M-SM04-4L001G-E008G-BIA	i.MX8M Mini Quad, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM4L-4L001G-E008G-BIA	i.MX8M Mini Quad Lite, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM02-4L001G-E008G-BIA	i.MX8M Mini Dual, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM2L-4L001G-E008G-BIA	i.MX8M Mini Dual Lite, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM01-4L001G-E008G-BIA	i.MX8M Mini Solo, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM1L-4L001G-E008G-BIA	i.MX8M Mini Solo Lite, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-Rainbow G34M - i.MX 8M Mini SODIMM SOM (industrial grade) without Wi-Fi & 2xEthernet		
iW-G34M-SM04-4L001G-E008G-BIB	i.MX8M Mini Quad, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code	-40°C to 85°C
iW-G34M-SM4L-4L001G-E008G-BIB	i.MX8M Mini Quad Lite, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code	-40°C to 85°C
iW-G34M-SM02-4L001G-E008G-BIB	i.MX8M Mini Dual, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code	-40°C to 85°C
iW-G34M-SM2L-4L001G-E008G-BIB	i.MX8M Mini Dual Lite, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code	-40°C to 85°C
iW-G34M-SM01-4L001G-E008G-BIB	i.MX8M Mini Solo, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code	-40°C to 85°C
iW-G34M-SM1L-4L001G-E008G-BIB	i.MX8M Mini Solo Lite, 1GB LPDDR4, 8GB eMMC, 2xETH with boot code	-40°C to 85°C
iW-Rainbow G34M - i.MX 8M Mini SODIMM SOM (industrial grade) with Wi-Fi & 1xEthernet		
iW-G34M-SM04-4L001G-E008G-BIC	i.MX8M Mini Quad, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM4L-4L001G-E008G-BIC	i.MX8M Mini Quad Lite, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM02-4L001G-E008G-BIC	i.MX8M Mini Dual, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code - With Wi-Fi, BT	-40°C to 85°C

Product Part Number	Description	Temperature
iW-G34M-SM2L-4L001G-E008G-BIC	i.MX8M Mini Dual Lite, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM01-4L001G-E008G-BIC	i.MX8M Mini Solo, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-SM1L-4L001G-E008G-BIC	i.MX8M Mini Solo Lite, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-Rainbow G34M - i.MX 8M Mini SODIMM SOM without Wi-Fi & 1xEthernet		
iW-G34M-SM04-4L001G-E008G-BID	i.MX8M Mini Quad, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code	-40°C to 85°C
iW-G34M-SM4L-4L001G-E008G-BID	i.MX8M Mini Quad Lite, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code	-40°C to 85°C
iW-G34M-SM02-4L001G-E008G-BID	i.MX8M Mini Dual, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code	-40°C to 85°C
iW-G34M-SM2L-4L001G-E008G-BID	i.MX8M Mini Dual Lite, 1GB LPDDR4, 8GB eMMC, 1xETH with boot code	-40°C to 85°C

Table 14:i.MX 8M Nano SODIMM SOM Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G37M - i.MX 8M Nano SODIMM SOM (industrial grade) with 1GB LPDDR4 and Wi-Fi		
iW-G37M-SM04-4L001G-E008G-BIA	i.MX8M Nano Quad, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM4L-4L001G-E008G-BIA	i.MX8M Nano Quad Lite, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM02-4L001G-E008G-BIA	i.MX8M Nano Dual, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM2L-4L001G-E008G-BIA	i.MX8M Nano Dual Lite, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM01-4L001G-E008G-BIA	i.MX8M Nano Solo, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM1L-4L001G-E008G-BIA	i.MX8M Nano Solo Lite, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-Rainbow G37M - i.MX 8M Nano SODIMM SOM (industrial grade) with 1GB LPDDR4 without Wi-Fi		
iW-G37M-SM04-4L001G-E008G-BIB	i.MX8M Nano Quad, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-SM4L-4L001G-E008G-BIB	i.MX8M Nano Quad Lite, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-SM02-4L001G-E008G-BIB	i.MX8M Nano Dual, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-SM2L-4L001G-E008G-BIB	i.MX8M Nano Dual Lite, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C

Product Part Number	Description	Temperature
iW-G37M-SM01-4L001G-E008G-BIB	i.MX8M Nano Solo, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-SM1L-4L001G-E008G-BIB	i.MX8M Nano Solo Lite, 1GB LPDDR4, 8GB eMMC with boot cod	-40°C to 85°C
iW-Rainbow G37M - i.MX 8M Nano SODIMM SOM (industrial grade) with 2GB LPDDR4 with Wi-Fi		
iW-G37M-SM04-4L002G-E008G-BIA	i.MX8M Nano Quad, 2GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM4L-4L002G-E008G-BIA	i.MX8M Nano Quad Lite, 2GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM02-4L002G-E008G-BIA	i.MX8M Nano Dual, 2GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM2L-4L002G-E008G-BIA	i.MX8M Nano Dual Lite, 2GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM01-4L002G-E008G-BIA	i.MX8M Nano Solo, 2GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-SM1L-4L002G-E008G-BIA	i.MX8M Nano Solo Lite, 2GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-Rainbow G37M - i.MX 8M Nano SODIMM SOM (industrial grade) with 2GB LPDDR4 without Wi-Fi		
iW-G37M-SM04-4L002G-E008G-BIB	i.MX8M Nano Quad, 2GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-SM4L-4L002G-E008G-BIB	i.MX8M Nano Quad Lite, 2GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-SM02-4L002G-E008G-BIB	i.MX8M Nano Dual, 2GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-SM2L-4L002G-E008G-BIB	i.MX8M Nano Dual Lite, 2GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C

Important Note: Some of the above-mentioned Part Numbers are subject to MOQ purchase. Please contact iWave for further details.

For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

5. APPENDIX I

5.1 Guidelines to insert the SOIDMM SOM into carrier board

- Make sure that power is not provided to the Carrier board.
- Insert the module into the Socket at a slight angle (approximately 30 degrees). Note that the socket and module are both keyed, which means the module can be installed one way only.
- To seat the module into the socket, apply firm, even pressure to each end of the module until you feel it slip down into the socket.
- With the module properly seated in the socket, rotate the module downward, as indicated in the illustration. Continue pressing downward until the clips at each end of the socket lock into position.
- Once the module has been installed, Carrier board can be Powered ON with 5V power supply.

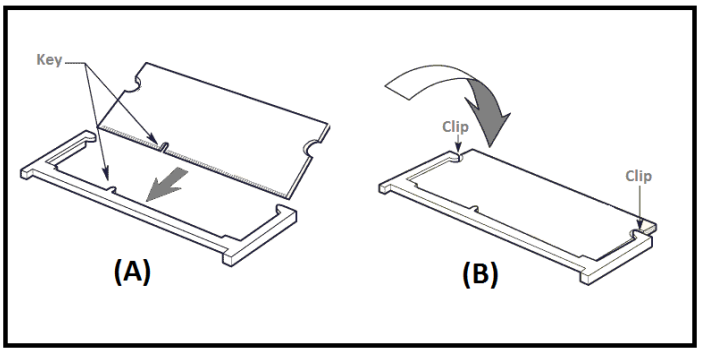

Figure 11: Module Insertion Procedure

5.2 Guidelines to remove the SOIDMM SOM from carrier board

- Make sure that power is not provided to the Carrier board.
- When you remove the module, pull away the retention clips (A) on each side of the memory module.
- The module pops up. Grasp the edge of the module (B) and gently pull the module out of the connector.

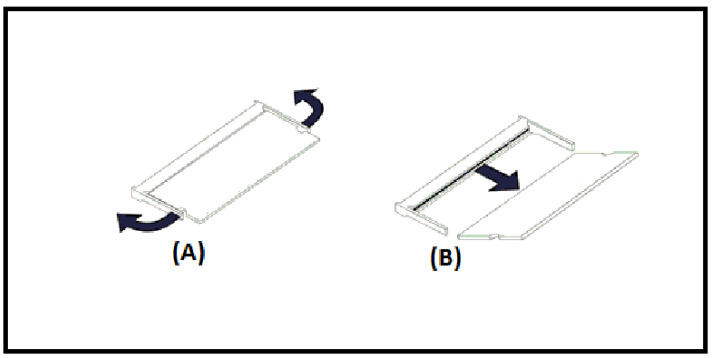

Figure 12: Module Removal Procedure

6. APPENDIX II

6.1 i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Development Platform

iWave Systems supports iW-RainboW-G34D-i.MX 8M Mini SODIMM SOM Development Platform and iW-RainboW-G37D-i.MX 8M Nano SODIMM SOM which is targeted for quick validation of i.MX 8M Mini or i.MX 8M Nano SoC based SODIMM SOM and its features. Being a Pico-ITX form factor with 100mm x 72mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete supported features.

iWave Systems supports also supports SODIMM MIPI Add-On-module for i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Development Platform to validate MIPI DSI and MIPI CSI interface. For more details on i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Development Platform, visit the below web link.

https://www.iwavesystems.com/product/i-mx-8m-mini-nano-sodimm-som/

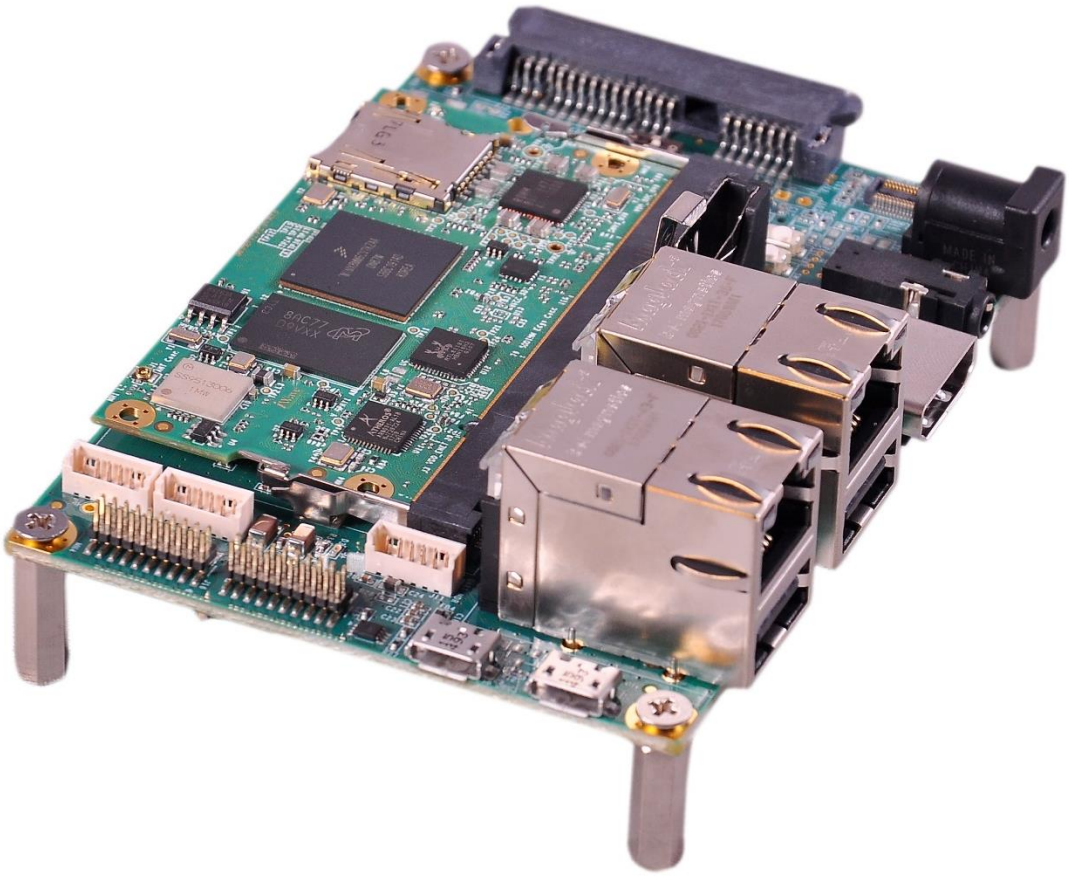

Figure 13: i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Development Platform


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