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Kintex Ultrascale+ FPGA SOM
Hardware User Guide

iWave
Embedding Intelligence

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Kintex Ultrascale+ FPGA System on Module based on the Xilinx Kintex Ultrascale+ FPGA (KU19P). This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Kintex Ultrascale+ FPGA System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The Kintex Ultrascale+ FPGA (KU19P) SOM is integrated with Xilinx KU19P FPGA SoC and NXP's LS1021A Layerscape Processor. Kintex Ultrascale+ FPGA SOM has a form factor of 110mm x 75mm and provides the functional requirements for an embedded application. Two high speed ruggedized terminal strip connectors and Two High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Kintex Ultrascale+ FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
RCW	Reset Configuration Word
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
PBL	Pre-boot Loader
GB	Giga Byte
Gbps	Gigabits per sec
IFC	Integrated Flash Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
MRAM	Magneto-resistive Random Access Memory
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
SRAM	Static Random Access Memory
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
TPM	Trusted Platform Module

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

1.5 References

- Kintex Ultrascale+ FPGA Technical Reference Manual
- Kintex Ultrascale+ FPGA Device Overview
- Kintex Ultrascale+ FPGAs Data Sheet: DC and AC Switching Characteristics
- QorIQ LS1021A Reference Manual
- QorIQ LS1021A Data Sheet

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Kintex Ultrascale+ FPGA (KU19P) SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Kintex Ultrascale+ FPGA (KU19P) SOM Block Diagram

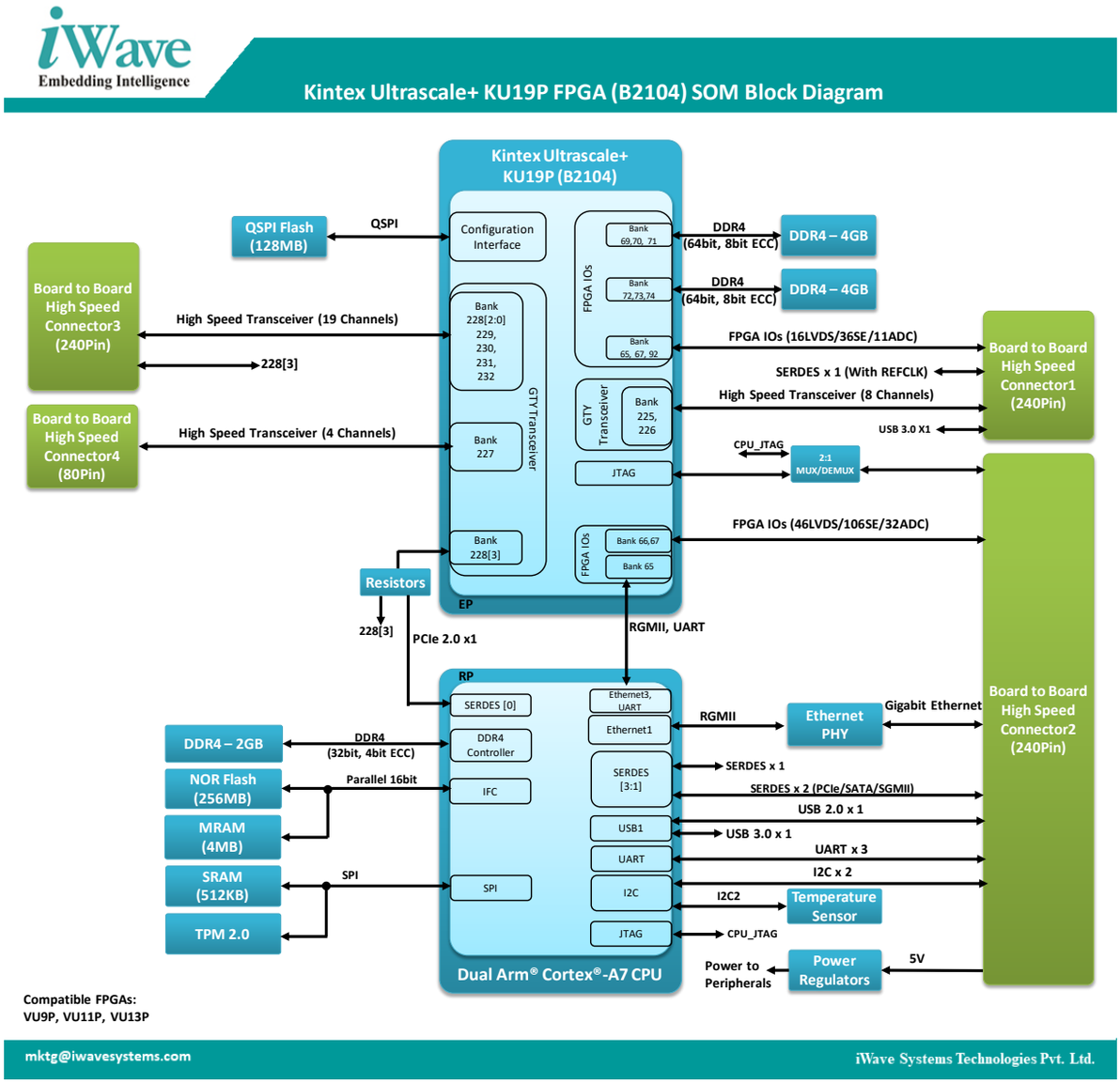


Figure 1: Kintex Ultrascale+ FPGA SOM Block Diagram

2.2 Kintex Ultrascale+ FPGA SOM Features

The Kintex Ultrascale+ FPGA (KU19P) SOM supports the following features.

FPGA

- Xilinx Kintex Ultrascale+ FPGA
  - Kintex Ultrascale+ FPGA (FBVB2104) Package
    System Logic cells up to 1.843K Logic cells and up to 1.685K Configurable Logic Blocks.
  - UltraRAM for on-chip memory integration
  - Integrated 100G Ethernet MAC with KR4 RS-FEC, PCIe® Gen4, and 150G Interlaken cores
  - 16G and 28G backplane-capable transceivers

PMIC

- Dialog's DA9062 PMIC (RTC is optional)

Memory

- 4GB DDR4 SDRAM1 (64bit) with 8-bit ECC (Expandable)
- 4GB DDR4 SDRAM2 (64bit) with 8-bit ECC (Expandable)
- 128MB QSPI Flash.

CPU

- QorIQ LS1021A Processor
  - Arm® Cortex®-A7 MPCore compliant with Armv7-A™ architecture. LS1021A contains a dual-core Cortex-A7 cores running up to 1.2 GHz
  - 32 KB instruction and data L1 cache with single bit error detection and correction, ECC protection on both instruction and data caches
- Up to 512 KB coherent L2 cache with single bit error detection and correction, ECC protection

PMIC

- Dialog's DA9062 PMIC (with RTC)

Memory

- 2GB DDR4 SDRAM (32bit) with 4-bit ECC (Expandable)
- 256MB NOR Flash (16bit)
- 4MB MRAM (16bit)
- 512KB SRAM

FPGA to CPU Interfaces

- PCIex1 Gen2
- RGMII
- UART
- Slide IDs
- Interrupt Request Pins

Other On-SOM Features

- TPM 2.0 Module
- Temperature Sensor
- Gigabit Ethernet PHY Transceiver
- Clock Synthesizer for On-SOM Clocks
- Fan Header (Optional)

Board to Board Connector1 Interfaces (240pin)

From LS1021a

- USB 3.0 x 1
- 1 SerDes lane for high-speed peripheral interface with reference clock
- 6 GPIOs From LS1021A

From KU19P

- GTY High Speed Transceivers (up to 32.75Gbps) x 8
- FPGA IOs - HD Bank 92
  - Up to 11 LVDS IOs/22 Single ended (SE) IOs
    - Up to 3 HDGC Global Clock Input pins (LVDS/SE)
    - Up to 11 ADC Input pins (Differential/Single Ended)
- FPGA IOs - HP Bank 65,67
  - Up to 5 LVDS IOs/14 Single ended (SE) IOs
    - Up to 4 HDGC Global Clock Input pins (LVDS/SE)

Board to Board Connector2 Interfaces (240pin)

From LS1021a

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY)
- USB2.0 x 1 Port
- Debug UART x 1 Port

- Data UART x 2 Port
- I2C x 2 Ports
- JTAG x1 Port
- Up to 2 SerDes lanes for high-speed peripheral interfaces (PCIe, SATA, SGMII)
- 10 GPIOs From LS1021A

From KU19P

- FPGA IOs - HP Bank 65,66
  - Up to 24 LVDS IOs/52 Single ended (SE) IOs
    - Up to 4 GC Global Clock Input pins (LVDS/SE)
    - Up to 16 ADC Input pins (Differential/Single Ended)
- FPGA IOs - HP Bank 67
  - Up to 22 LVDS IOs/44 Single ended (SE) IOs
    - Up to 4 GC Global Clock Input pins (LVDS/SE)
    - Up to 15 ADC Input pins (Differential/Single Ended)

Board to Board Connector3 Interfaces (240pin)

From KU19P

- GTY High Speed Transceivers (up to 32.75Gbps) x 20[1]

Board to Board Connector4 Interfaces (80pin)

From KU19P

- GTY High Speed Transceivers (up to 32.75Gbps) x 4

General Specification

- Power Supply : 5V (from Board-to-Board Connector2)
- Form Factor : 110mm x 75mm

[1] *In Board-to-Board Connector3, by default one GTY transceiver link is connected with on-SOM PCIe transceiver.*

2.3 Kintex Ultrascale+ FPGA

2.3.1 FPGA & Design Information

The Kintex Ultrascale+ FPGA SoC provides best performance with up to 40% lower power than previous generation Kintex series due to enhanced system logic cell packaging. This also includes the highest signal processing bandwidth in a mid-range device, next generation transceivers. The family is ideal for DSP intensive processing required for next generation and packet processing in 100G networking.

Note: Please refer the latest Kintex Ultrascale+ FPGA Datasheet & Technical Reference Manual for more details which may be revised from time to time.

		KU19P	VU7P	VU9P	VU11P	VU13P
Logic	System Logic Cells (K)	1,843	1,724	2,586	2,835	3,780
	CLB Flip-Flops (K)	1,685	1,576	2,364	2,592	3,456
	CLB LUTs (K)	842	788	1,182	1,296	1,728
Memory	Max. Distributed RAM (Mb)	11.6	24.1	36.1	36.2	48.3
	Total Block RAM (Mb)	60.8	50.6	75.9	70.9	94.5
	UltraRAM (Mb)	81	180	270	270	360
Clocking	Clock Mgmt Tiles (CMTs)	9	NA	NA	NA	NA
Integrated IP	DSP Slices	1,080	4,560	6,840	9,216	12,288
	PCIe® Gen3 x16	0	4	6	3	4
	PCIe® Gen3 x16 /Gen4 x8/CCIX	3	NA	NA	NA	NA
	100G Ethernet w/ KR4 RS-FEC	1	6	9	9	12
I/O	Max. Single-Ended HD I/Os	72	0	0	0	0
	Max. Single-Ended HP I/Os	468	832	832	624	832
	GTY 32.75Gb/s Transceivers	32	80	120	96	128

Figure 2: Kintex Ultrascale+ FPGA Devices Comparison

The Kintex Ultrascale+ FPGA's IO Banks are classified as high-performance (HP) banks or high-density (HD) banks. The HP Bank I/Os are optimized for highest performance operation organized in banks of 52pins. The HD Bank I/Os are reduced-feature I/Os organized in banks of 24pins.

In Kintex Ultrascale+ FPGA, each IO bank supports four global clock (GC or HDGC) input pin pairs. GC pins have direct access to the global clock buffers, PLLs of the same Bank. HDGC pins are from HD I/O banks and have direct access only to the global clock buffers. Also, Kintex Ultrascale+ FPGA supports high speed GTY transceivers.

2.3.1.1 FPGA Power

The Kintex Ultrascale+ FPGA SOM uses discrete power regulators along with DA9062 PMIC from Dialog Semiconductor for FPGA power management. In SOM, FPGA power domain supply voltage (VCC_INT, VCCINT_IO, VCCBRAM) is fixed to 0.85V or 0.9V based on the speed grade of the FPGA.

The Kintex Ultrascale+ FPGA SOM supports Dialog semiconductor DA9062 PMIC for other powers to FPGA. The I2C2 module of LS1021A is used for FPGA PMIC interface with I2C address 0x48. The I/O voltage of HD Bank (PL Bank 92) and HP Banks (Bank 65, 66 & 67) which are connected to Board-to-Board Connectors are generated from PMIC LDO1, LDO2, LDO3 and LDO4 respectively.

PMIC's LDO1 is connected to I/O voltage of HD Bank92 and by default set to 1.2V, LDO2 is connected to I/O voltage of HP Bank65 and by default set to 1.8V, LDO3 is connected to HP Bank66 and by default set to 1.0V, LDO4 is connected to I/O voltage of HP Bank67 and by default set to 1.0V. IO voltage is configurable through software after LS1021A boot-up.

PMIC supports reset output and connected to Kintex Ultrascale+ FPGA AL28 pin (IO_L24N_T3U_N11_DOUT_CSO_B_65) for power on reset. Also, PMIC supports IRQ output for events indication and connected to FPGA BC28 pin (IO_T1U_N12_SMBALERT_65).

Important Note: Every Power Off and On, The DA9062 PMIC work as initial OTP Setting

2.3.1.2 FPGA Reset

The Kintex Ultrascale+ FPGA SOM uses PMIC's Reset output (nRESET) for FPGA Power On Reset and connected to AL28 pin (IO_L24N_T3U_N11_DOUT_CSO_B_65) of FPGA.

2.3.1.3 FPGA Reference Clock

The Kintex Ultrascale+ FPGA SOM supports on board clock synthesizer for reference clock to different blocks of Kintex Ultrascale+ FPGA and LS1021A processor. The reference clock from Clock Synthesizer to FPGA is mentioned in the below table.

Sl. No	On-SOM Clock Synthesizer Frequency	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description	Stability
1	300MHz	IO_L13P_T2L_N0_GC_QBC_68	68	G14	1.8V, LVDS	LVDS reference clock for FPGA DDR4 SDRAM1. This is connected to FPGA Bank68 Global clock pins.	NA
		IO_L13N_T2L_N1_GC_QBC_68		F14			
2	300MHz	IO_L13P_T2L_N0_GC_QBC_71	71	J26	1.8V, LVDS	LVDS reference clock for FPGA DDR4 SDRAM2. This is connected to FPGA Bank71 Global clock pins.	NA
		IO_L13N_T2L_N1_GC_QBC_71		H26			NA
3	125MHz	IO_L7P_HDGC_AD5P_92	92	AN22	1.8V, LVDS	Reference clock for FPGA. This is connected to FPGA Bank92 HDGC Global clock pin.	NA
		IO_L7N_HDGC_AD5N_92		AN21			NA
4	100MHz	MGTREFCLK0P_228	228	AH11	1.8V, LVDS	Bank228 PCIe Reference Clock0.	NA
		MGTREFCLK0N_228		AH10			NA
5	125MHz	IO_L24P_T3U_N10_EMCCLK_65	65	AL27	1.8V, LVCMOS	External Master Clock	NA

2.3.1.4 FPGA Configuration & Status

In Kintex Ultrascale+ SOM, by default QSPI Flash is set as configuration device through mode pins. Memory configuration files are generated from the BIT file in Vivado is programmed to QSPI through JTAG.

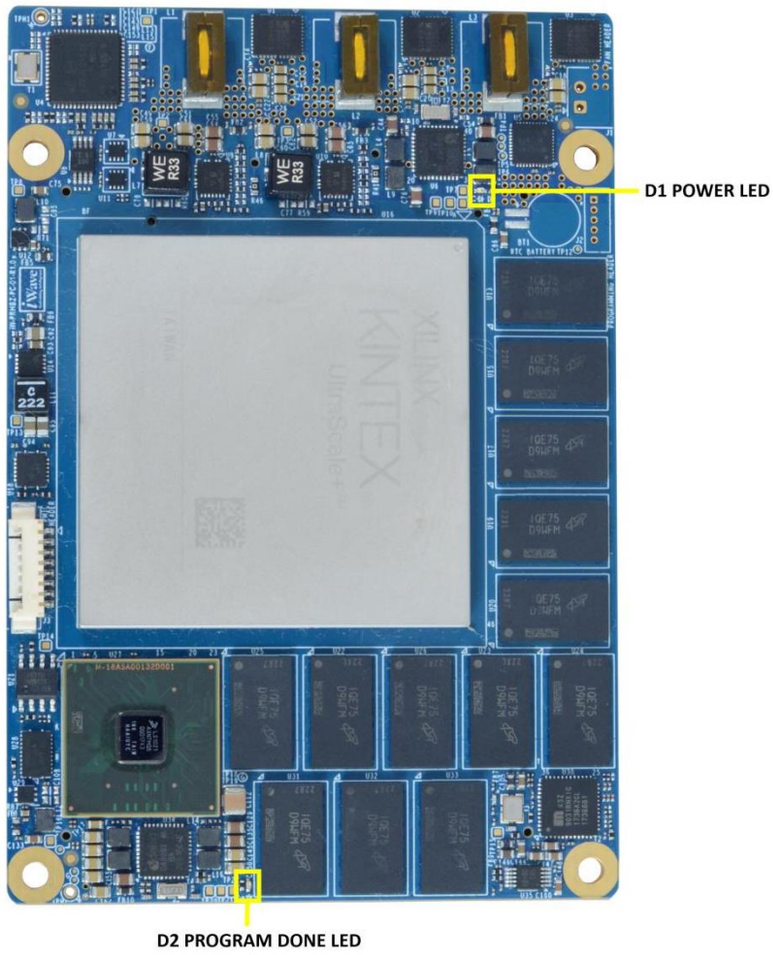


Figure 3: Indication LEDs

The Kintex Ultrascale+ FPGA SOM supports two LEDs for the Program Done indication and Power LED indication. LED D2 is for PROG_DONE and it is asserted for DONE indicates successful completion of configuration. LED D1 is for Power LED and it indicates the power which is the final in the power sequence.

The Kintex Ultrascale+ FPGA SOM supports three dedicated input and output configuration pins. By default, Weak pre - reconfiguration I/O pull-up resistors disabled for PUDC_B pin, Standard FPGA power-on delay time for POR_OVERRIDE pin is connected to Ground through 4.7K.

2.3.1.5 FPGA Mode Configuration

The Kintex Ultrascale+ SOM provides mode pins for selection of configuration device. The SOM supports 4-bit QSPI Flash and JTAG for the configuration of FPGA. By default, mode bit is configured to “001” for QSPI Flash as configuration device.

Below table provides the Mode bit status for available configuration devices of SOM.

MODE2	MODE1	MODE0	CONFIGURATION MODE
0	0	1	QSPI
1	0	0	JTAG

2.3.1.6 FPGA System Monitor/ADC

The Kintex Ultrascale+ FPGA contain one System Monitor block (SYSMONE4). It is used to enhance the overall safety, security and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

The SYSMON uses 10-bit 200kSPS ADC to digitize the sensor/ADC inputs. It monitors the die temperature of the FPGA and several internal supply nodes. The SYSMON can also monitor up to 17 external analog channels which includes 16 auxiliary analog inputs and one VP_VN dedicated input. The external auxiliary inputs can be routed through any IO Bank. The ADC voltage reference is selectable between an internal reference and the external pins VREFP and VREFN. In Kintex Ultrascale+ FPGA SOM, 1.25V external voltage reference is supported.

2.3.2 FPGA Memory

2.3.2.1 DDR4 SDRAM1 with ECC

The Kintex Ultrascale+ FPGA SOM supports 64bit, 4GB DDR4 RAM memory for FPGA. Four 16 bit, 1GB DDR4 SDRAM ICs is used to support RAM memory of 4GB. These DDR4 devices operates at 2666Mbps data rate. In Kintex Ultrascale+ FPGA SOM, Bank64, 65 & 66 is used for FPGA DDR4 SDRAM1 interface. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The Kintex Ultrascale+ FPGA SOM supports 300MHz LVDS DDR4 reference clock from on board clock synthesizer and connected to Bank64 AT21 & AT22 dedicated clock input pins through AC Coupling capacitors.

Note: Kintex Ultrascale+ FPGA SOM with -2 & -3 speed grade FPGA can support up to 2666Mbps data rate for FPGA DDR4.

2.3.2.2 DDR4 SDRAM2 with ECC

The Kintex Ultrascale+ FPGA SOM supports 64bit, 4GB DDR4 RAM memory for FPGA's FPGA. Four 16 bit, 1GB DDR4 SDRAM ICs is used to support RAM memory of 4GB. These DDR4 devices operates at 2666Mbps data rate. In Kintex Ultrascale+ FPGA SOM, Bank69, 70 & 71 is used for FPGA SDRAM2 DDR4 interface. Also, Both SDRAM1 and SDRAM2 supports two 4bit ECC for RAM memory. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The Kintex Ultrascale+ FPGA SOM supports 300MHz LVDS DDR4 reference clock from on board clock synthesizer and connected to Bank71 J26 & H26 dedicated clock input pins through AC Coupling capacitors.

Note: Kintex Ultrascale+ FPGA SOM with -2 & -3 speed grade FPGA can support up to 2666Mbps data rate for FPGA DDR4.

2.4 Layerscape Processor

2.4.1 Processor & Design Information

The Kintex Ultrascale+ FPGA (KU19P) SOM is based on Xilinx Kintex Ultrascale+ FPGA (KU19P) integrated with LS1021A Layerscape Processor. Featuring a pair of extremely power-efficient 32-bit Arm Cortex-A7 cores with ECC protected L1 and L2 cache memories for high reliability, running up to 1.2 GHz, and providing pre-silicon CoreMark performance of over 5,000, the LS102xA family delivers greater performance than any previous sub-4W communication processor. The Block Diagram of LS1021A from NXP website is shown below for reference.

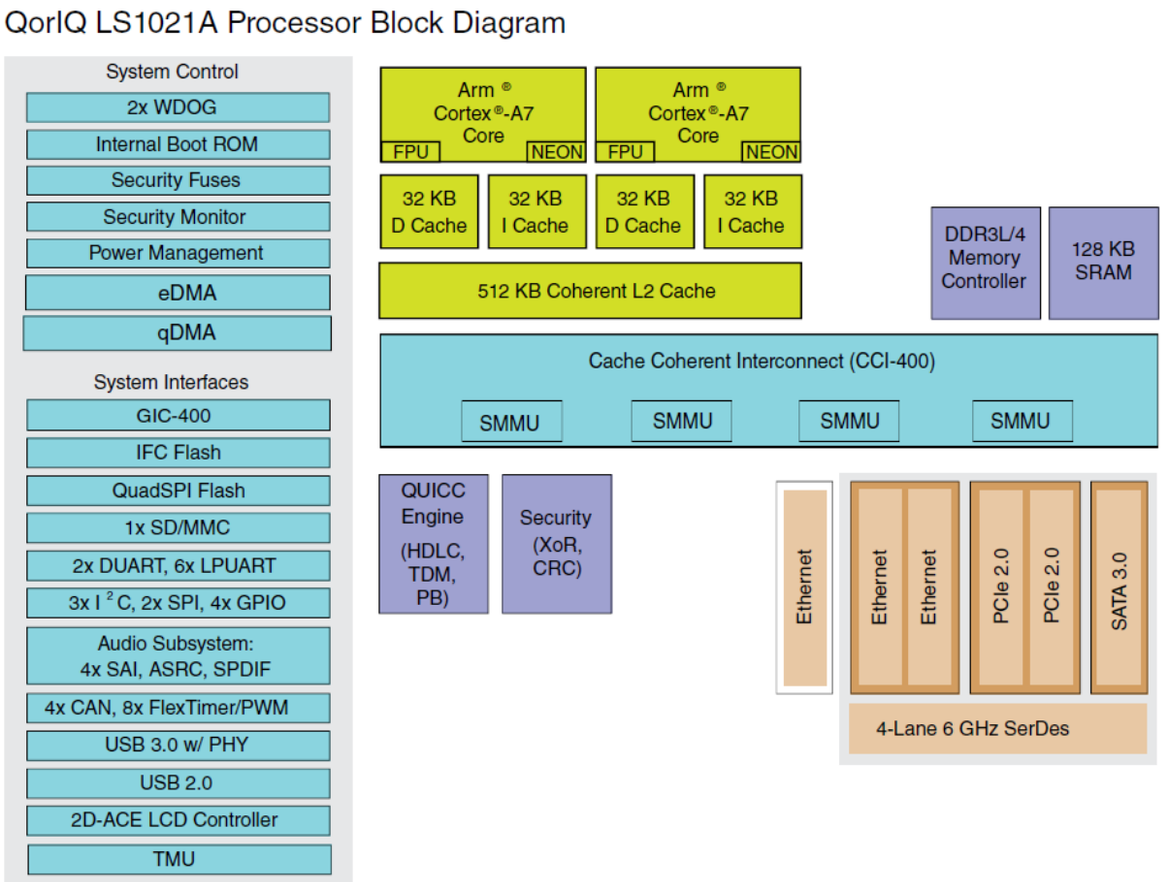


Figure 4: LS1021A Internal Block Diagram

2.4.1.1 LS1021A Booting and Configuration

The Kintex Ultrascale+ SOM integrates KU19P FPGA SoC with L1021A Layerscape processor. The RCW and U-boot is programmed in to the NOR Flash. On POR, Pre-Boot Loader (PBL) will fetch RCW configuration and PBL commands from NOR flash (chosen by rcw_src selection pins). Then executes u-boot from NOR flash.

2.4.1.2 LS1021A PMIC

The Kintex Ultrascale+ FPGA SOM supports Dialog semiconductor DA9062 PMIC and one regulator for LS1021A Processor. The I2C2 module of LS1021A is used for PMIC interface through LS1021A pins with I2C address 0x58.

PMIC supports reset output and connected to LS1021A (LS_PMIC_POR) for power on reset. Also, PMIC supports IRQ output for events indication and connected to LS1021A's GPIO (GPIO3_23).

The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from Board-to-Board Connector2 pin68 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

2.4.1.3 LS1021A Reference Clock

The Kintex Ultrascale+ FPGA SOM supports on board clock synthesizer for reference clock to LS1021A Processor. These reference clock from clock synthesizer to LS1021A is mentioned in the below table.

Sl. No	On-SOM Clock Synthesizer Frequency	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description	Stability
1	100MHz	DIFF_SYSCLK	G14	1.8V, LVDS	Differential system clock positive/negative.	NA
		DIFF_SYSCLK_B	F14			
2	100MHz	SD1_REF_CLK1_P	AC8	1.8V, LVDS	SerDes PLL 1 Reference Clock (Optional)	NA
		SD1_REF_CLK1_N	AB8			NA
3	100MHz	SD1_REF_CLK2_P	AC16	1.8V, LVDS	SerDes PLL 2 Reference Clock (Optional)	NA
		SD1_REF_CLK2_N	AB16			NA
4	100MHz	DDRCLK	H18	1.8V, LVCMOS	DDR controller complex clock. (Optional)	NA
5	66.66MHz	SYSCLK	F5	1.8V, LVCMOS	System Clock	NA

2.4.2 Processor Memory

2.4.2.1 DDR4 SDRAM with ECC for LS1021A

The Kintex Ultrascale+ FPGA SOM supports 32bit, 2GB DDR4 RAM memory for LS1021A. Two 16 bit, 1GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 2GB. Also, Kintex Ultrascale+ FPGA SOM supports one 4bit ECC for RAM memory. These DDR4 devices operates at 1600MTps data rate. DDR4 memory is connected to the DDR4 SDRAM controller of the LS1021A Processor. The RAM size can be expandable up to maximum of 8GB based on the availability of higher density 16bit DDR4 device.

2.4.2.2 NOR Flash

The Kintex Ultrascale+ FPGA SOM supports 250MB NOR Flash memory as boot-device of LS1021A Processor. The NOR Flash is used for programming RCW and U-boot for LS1021A booting purpose. This NOR Flash memory is connected to the Integrated Flash Controller of the LS1021A Processor and operates at 3.3V Voltage level.

2.4.2.3 MRAM

The Kintex Ultrascale+ FPGA SOM supports 4MB MRAM memory for storage purpose for Layerscape LS1021A Processor. This MRAM memory is connected to the Integrated Flash Controller of the LS1021A Processor and operates at 3.3V Voltage level.

2.4.2.4 SRAM

The Kintex Ultrascale+ FPGA SOM supports 512KB SPI Serial SRAM memory for storage purpose of LS1021A Processor. This SRAM memory is connected to the SPI2 lane of LS1021A and operates at 1.8V Voltage level.

2.5 FPGA to CPU Interfaces

2.5.1 PCIex1 Gen2

The Kintex Ultrascale+ SOM supports Generation2 PCIex1 interface between LS1021A Processor and KU19P. Channel3 of KU19P GTY Transceiver Bank228 is connected to LS1021A SERDES SD1 for PCIe interface.

Refer the below table for more details.

Signal Name	LS1021A Pin Name	LS1021A Pin No	KU19P Pin Name	KU19P Pin No.	Signal Type/ Termination*	Description
LS_SD1_RX0_P	SD1_RX0_P	AC10	MGTYTXP3_228	AF7	I, DIFF	SerDes Receive Data0 positive
LS_SD1_RX0_N	SD1_RX0_N	AB10	MGTYTXN3_228	AF6	I, DIFF	SerDes Receive Data0 negative
LS_SD1_TX0_P	SD1_TX0_P	W10	MGTYRXP3_228	AF2	O, DIFF	SerDes Transmit Data0 positive
LS_SD1_TX0_N	SD1_TX0_N	Y10	MGTYRXN3_228	AF1	O, DIFF	SerDes Transmit Data0 negative
LS_PERST0_PL_AR26(EC2_RX_CLK)	EC2_RX_CLK/GPIO3_26/USB2_DIR/FTM2_QD_PHA	R1	IO_T3U_N12_PERSTN0_65	AR26	O, 1.8V	PCIe Reset input from LS1021A to KU19P

** Signal directions mentioned in table are based on LS1021A chip.*

2.5.2 RGMII

The Kintex Ultrascale+ SOM supports RGMII interface between LS1021A Processor and KU19P through Ethernet Controller3 interface of LS1021A and PL HP Bank65 of KU19P.

Refer the below table for more details.

Signal Name	LS1021A Pin Name	LS1021A Pin No	KU19P Pin Name	KU19P Pin No.	Signal Type/ Termination*	Description
LS_EC3_TXCLK_PL_BC27_L6N_65	EC3_GTX_CLK/GPIO4_01/EC2_TX_ER/FTM3_CH0/EC3_TX_CLK	V5	IO_L6N_T0U_N11_AD6N_A21_65	BC27	O, 1.8V	Transmit Clock Out
LS_EC3_TXD0_PL_BC26_L6P_65	EC3_TXD0/GPIO3_31/TSEC_1588_PULSE_OUT2/FTM3_CH4	W4	IO_L6P_T0U_N10_AD6P_A20_65	BC26	O, 1.8V	Transmit Data

Signal Name	LS1021A Pin Name	LS1021A Pin No	KU19P Pin Name	KU19P Pin No.	Signal Type/ Termination*	Description
LS_EC3_TXD1_PL_BF25_L5N_65	EC3_TXD1/GPIO3_30/TSEC_1588_CLK_OUT/FTM3_CH5	W3	IO_L5N_T0U_N9_AD14N_A23_65	BF25	O, 1.8V	Transmit Data
LS_EC3_TXD2_PL_BE25_L5P_65	EC3_TXD2/GPIO3_29/TSEC_1588_ALARM_OUT1/FTM3_CH6	V4	IO_L5P_T0U_N8_AD14P_A22_65	BE25	O, 1.8V	Transmit Data
LS_EC3_TXD3_PL_BE26_L4N_65	EC3_TXD3/GPIO3_28/TSEC_1588_ALARM_OUT2/FTM3_CH7	V3	IO_L4N_T0U_N7_DBC_AD7N_A25_65	BE26	O, 1.8V	Transmit Data
LS_EC3_TXEN_PL_BD26_L4P_65	EC3_TX_EN/GPIO4_00/EC1_TX_ER/FTM3_CH1	Y3	IO_L4P_T0U_N6_DBC_AD7P_A24_65	BD26	O, 1.8V	Transmit Enable
LS_EC3_RXCLK_PL_BE28_L3N_65	EC3_RX_CLK/GPIO4_07/TSEC_1588_CLK_IN/FTM3_QD_PHA	V2	IO_L3N_T0L_N5_AD15N_A27_65	BE28	I, 1.8V	Receive Clock
LS_EC3_RXD0_PL_BD28_L3P_65	EC3_RXD0/GPIO4_06/TSEC_1588_TRIG_IN2/EC2_CRS/FTM3_CH2	AA1	IO_L3P_T0L_N4_AD15P_A26_65	BD28	I, 1.8V	Receive Data
LS_EC3_RXD1_PL_BF27_L2N_65	EC3_RXD1/GPIO4_05/TSEC_1588_PULSE_OUT1/FTM3_CH3	Y2	IO_L2N_T0L_N3_FWE_FCS2_B_65	BF27	I, 1.8V	Receive Data
LS_EC3_RXD2_PL_BE27_L2P_65	EC3_RXD2/GPIO4_04/EC1_COL/FTM3_EXTCLK	Y1	IO_L2P_T0L_N2_FOE_B_65	BE27	I, 1.8V	Receive Data
LS_EC3_RXD3_PL_BF29_L1N_65	EC3_RXD3/GPIO4_03/EC1_CRS/FTM3_FAULT	W1	IO_L1N_T0L_N1_DBC_RS1_65	BF29	I, 1.8V	Receive Data
LS_EC3_RXDDV_PL_BF28_L1P_65	EC3_RX_DV/GPIO4_08/TSEC_1588_TRIG_IN1/FTM3_QD_PHB	AA2	IO_L1P_T0L_N0_DBC_RS0_65	BF28	I, 1.8V	Receive Data Valid
LS_EC3_GTXCLK125_PL_AM27_L23P_65	EC3_GTX_CLK125/GPIO4_02/EC2_COL/USB2_DRVVBUS/EC3_RX_ER	Y4	IO_L23P_T3U_N8_I2C_SCLK_65	AM27	I, 1.8V	RGMII TX Reference Clock

** Signal directions mentioned in table are based on LS1021A chip.*

2.5.3 UART

The Kintex Ultrascale+ SOM supports UART interface between LS1021A Processor and KU19P through LPUART6 of LS1021A Processor and FPGA HP Bank65 of KU19P. Refer the below table for more details.

Signal Name	LS1021A Pin Name	LS1021A Pin No	KU19P Pin Name	KU19P Pin No.	Signal Type/ Termination*	Description
LS_LPUART6_SOUT_PL_AY25_L10N_65	SDHC_DAT3/GPIO2_08/LPUART3_RTS_B/LPUART6_SOUT	G1	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	AY25	O, 1.8V	Transmit Data
LS_LPUART6_SIN_PL_AW25_L10P_65	SDHC_CLK/GPIO2_09/LPUART3_CTS_B/LPUART6_SIN	D1	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	AW25	I, 1.8V	Receive Data

**Signal type is mentioned with respect to LS1021A processor*

2.5.4 Interrupt Request pins

The Kintex Ultrascale+ FPGA SOM supports 4 Interrupt Request signals from LS1021A to KU19P, which is connected from control signals of LS1021A to PL HP Bank 65 of KU19P.

Function Name	LS1021A Pin Name	LS1021A Pin No	KU19P Pin Name	KU19P Pin No.	Signal Type/ Termination	Description
LS_IRQ0_PL_AU25_CSI_ADV_65	IRQ0	G6	IO_T2U_N12_CSI_ADV_B_65	AU25	I, 1.8V	External Interrupt0 input from KU19P
LS_IRQ1_PL_BB27_L8N_65	IRQ1	G8	IO_L8N_T1L_N3_AD5N_A17_65	BB27	I, 1.8V	External Interrupt1 input from KU19P
LS_IRQ2_PL_BB26_L8P_65	IRQ2	W7	IO_L8P_T1L_N2_AD5P_A16_65	BB26	I, 1.8V	External Interrupt2 input from KU19P
LS_IRQ3_PL_BA28_L9N_65	IRQ3/GPIO1_23	R5	IO_L9N_T1L_N5_AD12N_A15_D31_65	BA28	I, 1.8V	External Interrupt3 input from KU19P
LS_IRQ4_PL_BA27_L9P_65	IRQ4/GPIO1_24/SDHC_VS	L2	IO_L9P_T1L_N4_AD12P_A14_D30_65	BA27	I, 1.8V	External Interrupt4 input from KU19P

2.6 Other On SOM Features

2.6.1 TPM Module

The Kintex Ultrascale+ FPGA SOM supports Trusted Platform Module (TPM) 2.0 Module through LS1021A Processor. The TPM technology is designed to provide hardware-based, security-related functions. A TPM chip is a secure crypto-processor that is

designed to carry out cryptographic operations. This TPM Module is connected to the SPI2 lane of LS1021A and operates at 1.8V Voltage level.

2.6.2 Temperature Sensor

The Kintex Ultrascale+ FPGA SOM supports Temperature sensor through both LS1021A Processor and KU19P SoC. In the temperature sensor the Channel 1 connected to the thermal diode pins in the LS1021A processor. And the Channel 2 is connected to the on-chip thermal diode pins of the KU19P SoC.

2.7 Board to Board Connector1

The Kintex Ultrascale+ FPGA SOM supports two 240 pin high speed ruggedized terminal strip connectors, one 240pin High-Speed High-Density connector and one 80pin High-Speed High-Density connector for interfaces expansion. All the effort is made in Kintex Ultrascale+ FPGA SOM design to provide the maximum interfaces of Kintex Ultrascale+ FPGA to the carrier board by adding these two Board to Board Connectors.

The Kintex Ultrascale+ FPGA SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J7) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240
Connector Part Number - QTH-120-01-L-D-A from Samtec
Mating Connector - QSH-120-01-L-D-A from Samtec
Staking Height - 5mm

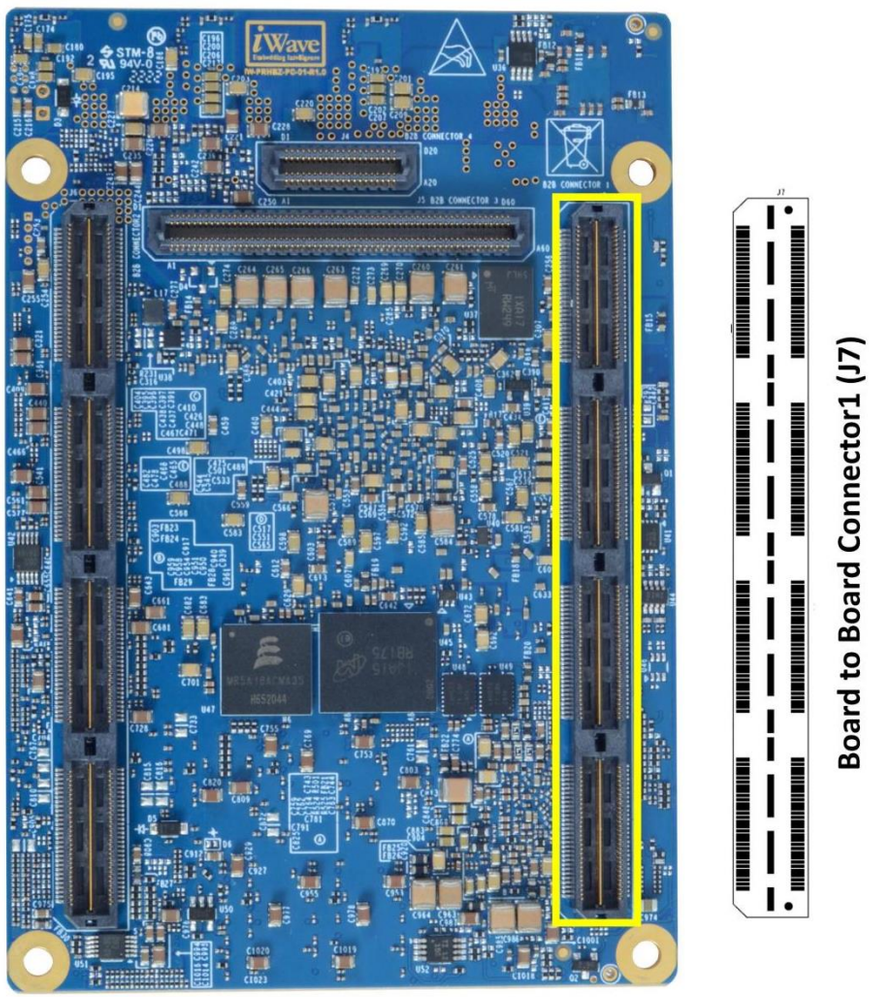


Figure 5: Board to Board Connector1

Table 3: Board to Board Connector1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GND	1	2	GND
GTYTXP0_225	3	4	GTREFCLK0P_225
GTYTXN0_225	5	6	GTREFCLK0N_225
GND	7	8	GND
GTYTXP1_225	9	10	NC
GTYTXN1_225	11	12	PL_AL22_LVDS92_L11P
GND	13	14	PL_AM22_LVDS92_L11N
GTYRXN1_225	15	16	PL_AU22_LVDS92_L3P
GTYRXP1_225	17	18	LS_GPIO3_22(EC2_RXD3)
GND	19	20	GND
GTYRXN0_225	21	22	PL_AP23_LVDS92_L8N_HDGC
GTYRXP0_225	23	24	PL_AN23_LVDS92_L8P_HDGC
GND	25	26	GND
PL_AV24_LVDS92_L2P	27	28	LS_GPIO3_18(EC2_TXD0)
PL_AW24_LVDS92_L2N	29	30	LS_GPIO3_17(EC2_TXD1)
PL_AL24_LVDS92_L10P	31	32	LS_GPIO3_24(EC2_RXD1)
PL_AM24_LVDS92_L10N	33	34	LS_GPIO4_09(TDMA_RXD)
GND	35	36	GND
GTYTXP2_225	37	38	LS_GPIO3_19(EC2_TXEN)
GTYTXN2_225	39	40	PL_AP24_LVDS92_L9N
GND	41	42	NC
GTYTXP3_225	43	44	PL_AN24_LVDS92_L9P
GTYTXN3_225	45	46	PL_AR22_LVDS92_L4P
GND	47	48	PL_AT22_LVDS92_L4N
GTYRXN3_225	49	50	PL_AV22_LVDS92_L3N
GTYRXP3_225	51	52	NC
GND	53	54	GND
GTYRXN2_225	55	56	NC
GTYRXP2_225	57	58	NC
GND	59	60	GND
GND	61	62	GND
LS_SD1_TX2_P	63	64	GTREFCLK1P_225
LS_SD1_TX2_N	65	66	GTREFCLK1N_225
GND	67	68	GND
NC	69	70	PL_AL21_LVDS92_L12P
NC	71	72	PL_AM21_LVDS92_L12N
GND	73	74	NC
SD1_REFCLKN	75	76	NC
SD1_REFCLKP	77	78	NC
GND	79	80	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
LS_SD1_RX2_N	81	82	NC
LS_SD1_RX2_P	83	84	NC
GND	85	86	GND
PL_AT24_LVDS92_L6P_HDGC	87	88	PL_AW23_LVDS92_L1N
PL_AU24_LVDS92_L6N_HDGC	89	90	PL_AV23_LVDS92_L1P
PL_AR23_LVDS92_L5P_HDGC	91	92	NC
PL_AT23_LVDS92_L5N_HDGC	93	94	NC
GND	95	96	GND
GTYTXP0_226	97	98	GTREFCLK0P_226
GTYTXN0_226	99	100	GTREFCLK0N_226
GND	101	102	GND
GTYTXP1_226	103	104	NC
GTYTXN1_226	105	106	NC
GND	107	108	NC
GTYRXN1_226	109	110	NC
GTYRXP1_226	111	112	NC
GND	113	114	GND
GTYRXN0_226	115	116	PL_AV28_LVDS65_L14N_A05_D21_GC
GTYRXP0_226	117	118	PL_AV27_LVDS65_L14P_A04_D20_GC
GND	119	120	GND
GND	121	122	GND
GTYTXP2_226	123	124	PL_AV26_LVDS65_L13P_A06_D22_GC
GTYTXN2_226	125	126	PL_AW26_LVDS65_L13N_A07_D23_GC
GND	127	128	NC
GTYTXP3_226	129	130	PL_AW28_LVDS65_L12P_A08_D24_GC
GTYTXN3_226	131	132	PL_AY28_LVDS65_L12N_A09_D25_GC
GND	133	134	NC
GTYRXN3_226	135	136	NC
GTYRXP3_226	137	138	NC
GND	139	140	GND
GTYRXN2_226	141	142	PL_AY27_LVDS65_L11N_A11_D27_GC
GTYRXP2_226	143	144	PL_AY26_LVDS65_L11P_A10_D26_GC
GND	145	146	GND
NC	147	148	NC
NC	149	150	NC
NC	151	152	NC
NC	153	154	NC
GND	155	156	GND
LS_USB1_TX_P	157	158	GTREFCLK1P_226
LS_USB1_TX_M	159	160	GTREFCLK1N_226
GND	161	162	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
NC	163	164	SYSMON_DXP
NC	165	166	SYSMON_DXN
GND	167	168	SYSMON_VN
CLK_GEN_IN_N	169	170	PL_AN27_LVDS65_L23N_PERSTN1_SDA
CLK_GEN_IN_P	171	172	NC
GND	173	174	GND
LS_USB1_RX_M	175	176	NC
LS_USB1_RX_P	177	178	NC
GND	179	180	GND
GND	181	182	GND
GTYTXP0_124	183	184	GTREFCLK0P_124
GTYTXN0_124	185	186	GTREFCLK0N_124
GND	187	188	GND
GTYTXP1_124	189	190	PL_AM14_LVDS67_L24N
GTYTXN1_124	191	192	PL_AL14_LVDS67_L24P
GND	193	194	PL_AT13_T3U_N12_67
GTYRXN1_124	195	196	PL_AT14_T2U_N12_67
GTYRXP1_124	197	198	PL_BB16_T1U_N12_67
GND	199	200	GND
GTYRXN0_124	201	202	NC
GTYRXP0_124	203	204	NC
GND	205	206	GND
NC	207	208	NC
NC	209	210	NC
NC	211	212	NC
NC	213	214	NC
GND	215	216	GND
GTYTXP2_124	217	218	GTREFCLK1P_124
GTYTXN2_124	219	220	GTREFCLK1N_124
GND	221	222	GND
GTYTXP3_124	223	224	NC
GTYTXN3_124	225	226	NC
GND	227	228	NC
GTYRXN3_124	229	230	NC
GTYRXP3_124	231	232	SOMPWR_EN
GND	233	234	GND
GTYRXN2_124	235	236	NC
GTYRXP2_124	237	238	NC
GND	239	240	GND

2.7.1 LS1021A Interfaces

The interfaces which are supported in Board-to-Board Connector1 from LS1021A Processor is explained in the following section

2.7.1.1 USB3.0

The LS1021A Layerscape processor supports USB3.0 interface through Board-to-Board Connector1 from USB PHY integrated in the Layerscape processor.

For more details on USB3.0 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
157	LS_USB1_TX_P	USB1_TX_P	B2	IO	USB PHY 3.0 Transmit Data Positive
159	LS_USB1_TX_M	USB1_TX_M	A2	IO	USB PHY 3.0 Transmit Data Negative
175	LS_USB1_RX_M	USB1_RX_M	A4	IO	USB PHY 3.0 Receive Data Negative
177	LS_USB1_RX_P	USB1_RX_P	B4	IO	USB PHY 3.0 Receive Data Positive

2.7.1.2 SerDes Interface

The Kintex Ultrascale+ FPGA SOM supports 1 highspeed SerDes lane and its reference clock through LS1021A Layerscape Processor in board-to-board connector1

For more details on SerDes Interface pinouts on Board-to-Board Connector1, refer the below table.

B2B-2 Pin No	B2B Connector1 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
63	LS_SD1_TX2_P	SD1_TX2_P	W13	O, DIFF	SerDes Transmit Data Positive
65	LS_SD1_TX2_N	SD1_TX2_N	Y13	O, DIFF	SerDes Transmit Data Negative
81	LS_SD1_RX2_N	SD1_RX2_N	AB13	I, DIFF	SerDes Receive Data Negative
83	LS_SD1_RX2_P	SD1_RX2_P	AC13	I, DIFF	SerDes Receive Data Positive
75	LS_SD1_REF_CLK2_N	SD1_REF_CLK2_N	AB16	I, DIFF	SerDes PLL 2 Reference Clock Negative
77	LS_SD1_REF_CLK2_P	SD1_REF_CLK2_P	AC16	I, DIFF	SerDes PLL 2 Reference Clock Positive

2.7.1.3 GPIOs From LS1021A

The Kintex Ultrascale+ FPGA SOM supports 6 GPIOs from LS1021A Layerscape Processor in board-to-board connector1

For more details on GPIOs pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector1 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
18	LS_GPIO3_22(EC2_RXD3)	EC2_RXD3/GPIO3_22/CAN4_RX/USB2_D3/FTM2_CH4	R2	O, 3V3	General Purpose I/O from LS1021A Processor
28	LS_GPIO3_18(EC2_TXD0)	EC2_TXD0/GPIO3_18/USB2_D4/FTM2_CH2	T3	I, 3V3	General Purpose I/O from LS1021A Processor
30	LS_GPIO3_17(EC2_TXD1)	EC2_TXD1/GPIO3_17/USB2_D5/FTM2_CH3	T4	I, 3V3	General Purpose I/O from LS1021A Processor
32	LS_GPIO3_24(EC2_RXD1)	EC2_RXD1/GPIO3_24/USB2_D1/FTM2_CH1	U1	I, 3V3	General Purpose I/O from LS1021A Processor
34	LS_GPIO4_09(TDMA_RXD)	TDMA_RXD/GPIO4_09/UC1_RXD7/SAI3_RX_DATA/FTM4_CH7/2D-ACE_D00	H3	I, 3V3	General Purpose I/O from LS1021A Processor
38	LS_GPIO3_19(EC2_TXEN)	EC2_TX_EN/GPIO3_19/USB2_STP/FTM2_FAULT	T5	O, 3V3	General Purpose I/O from LS1021A Processor

2.7.2 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Kintex Ultrascale+ FPGA is explained in the following section.

2.7.2.1 GTY High Speed Transceivers

The Kintex Ultrascale+ FPGA (KU19P) supports 32 GTY transceivers through 8 transceiver Quad (Bank 225, 226, 228, 229, 230, 231, 232 & 227) with line rate from 500Mbps to 32.75Gbps based on the speed grade of the FPGA. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

Kintex Ultrascale+ FPGA Speed Grade	GTY Transceiver line rate (min)	GTY Transceiver line rate (max)
-1L Speed Grade	0.5Gbps	12.5 Gbps
-1 Speed Grade	0.5 Gbps	25.785 Gbps
-2 Speed Grade	0.5 Gbps	28.21 Gbps
-3 Speed Grade	0.5 Gbps	32.75 Gbps

Note: For Backplane application, the transceiver maximum line rate may come down.

The Kintex Ultrascale+ FPGA SOM Supports 8 GTY transceivers along with the reference clock inputs (Bank 225 & 226) on Board-to-Board Conenctor1, 20 GTY transceivers through Five transceiver Quad (Bank 228, 229, 230, 231 & 232) on Board-to-Board Connector3 and 4 GTY transceivers along with reference clock inputs (Bank 227) on Board-to-Board Connector4.

In Kintex Ultrascale+ FPGA SOM, on board reference clock to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required peripheral standards on GTY transceivers. Also, on board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommended.

For more details on GTY transceiver pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank225 Transceiver Quad Pins						
3	GTYTXP0_225	MGTYTXP0_225	225	BF5	O, DIFF	GTY Bank225 channel0 High speed differential transmitter positive.
5	GTYTXN0_225	MGTYTXN0_225	225	BF4	O, DIFF	GTY Bank225 channel0 High speed differential transmitter negative.
9	GTYTXP1_225	MGTYTXP1_225	225	BD5	O, DIFF	GTY Bank225 channel1 High speed differential transmitter positive.
11	GTYTXN1_225	MGTYTXN1_225	225	BD4	O, DIFF	GTY Bank225 channel1 High speed differential transmitter negative.
15	GTYRXN1_225	MGTYRXN1_225	225	BA1	I, DIFF	GTY Bank225 channel1 High speed differential receiver negative.
17	GTYRXP1_225	MGTYRXP1_225	225	BA2	I, DIFF	GTY Bank225 channel1 High speed differential receiver positive.
21	GTYRXN0_225	MGTYRXN0_225	225	BC1	I, DIFF	GTY Bank225 channel0 High speed differential receiver negative.
23	GTYRXP0_225	MGTYRXP0_225	225	BC2	I, DIFF	GTY Bank225 channel0 High speed differential receiver positive.
37	GTYTXP2_225	MGTYTXP2_225	225	BB5	O, DIFF	GTY Bank225 channel2 High speed differential transmitter positive.
39	GTYTXN2_225	MGTYTXN2_225	225	BB4	O, DIFF	GTY Bank225 channel2 High speed differential transmitter negative.
43	GTYTXP3_225	MGTYTXP3_225	225	AV7	O, DIFF	GTY Bank225 channel3 High speed differential transmitter positive.
45	GTYTXN3_225	MGTYTXN3_225	225	AV6	O, DIFF	GTY Bank225 channel3 High speed differential transmitter negative.
49	GTYRXN3_225	MGTYRXN3_225	225	AV1	I, DIFF	GTY Bank225 channel3 High speed differential receiver negative.

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
51	GTYRXP3_225	MGTYRXP3_225	225	AV2	I, DIFF	GTY Bank225 channel3 High speed differential receiver positive.
55	GTYRXN2_225	MGTYRXN2_225	225	AW3	I, DIFF	GTY Bank225 channel2 High speed differential receiver negative.
57	GTYRXP2_225	MGTYRXP2_225	225	AW4	I, DIFF	GTY Bank225 channel2 High speed differential receiver positive.
4	GTREFCLK0P_225	MGTREFCLK0P_225	225	AW9	I, DIFF	GTY Bank225 differential reference clock0 positive.
6	GTREFCLK0N_225	MGTREFCLK0N_225	225	AW8	I, DIFF	GTY Bank225 differential reference clock0 negative.
64	GTREFCLK1P_225	MGTREFCLK1P_225	225	AV11	I, DIFF	GTY Bank225 differential reference clock1 positive.
66	GTREFCLK1N_225	MGTREFCLK1N_225	225	AV10	I, DIFF	GTY Bank225 differential reference clock1 negative.
Bank226 Transceiver Quad Pins						
97	GTYTXP0_226	MGTYTXP0_226	226	AU9	O, DIFF	GTY Bank226 channel0 High speed differential transmitter positive.
99	GTYTXN0_226	MGTYTXN0_226	226	AU8	O, DIFF	GTY Bank226 channel0 High speed differential transmitter negative.
103	GTYTXP1_226	MGTYTXP1_226	226	AT7	O, DIFF	GTY Bank226 channel1 High speed differential transmitter positive.
105	GTYTXN1_226	MGTYTXN1_226	226	AT6	O, DIFF	GTY Bank226 channel1 High speed differential transmitter negative.
109	GTYRXN1_226	MGTYRXN1_226	226	AT1	I, DIFF	GTY Bank226 channel1 High speed differential receiver negative.
111	GTYRXP1_226	MGTYRXP1_226	226	AT2	I, DIFF	GTY Bank226 channel1 High speed differential receiver positive.
115	GTYRXN0_226	MGTYRXN0_226	226	AU3	I, DIFF	GTY Bank226 channel0 High speed differential receiver negative.
117	GTYRXP0_226	MGTYRXP0_226	226	AU4	I, DIFF	GTY Bank226 channel0 High speed differential receiver positive.
123	GTYTXP2_226	MGTYTXP2_226	226	AR9	O, DIFF	GTY Bank226 channel2 High speed differential transmitter positive.
125	GTYTXN2_226	MGTYTXN2_226	226	AR8	O, DIFF	GTY Bank226 channel2 High speed differential transmitter negative.
129	GTYTXP3_226	MGTYTXP3_226	226	AP7	O, DIFF	GTY Bank226 channel3 High speed differential transmitter positive.
131	GTYTXN3_226	MGTYTXN3_226	226	AP6	O, DIFF	GTY Bank226 channel3 High speed differential transmitter negative.
135	GTYRXN3_226	MGTYRXN3_226	226	AP1	I, DIFF	GTY Bank226 channel3 High speed differential receiver negative.

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
137	GTYRXP3_226	MGTYRXP3_226	226	AP2	I, DIFF	GTY Bank226 channel3 High speed differential receiver positive.
141	GTYRXN2_226	MGTYRXN2_226	226	AR3	I, DIFF	GTY Bank226 channel2 High speed differential receiver negative.
143	GTYRXP2_226	MGTYRXP2_226	226	AR4	I, DIFF	GTY Bank226 channel2 High speed differential receiver positive.
98	GTREFCLK0P_226	MGTREFCLK0P_226	226	AT11	I, DIFF	GTY Bank226 differential reference clock0 positive.
100	GTREFCLK0N_226	MGTREFCLK0N_226	226	AT10	I, DIFF	GTY Bank226 differential reference clock0 negative.
158	GTREFCLK1P_226	MGTREFCLK1P_226	226	AP11	I, DIFF	GTY Bank226 differential reference clock0 positive.
160	GTREFCLK1N_226	MGTREFCLK1N_226	226	AP10	I, DIFF	GTY Bank226 differential reference clock1 negative.

2.7.2.2 FPGA IOs – HD BANK92

The Kintex Ultrascale+ FPGA SOM supports 11 DIFF IOs/22 Single Ended (SE) IOs on Board-to-Board Connector1 from FPGA High-Density (HD) Bank92. Upon these 11 DIFF IOs/22 SE IOs, up to 3 HDGC Global Clock Inputs and up to 22 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank92 is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for Bank92. By default, IO voltage of Bank92 is set as 1.2V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Kintex Ultrascale+ FPGA datasheet.

In the Kintex Ultrascale+ FPGA SOM, Bank92 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank92 signals are routed as DIFF IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins 22, 24,70, 72, 87, 88, 89, ,90, 91, 93 are HDGC Global Clock Input capable pins of Bank92. Also, Board to Board Connector1 pins 12, 14, 16, 22, 24, 27, 29, 31, 33, 40, 44, 46, 48, 50, 70, 72, 87, 88, 89, 90, 91, 93, and are PLSYSMON auxiliary analog Input capable pins of Bank92.

For more details on HD Bank92 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
27	PL_AV24_LVDS92_L2P	IO_L2P_AD10P_92	92	AV24	IO, 3.3V	Bank92 IO2 differential positive. Same pin can be configured as SYSMON differential analog input10 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
29	PL_AW24_LVDS92_L2N	IO_L2N_AD10N_92	92	AW24	IO, 3.3V	Bank92 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
31	PL_AL24_LVDS92_L10P	IO_L10P_AD2P_92	92	AL24	IO, 3.3V	Bank92 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
33	PL_AM24_LVDS92_L10N	IO_L10N_AD2N_92	92	AM24	IO, 3.3V	Bank92 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
87	PL_AT24_LVDS92_L6P_HDGC	IO_L6P_HDGC_AD6P_92	92	AT24	IO, 3.3V	Bank92 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input6 negative or Single ended I/O.
89	PL_AU24_LVDS92_L6N_HDGC	IO_L6N_HDGC_AD6N_92	92	AU24	IO, 3.3V	Bank92 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input6 positive or Single ended I/O.
91	PL_AR23_LVDS92_L5P_HDGC	IO_L5P_HDGC_AD7P_92	92	AR23	IO, 3.3V	Bank92 IO5 differential positive. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input7 positive or Single ended I/O.
93	PL_AT23_LVDS92_L5N_HDGC	IO_L5N_HDGC_AD7N_92	92	AT23	IO, 3.3V	Bank92 IO5 differential negative. Same pin can be configured as HDGC G0lobal Clock Input differential negative or PLSYSMON differential analog input7 negative or Single ended I/O.
12	PL_AL22_LVDS92_L11P	IO_L11P_AD1P_92	92	AL22	IO, 3.3V	Bank92 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
14	PL_AM22_LVDS 92_L11N	IO_L11N_AD1 N_92	92	AM22	IO, 3.3V	Bank92 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
16	PL_AU22_LVDS9 2_L3P	IO_L3P_AD9P_ 92	92	AU22	IO, 3.3V	Bank92 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
50	PL_AV22_LVDS9 2_L3N	IO_L3N_AD9N_ 92	92	AV22	IO, 3.3V	Bank92 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
22	PL_AP23_LVDS9 2_L8N_HDGC	IO_L8N_HDGC _AD4N_92	92	AP23	IO, 3.3V	Bank92 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input4 negative or Single ended I/O.
24	PL_AN23_LVDS9 2_L8P_HDGC	IO_L8P_HDGC_ AD4P_92	92	AN23	IO, 3.3V	Bank92 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input4 positive or Single ended I/O.
40	PL_AP24_LVDS9 2_L9N	IO_L9N_AD3N_ 92	92	AP24	IO, 3.3V	Bank92 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
44	PL_AN24_LVDS9 2_L9P	IO_L9P_AD3P_ 92	92	AN24	IO, 3.3V	Bank92 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
46	PL_AR22_LVDS9 2_L4P	IO_L4P_AD8P_ 92	92	AR22	IO, 3.3V	Bank92 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
48	PL_AT22_LVDS9 2_L4N	IO_L4N_AD8N_ 92	92	AT22	IO, 3.3V	Bank92 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
70	PL_AL21_LVDS92_L12P	IO_L12P_AD0P_92	92	AL21	IO, 3.3V	Bank92 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
72	PL_AM21_LVDS92_L12N	IO_L12N_AD0N_92	92	AM21	IO, 3.3V	Bank92 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
88	PL_AW23_LVDS92_L1N	IO_L1N_AD11N_92	92	AW23	IO, 3.3V	Bank92 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
90	PL_AV23_LVDS92_L1P	IO_L1P_AD11P_92	92	AV23	IO, 3.3V	Bank92 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.

**IO Type of IOs originating from KU19P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx KU19P FPGA datasheet.*

2.7.2.3 FPGA IOs – HP BANK65 & 67

The Kintex Ultrascale+ FPGA SOM supports 4 DIFF IOs/9 Single Ended (SE) IOs on Board-to-Board Connector1 from FPGA High-Performance (HP) Bank65 and 1 DIFF IOs/5 Single Ended (SE) IOs from FPGA High-Performance (HP) Bank67 Upon these 5 DIFF IOs/14 SE IOs, up to 4 HDGC Global Clock Inputs are available.

The IO voltage of Bank65 is connected from LDO2 and Bank67 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.14V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO2 & LDO4 to output appropriate IO voltage for Bank65 & 67. By default, IO voltage of Bank65 is set as 1.2V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Kintex Ultrascale+ FPGA datasheet.

In the Kintex Ultrascale+ FPGA SOM, Bank65 & 67 signals are routed as DIFF IOs to Board-to-Board Connector1. Even though Bank65 & 67 signals are routed as DIFF IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins 116, 118, 124, 126, 130, 132, 142 and 144 are HDGC Global Clock Input capable pins of Bank65.

For more details on HD Bank65 & 67 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
190	PL_AM14_LVDS 67_L24N	IO_L24N_T3U_ N11_67	67	AM14	IO, 1.8V	Bank67 IO24 differential negative. Same pin can be configured as Single ended I/O.
192	PL_AL14_LVDS6 7_L24P	IO_L24P_T3U_ N10_67	67	AL14	IO, 1.8V	Bank67 IO24 differential positive. Same pin can be configured as Single ended I/O.
194	PL_AT13_T3U_N 12_67	IO_T3U_N12_6 7	67	AT13	IO, 1.8V	Bank67 Single ended I/O.
196	PL_AT14_T2U_N 12_67	IO_T2U_N12_6 7	67	AT14	IO, 1.8V	Bank67 Single ended I/O.
198	PL_BB16_T1U_N 12_67	IO_T1U_N12_6 7	67	BB16	IO, 1.8V	Bank67 Single ended I/O.
170	PL_AN27_LVDS6 5_L23N_PERSTN 1_SDA	IO_L23N_T3U_ N9_PERSTN1_I2 C_SDA_65	65	AN27	IO, 1.8V	Bank65 IO23 differential negative. Same pin can be configured as Single ended I/O.
116	PL_AV28_LVDS6 5_L14N_A05_D2 1_GC	IO_L14N_T2L_N 3_GC_A05_D21 _65	65	AV28	IO, 1.8V	Bank65 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
118	PL_AV27_LVDS6 5_L14P_A04_D2 0_GC	IO_L14P_T2L_N 2_GC_A04_D20 _65	65	AV27	IO, 1.8V	Bank65 IO14 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
126	PL_AW26_LVDS 65_L13N_A07_D 23_GC	IO_L13N_T2L_N 1_GC_QBC_A07 _D23_65	65	AW26	IO, 1.8V	Bank65 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
124	PL_AV26_LVDS6 5_L13P_A06_D2 2_GC	IO_L13P_T2L_N 0_GC_QBC_A06 _D22_65	65	AV26	IO, 1.8V	Bank65 IO13 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
132	PL_AY28_LVDS6 5_L12N_A09_D2 5_GC	IO_L12N_T1U_ N11_GC_A09_D 25_65	65	AY28	IO, 1.8V	Bank65 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
130	PL_AW28_LVDS 65_L12P_A08_D 24_GC	IO_L12P_T1U_ N10_GC_A08_D 24_65	65	AW28	IO, 1.8V	Bank65 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
142	PL_AY27_LVDS65_L11N_A11_D27_GC	IO_L11N_T1U_N9_GC_A11_D27_65	65	AY27	IO, 1.8V	Bank65 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
144	PL_AY26_LVDS65_L11P_A10_D26_GC	IO_L11P_T1U_N8_GC_A10_D26_65	65	AY26	IO, 1.8V	Bank65 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.

**IO Type of IOs originating from KU19P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx KU19P FPGA datasheet.*

2.7.3 Power Control Input

The Kintex Ultrascale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin in Board-to-Board Connector1. Also, in Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance. For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
232	SOMPWR_EN	NA	NA	NA	I, 5V	Active High SOM power enable. *Important Note: High – SOM power ON Low – SOM Power OFF*
1, 7, 13, 19, 25, 35, 41, 47, 53, 59, 61, 67, 73, 79, 85, 95, 101, 107, 113, 119, 121, 127, 133, 139, 145, 155, 161, 167, 173, 179, 181, 187, 193, 199, 205, 215, 221, 227, 233, 239, 2, 8, 20, 26, 36, 54, 60, 62, 68, 80, 86, 96, 102, 114, 120, 122, 140, 146, 156, 162, 174, 180, 182, 188, 200, 206, 216, 222, 234, 240	GND	NA	NA	NA	Power	Ground.

2.8 Board to Board Connector2

The Kintex Ultrascale+ FPGA SOM Board to Board connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2 (J6) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A from Samtec

Mating Connector - QSH-120-01-L-D-A from Samtec

Staking Height - 5mm

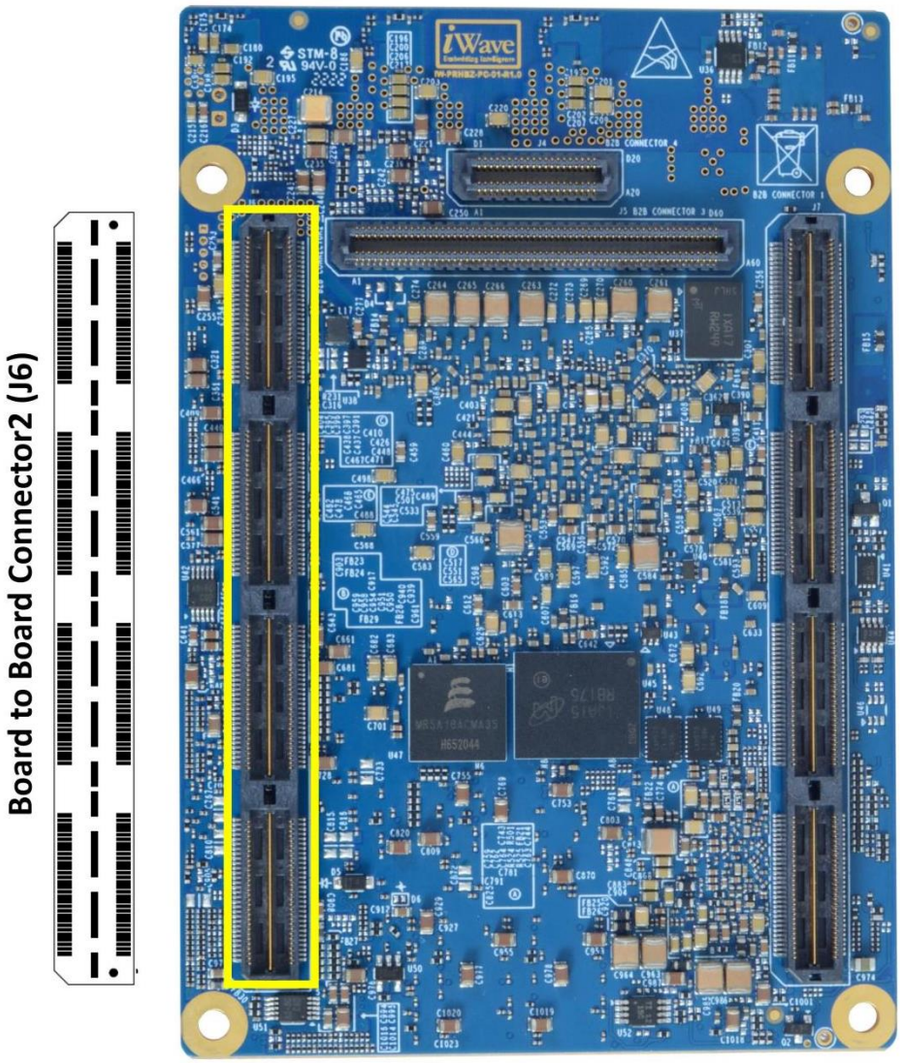


Figure 6: Board to Board Connector2

Table 4: Board to Board Connector2 Pinout

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
VCC_5V	1	2	VCC_5V
VCC_5V	3	4	VCC_5V
VCC_5V	5	6	VCC_5V
VCC_5V	7	8	VCC_5V
VCC_5V	9	10	VCC_5V
VCC_5V	11	12	VCC_5V
VCC_5V	13	14	VCC_5V
VCC_5V	15	16	VCC_5V
VCC_5V	17	18	VCC_5V
VCC_5V	19	20	VCC_5V
GND	21	22	GND
GND	23	24	GND
LS_JTAG_TRST	25	26	LS_USB1_D_M
JTAG_TDI	27	28	LS_USB1_D_P
JTAG_TMS	29	30	GND
JTAG_TCK	31	32	LS_GPIO3_16(EC2_TXD2)
JTAG_TDO	33	34	LS_USB1_ID
RESET_SW_IN	35	36	LS_USB1_VBUS
GND	37	38	LS_IIC2_SDA
GPHY_DTXRXM	39	40	PL_AP28_LVDS65_L20N_D09
GPHY_DTXRXP	41	42	LS_GPIO4_26(SDHC_DAT7)
GND	43	44	LS_GPIO4_16(TDMB_TXD)
GPHY_CTXRXM	45	46	LS_IIC1_SDA
GPHY_CTXRXP	47	48	LS_IIC1_SCL
GND	49	50	LS_LPUART3_SOUT
GPHY_BTXRXM	51	52	LS_LPUART3_SIN
GPHY_BTXRXP	53	54	LS_UART1_SOUT
GND	55	56	LS_UART1_SIN
GPHY_ATXRXM	57	58	GPHY_LINK_LED2
GPHY_ATXRXP	59	60	GPHY_ACTIVITY_LED1
LS_GPIO3_15(EC2_TXD3)	61	62	LS_GPIO4_19(CLK09)
PL_AN28_LVDS65_L20P_D08	63	64	LS_GPIO4_14(TDMB_RXD)
LS_GPIO4_25(SDHC_DAT6)	65	66	LS_GPIO4_15(TDMB_RSYNC)
NC	67	68	B2B_RTC
LS_GPIO4_18(TDMB_RQ)	69	70	LS_IIC2_SCL
LS_GPIO4_12(TDMA_TSYNC)	71	72	LS_GPIO4_24(SDHC_DAT5)
GND	73	74	GND
PL_AV16_LVDS67_L18N	75	76	B2B2_SCL
PL_AU16_LVDS67_L18P	77	78	B2B2_SDA

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
LS_LPUART5_SIN	79	80	PL_AY11_LVDS67_L8N
LS_LPUART5_SOUT	81	82	PL_AY12_LVDS67_L8P
PL_AR13_LVDS67_L22N_DBC	83	84	PL_BF13_LVDS67_L1N
PL_AP13_LVDS67_L22P_DBC	85	86	PL_BF14_LVDS67_L1P
PL_AR16_LVDS67_L19P_DBC	87	88	PL_BC14_LVDS67_L6P
PL_AR15_LVDS67_L19N_DBC	89	90	PL_BC13_LVDS67_L6N
PL_AL15_LVDS67_L23P	91	92	PL_AU13_LVDS67_L15P
PL_AM15_LVDS67_L23N	93	94	PL_AV13_LVDS67_L15N
PL_BD13_LVDS67_L4P_DBC	95	96	PL_AV14_LVDS67_L16N_QBC
PL_BE13_LVDS67_L4N_DBC	97	98	PL_AU14_LVDS67_L16P_QBC
PL_AN14_LVDS67_L21P	99	100	PL_BB15_LVDS67_L10P_QBC
PL_AN13_LVDS67_L21N	101	102	PL_BB14_LVDS67_L10N_QBC
PL_AP15_LVDS67_L20P	103	104	PL_BA12_LVDS67_L7P_QBC
PL_AP14_LVDS67_L20N	105	106	PL_BB12_LVDS67_L7N_QBC
GND	107	108	GND
PL_AW16_LVDS67_L14P_GC	109	110	PL_AW14_LVDS67_L13P_GC
PL_AW15_LVDS67_L14N_GC	111	112	PL_AW13_LVDS67_L13N_GC
GND	113	114	GND
PL_AY13_LVDS67_L12P_GC	115	116	PL_BA15_LVDS67_L11P_GC
PL_BA13_LVDS67_L12N_GC	117	118	PL_BA14_LVDS67_L11N_GC
GND	119	120	GND
PL_AY15_LVDS67_L9N	121	122	PL_AN18_LVDS66_L19P_DBC
PL_AY16_LVDS67_L9P	123	124	PL_AN17_LVDS66_L19N_DBC
PL_BE16_LVDS67_L3N	125	126	PL_AW20_LVDS66_L9P
PL_BD16_LVDS67_L3P	127	128	PL_AY20_LVDS66_L9N
GND	129	130	GND
PL_AL20_LVDS66_L24P	131	132	PL_AL17_LVDS66_L22P_DBC
PL_AM20_LVDS66_L24N	133	134	PL_AM17_LVDS66_L22N_DBC
PL_AN19_LVDS66_L20P	135	136	PL_AM16_LVDS66_L21P
PL_AP19_LVDS66_L20N	137	138	PL_AN16_LVDS66_L21N
PL_BD15_LVDS67_L5P	139	140	PL_AL19_LVDS66_L23P
PL_BD14_LVDS67_L5N	141	142	PL_AM19_LVDS66_L23N
PL_BF15_LVDS67_L2N	143	144	PL_AP18_LVDS66_L17P
PL_BE15_LVDS67_L2P	145	146	PL_AR18_LVDS66_L17N
PL_AP20_LVDS66_L18P	147	148	PL_BD18_LVDS66_L3P
PL_AR20_LVDS66_L18N	149	150	PL_BE18_LVDS66_L3N
PL_AY18_LVDS66_L8P	151	152	PL_BE17_LVDS66_L1P_DBC
PL_BA18_LVDS66_L8N	153	154	PL_BF17_LVDS66_L1N_DBC
PL_AV21_LVDS66_L10P_QBC	155	156	PL_AR17_LVDS66_L16P_QBC
PL_AW21_LVDS66_L10N_QBC	157	158	PL_AT17_LVDS66_L16N_QBC
PL_BC19_LVDS66_L4P_DBC	159	160	PL_BF18_LVDS66_L2N

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
PL_BD19_LVDS66_L4N_DBC	161	162	PL_BF19_LVDS66_L2P
PL_BB19_LVDS66_L6P	163	164	PL_AT18_LVDS66_L15P
PL_BC18_LVDS66_L6N	165	166	PL_AU17_LVDS66_L15N
GND	167	168	GND
PL_AT20_LVDS66_L14P_GC	169	170	PL_AV19_LVDS66_L12P_GC
PL_AU20_LVDS66_L14N_GC	171	172	PL_AW19_LVDS66_L12N_GC
GND	173	174	GND
PL_AT19_LVDS66_L13P_GC	175	176	PL_AV18_LVDS66_L11P_GC
PL_AU19_LVDS66_L13N_GC	177	178	PL_AW18_LVDS66_L11N_GC
GND	179	180	GND
PL_BC17_LVDS66_L5N	181	182	PL_AY17_LVDS66_L7P_QBC
PL_BB17_LVDS66_L5P	183	184	PL_BA17_LVDS66_L7N_QBC
GND	185	186	GND
NC	187	188	NC
NC	189	190	NC
GND	191	192	GND
NC	193	194	NC
NC	195	196	NC
GND	197	198	GND
NC	199	200	NC
NC	201	202	NC
GND	203	204	GND
NC	205	206	LS_SD1_RX3_P
NC	207	208	LS_SD1_RX3_N
GND	209	210	GND
NC	211	212	SD1_TX3_P
NC	213	214	SD1_TX3_N
GND	215	216	GND
NC	217	218	NC
NC	219	220	NC
GND	221	222	GND
NC	223	224	NC
NC	225	226	NC
GND	227	228	GND
LS_SD1_RX1_P	229	230	NC
LS_SD1_RX1_N	231	232	NC
GND	233	234	GND
SD1_TX1_P	235	236	NC
SD1_TX1_N	237	238	NC
GND	239	240	GND

2.8.1 LS1021A Interfaces

The interfaces which are supported in Board-to-Board Conenector2 from LS1021A Processor is explained in the following section.

2.8.1.1 Gigabit Ethernet Interface

The Kintex Ultrascale+ FPGA SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2.The MAC is integrated in the LS1021A Processor and connected to the external Gigabit Ethernet PHY "KSZ9031RNXIC" on SOM. This Gigabit Ethernet PHY is interfaced with Ethernet Controller 1 RGMII interface of LS1021A and works at 1.8V IO voltage level.

In Kintex Ultrascale+ FPGA SOM, LS1021A GPIO "LS_ETH_RSTN_GPIO4_23(SDHC_DAT4)" is used for Ethernet PHY reset. Also, SOM supports Ethernet PHY interrupt through LS1021A GPIO "LS_ETH_INT_GPIO1_25(IRQ5)". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magjack is required on the carrier board.

In Kintex Ultrascale+ FPGA SOM, Ethernet PHY Address is fixed to 001 as per below table.

PHYADDRESS2	PHYADDRESS1	PHYADDRESS0	Ethernet PHY Address
PHYAD2	GPHY_LINK_LED2	GPHY_ACTIVITY_LED1	1
0(PD)	0(PD)	1(PU)	

Important Note: GPHY_ACTIVITY_LED1 signal is muxed with PHYADDRESS2 pin. The same GPHY_ACTIVITY_LED1 signal is connected to 60th pin of Board to Board connector2 to support Gigabit Ethernet Activity LED.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
59	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
57	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
53	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
51	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
47	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
45	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
41	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
39	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
60	GPHY_ACTIVITY_LED1	NA	NA	NA	O, 2.5V CMOS/ 10K PD	Gigabit Ethernet 1000Mbps Link status LED (Active High).
58	GPHY_LINK_LED2	NA	NA	NA	O, 2.5V CMOS/ 10K PD	Gigabit Ethernet Activity LED (Active High).

2.8.1.2 USB2.0 Interface

The Kintex Ultrascale+ FPGA SOM supports one USB2.0 & 3.0 OTG interface on Board-to-Board Connector2 & 1. USB1 controller of LS1021A is used for USB2.0 & 3.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 & 3.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

Also, Kintex Ultrascale+ FPGA SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
26	LS_USB1_D_M	USB1_D_M	C3	IO	USB PHY Data Minus
28	LS_USB1_D_P	USB1_D_P	D3	IO	USB PHY Data Plus
34	LS_USB1_ID	USB1_ID	C3	I	USB PHY ID Detect
36	LS_USB1_VBUS	USB1_VBUS	C1	I,5V	USB VBUS for VBUS monitoring.

2.8.1.3 Debug UART Interface

The Kintex Ultrascale+ FPGA SOM supports one Debug UART interface on Board-to-Board Connector2. The DUART controller of LS1021A is used for Debug UART interface. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
54	LS_UART1_SOUT	UART1_SOUT/GPIO1_15	N1	O	Debug UART Transmit data
56	LS_UART1_SIN	UART1_SIN/GPIO1_17	M1	I	Debug UART Receive data

2.8.1.4 Data UART Interface

The Kintex Ultrascale+ FPGA SOM supports two DATA UART interface on Board-to-Board Connector2. The pins from eSDHC controller of alternate function are used in the Data UART interface. This controller supports full-duplex asynchronous receiver and transmitter path with autobaud rates.

For more details on Data UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
50	LS_LPUART3_SOUT	SDHC_CMD/GPIO2_04/LPUART3_SOUT	E2	O	Data UART Transmit Data
52	LS_LPUART3_SIN	SDHC_DAT0/GPIO2_05/LPUART3_SIN	E1	I	Data UART Receive Data
81	LS_LPUART5_SOUT	SDHC_DAT1/GPIO2_06/LPUART2_RTS_B/ LPUART5_SOUT	F2	O	Data UART Transmit Data
79	LS_LPUART5_SIN	SDHC_DAT2/GPIO2_07/LPUART2_CTS_B/ LPUART5_SIN	F1	I	Data UART Receive Data

2.8.1.5 I2C Interface

The Kintex Ultrascale+ FPGA SOM supports two I2C interface on Board-to-Board Connector2. The I2C controller of LS1021A processor's is used for I2C interface with the standard NXP I2C bus protocol. It can function as a master or a slave in a multi-master design. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C2 interface is also connected to On-SOM PMIC with I2C address 0x58 in the Kintex Ultrascale+ FPGA SOM. Also, one more I2C interface (I2C1) can be taken out on Board-to-Board Connector2.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
46	LS_IIC1_SDA	IIC1_SDA	P6	IO	I2C1 Serial Data
48	LS_IIC1_SCL	IIC1_SCL	N6	O	I2C1 Serial Clock
76	LS_IIC2_SCL	IIC2_SCL/GPIO4_27/SDHC_CD_B/SPI2_PCS3	K1	O	I2C2 Serial Clock
78	LS_IIC2_SDA	IIC2_SDA/GPIO4_28/SDHC_WP/ SPI2_PCS4	L1	IO	I2C2 Serial Data

2.8.1.6 JTAG Interface

The Kintex Ultrascale+ FPGA SOM supports JTAG interface on Board-to-Board Connector2. Both LS1021A and KU19P share a common set of JTAG pins in the Board-to-Board2 connector and each have their own TAP controller. KU19P and LS1021A's JTAG signals are given to JTAG Selection 2:1 Mux IC which will select according to JTAG_SEL configuration.

Refer the below table for JTAG selection details.

JTAG_SEL	JTAG Controller
0	LS1021A
1	KU19P

By default, the JTAG_SEL will be high and KU19P will be selected as JTAG controller. Refer the below given pinout for more details.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
27	JTAG_TDI	TDI_0	0	AE15	I, 1.8V LVCMOS/ 4.7K	JTAG Test Data Input.
29	JTAG_TMS	TMS_0	0	AG15	I, 1.8V LVCMOS/ 4.7K	JTAG Test Mode Select.
31	JTAG_TCK	TCK_0	0	AE13	I, 1.8V LVCMOS/ 4.7K	JTAG Test Clock.
33	JTAG_TDO	TDO_0	0	AC13	O, 1.8V LVCMOS	JTAG Test Data Output.

If the JTAG_SEL pin is low it will select LS1021A as JTAG controller. Refer the below pinout for more details.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
25	LS_JTAG_TRST	TRST_B	F6	I, 1.8V LVCMOS	JTAG Test Reset from LS1021A
27	JTAG_TDI	TDI	E7	I, 1.8V LVCMOS/ 4.7K	JTAG Test Data Input.
29	JTAG_TMS	TMS	F8	I, 1.8V LVCMOS/ 4.7K	JTAG Test Mode Select.
31	JTAG_TCK	TCK	E8	I, 1.8V LVCMOS/ 4.7K	JTAG Test Clock.
33	JTAG_TDO	TDO	F7	O, 1.8V LVCMOS	JTAG Test Data Output.

2.8.1.7 SerDes Interface

The Kintex Ultrascale+ FPGA SOM supports 2 highspeed SerDes lanes through LS1021A Layerscape Processor in board-to-board connector2

For more details on SerDes Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
229	LS_SD1_RX1_P	SD1_RX1_P	AC11	I, DIFF	SerDes Receive Data1 Positive
231	LS_SD1_RX1_N	SD1_RX1_N	AB11	I, DIFF	SerDes Receive Data1 Negative
235	LS_SD1_TX1_P	SD1_TX1_P	W11	O, DIFF	SerDes Transmit Data1 Positive
237	LS_SD1_TX1_N	SD1_TX1_N	Y11	O, DIFF	SerDes Transmit Data1 Negative
206	LS_SD1_RX3_P	SD1_RX3_P	AC14	I, DIFF	SerDes Receive Data3 Positive
208	LS_SD1_RX3_N	SD1_RX3_N	AB14	I, DIFF	SerDes Receive Data3 Negative
212	LS_SD1_TX3_P	SD1_TX3_P	W14	O, DIFF	SerDes Transmit Data3 Positive
214	LS_SD1_TX3_N	SD1_TX3_N	Y14	O, DIFF	SerDes Transmit Data3 Negative

2.8.1.8 GPIOs From LS1021A

The Kintex Ultrascale+ FPGA SOM supports 10 GPIOs from LS1021A Layerscape Processor in board-to-board connector1

For more details on GPIOs pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
32	LS_GPIO3_16(EC2_TXD2)	EC2_TXD2/GPIO3_16/CAN3_TX/USB2_D6/FTM2_CH7	R3	IO, 3V3	General Purpose I/O from LS1021A
44	LS_GPIO4_16(TDMB_TXD)	TDMB_TXD/GPIO4_16/UC3_TXD7/SPDIF_OUT/SAI4_TX_DATA/FTM4_CH0/2D-ACE_D07	M3	IO, 1.8V	General Purpose I/O from LS1021A
61	LS_GPIO3_15(EC2_TXD3)	EC2_TXD3/GPIO3_15/CAN4_TX/USB2_D7/FTM2_CH5	R4	IO, 1.8V	General Purpose I/O from LS1021A
62	LS_GPIO4_19(CLK09)	CLK09/GPIO4_19/BRGO2/SAI3_RX_BCLK/FTM4_QD_PHA/2D-ACE_D10	K5	IO, 1.8V	General Purpose I/O from LS1021A
64	LS_GPIO4_14(TDMB_RXD)	TDMB_RXD/GPIO4_14/UC3_RXD7/SPDIF_IN/SAI4_RX_DATA/FTM4_CH2/2D-ACE_D05	K3	IO, 1.8V	General Purpose I/O from LS1021A
65	LS_GPIO4_25(SDHC_DAT6)	SDHC_DAT6/GPIO4_25/USB1_DRVVBUS/SDHC_DAT0_DIR	J2	IO, 1.8V	General Purpose I/O from LS1021A
66	LS_GPIO4_15(TDMB_RSYNC)	TDMB_RSYNC/GPIO4_15/UC3_CTSB_RXDV/SPDIF_PLOCK/SAI4_TX_BCLK/FTM4_CH1/2D-ACE_D06	L3	IO, 1.8V	General Purpose I/O from LS1021A
69	LS_GPIO4_18(TDMB_RQ)	TDMB_RQ/GPIO4_18/UC3_CDB_RXER/SPDIF_EXTCLK/SAI4_RX_BCLK/FTM4_EXTCLK/2D-ACE_D09	K4	IO, 1.8V	General Purpose I/O from LS1021A
71	LS_GPIO4_12(TDMA_TSYNC)	TDMA_TSYNC/GPIO4_12/UC1_RTSB_TXEN/SAI3_TX_SYNC/FTM4_CH4/2D-ACE_D03	J5	IO, 1.8V	General Purpose I/O from LS1021A
42	LS_GPIO4_26(SDHC_DAT7)	SDHC_DAT7/GPIO4_26/USB1_PWRFAULT/SDHC_DAT123_DIR	J1	IO, 1.8V	General Purpose I/O from LS1021A

2.8.2 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Kintex Ultrascale+ FPGA is explained in the following section.

2.8.2.1 FPGA IOs – HP BANK66,65

The Kintex Ultrascale+ FPGA SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector2 from FPGA's High Performance (HP) Bank66. Upon these 24 LVDS IOs/48 SE IOs, up to 4 GC Global Clock Inputs and up to 16 SYSMON auxiliary analog inputs are available. From HP Bank65 2 Single Ended (SE) IOs also is available. The IO voltage of Bank66 is connected from LDO3 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO3 to output appropriate IO voltage for Bank66. By default, IO voltage of Bank67 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Kintex Ultrascale+ FPGA datasheet.

In the Kintex Ultrascale+ FPGA SOM, Bank66 signals are routed as LVDS IOs to Board-to-Board Connector2. Even though Bank66 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector2 pins 169, 170, 171, 172, 176, 178, and 177 are GC Global Clock Input capable pins of Bank66. Also, Board to Board Connector2 pins 122, 124, 126, 128, 132, 134, 135, 136, 137, 138, 144, 146, 147, 148, 149, 150, 151, 153, 155, 156, 157, 158, 159, 161, 163, 164, 166, 181, 182, 183 and 184 are SYSMON auxiliary analog Input capable pins of Bank66.

For more details on HP Bank66 pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
131	PL_AL20_LVDS66_L24P	IO_L24P_T3U_N10_66	66	AL20	IO, 1.8V	Bank66 IO24 differential positive Same pin can be configured as Single ended I/O.
133	PL_AM20_LVDS66_L24N	IO_L24N_T3U_N11_66	66	AM20	IO, 1.8V	Bank66 IO24 differential negative Same pin can be configured as Single ended I/O.
135	PL_AN19_LVDS66_L20P	IO_L20P_T3L_N2_AD1P_66	66	AN19	IO, 1.8V	Bank66 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
137	PL_AP19_LVDS66_L20N	IO_L20N_T3L_N3_AD1N_66	66	AP19	IO, 1.8V	Bank66 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
147	PL_AP20_LVDS66_L18P	IO_L18P_T2U_N10_AD2P_66	66	AP20	IO, 1.8V	Bank66 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
149	PL_AR20_LVDS66_L18N	IO_L18N_T2U_N11_AD2N_66	66	AR20	IO, 1.8V	Bank66 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
151	PL_AY18_LVDS66_L8P	IO_L8P_T1L_N2_AD5P_66	66	AY18	IO, 1.8V	Bank66 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
153	PL_BA18_LVDS66_L8N	IO_L8N_T1L_N3_AD5N_66	66	BA18	IO, 1.8V	Bank66 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
155	PL_AV21_LVDS66_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_66	66	AV21	IO, 1.8V	Bank66 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
157	PL_AW21_LVDS66_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_66	66	AW21	IO, 1.8V	Bank66 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
159	PL_BC19_LVDS66_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_66	66	BC19	IO, 1.8V	Bank66 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
161	PL_BD19_LVDS66_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_66	66	BD19	IO, 1.8V	Bank66 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
163	PL_BB19_LVDS66_L6P	IO_L6P_T0U_N10_AD6P_66	66	BB19	IO, 1.8V	Bank66 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
165	PL_BC18_LVDS66_L6N	IO_L6N_T0U_N11_AD6N_66	66	BC18	IO, 1.8V	Bank66 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
169	PL_AT20_LVDS66_L14P_GC	IO_L14P_T2L_N2_GC_66	66	AT20	IO, 1.8V	Bank68 IO14 differential positive Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
171	PL_AU20_LVDS66_L14N_GC	IO_L14N_T2L_N3_GC_66	66	AU20	IO, 1.8V	Bank68 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
175	PL_AT19_LVDS66_L13P_GC	IO_L13P_T2L_N0_GC_QBC_66	66	AT19	IO, 1.8V	Bank68 IO13 differential positive Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
177	PL_AU19_LVDS66_L13N_GC	IO_L13N_T2L_N1_GC_QBC_66	66	AU19	IO, 1.8V	Bank68 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
181	PL_BC17_LVDS66_L5N	IO_L5N_T0U_N9_AD14N_66	66	BC17	IO, 1.8V	Bank66 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
183	PL_BB17_LVDS66_L5P	IO_L5P_T0U_N8_AD14P_66	66	BB17	IO, 1.8V	Bank66 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
122	PL_AN18_LVDS66_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_66	66	AN18	IO, 1.8V	Bank66 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
124	PL_AN17_LVDS66_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_66	66	AN17	IO, 1.8V	Bank66 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
126	PL_AW20_LVDS66_L9P	IO_L9P_T1L_N4_AD12P_66	66	AW20	IO, 1.8V	Bank66 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
128	PL_AY20_LVDS66_L9N	IO_L9N_T1L_N5_AD12N_66	66	AY20	IO, 1.8V	Bank66 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
132	PL_AL17_LVDS66_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_66	66	AL17	IO, 1.8V	Bank66 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
134	PL_AM17_LVDS66_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_66	66	AM17	IO, 1.8V	Bank66 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
136	PL_AM16_LVDS66_L21P	IO_L21P_T3L_N4_AD8P_66	66	AM16	IO, 1.8V	PL Bank66 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
138	PL_AN16_LVDS66_L21N	IO_L21N_T3L_N5_AD8N_66	66	AN16	IO, 1.8V	Bank66 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
140	PL_AL19_LVDS66_L23P	IO_L23P_T3U_N8_66	66	AL19	IO, 1.8V	Bank66 IO23 differential positive. Same pin can be configured as Single ended I/O.
142	PL_AM19_LVDS66_L23N	IO_L23N_T3U_N9_66	66	AM19	IO, 1.8V	Bank66 IO23 differential negative. Same pin can be configured as Single ended I/O.
144	PL_AP18_LVDS66_L17P	IO_L17P_T2U_N8_AD10P_66	66	AP18	IO, 1.8V	Bank66 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
146	PL_AR18_LVDS66_L17N	IO_L17N_T2U_N9_AD10N_66	66	AR18	IO, 1.8V	Bank66 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
148	PL_BD18_LVDS66_L3P	IO_L3P_T0L_N4_AD15P_66	66	BD18	IO, 1.8V	Bank66 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
150	PL_BE18_LVDS66_L3N	IO_L3N_T0L_N5_AD15N_66	66	BE18	IO, 1.8V	Bank66 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
152	PL_BE17_LVDS66_L1P_DBC	IO_L1P_T0L_N0_DBC_66	66	BE17	IO, 1.8V	Bank66 IO1 differential positive. Same pin can be configured as Single ended I/O.
154	PL_BF17_LVDS66_L1N_DBC	IO_L1N_T0L_N1_DBC_66	66	BF17	IO, 1.8V	Bank66 IO1 differential negative. Same pin can be configured as Single ended I/O.
156	PL_AR17_LVDS66_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_66	66	AR17	IO, 1.8V	Bank66 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
158	PL_AT17_LVDS66_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_66	66	AT17	IO, 1.8V	Bank66 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
160	PL_BF18_LVDS66_L2N	IO_L2N_T0L_N3_66	66	BF18	IO, 1.8V	Bank66 IO2 differential negative. Same pin can be configured as Single ended I/O.
162	PL_BF19_LVDS66_L2P	IO_L2P_T0L_N2_66	66	BF19	IO, 1.8V	Bank66 IO2 differential positive. Same pin can be configured as Single ended I/O.
164	PL_AT18_LVDS66_L15P	IO_L15P_T2L_N4_AD11P_66	66	AT18	IO, 1.8V	Bank66 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
166	PL_AU17_LVDS66_L15N	IO_L15N_T2L_N5_AD11N_66	66	AU17	IO, 1.8V	Bank66 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
170	PL_AV19_LVDS66_L12P_GC	IO_L12P_T1U_N10_GC_66	66	AV19	IO, 1.8V	Bank66 IO12 differential positive Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
172	PL_AW19_LVDS66_L12N_GC	IO_L12N_T1U_N11_GC_66	66	AW19	IO, 1.8V	Bank66 IO12 differential negative Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
176	PL_AV18_LVDS66_L11P_GC	IO_L11P_T1U_N8_GC_66	66	AV18	IO, 1.8V	Bank66 IO11 differential positive Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
178	PL_AW18_LVDS66_L11N_GC	IO_L11N_T1U_N9_GC_66	66	AW18	IO, 1.8V	Bank66 IO11 differential negative Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
182	PL_AY17_LVDS66_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_66	66	AY17	IO, 1.8V	Bank66 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
184	PL_BA17_LVDS66_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_66	66	BA17	IO, 1.8V	Bank66 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
40	PL_AP28_LVDS65_L20N_D09	IO_L20N_T3L_N3_AD1N_D09_65	65	AP28	IO, 1.8V	Bank65 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
63	PL_AN28_LVDS65_L20P_D08	IO_L20P_T3L_N2_AD1P_D08_65	65	AN28	IO, 1.8V	Bank65 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.

**IO Type of IOs originating from KU19P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx KU19P FPGA datasheet.*

2.8.2.2 FPGA IOs –HP BANK67

The Kintex Ultrascale+ FPGA SOM supports 22 LVDS IOs/44 Single Ended (SE) IOs on Board-to-Board Connector2 from FPGA High Performance (HP) Bank68. Upon these 22 LVDS IOs/44 SE IOs, up to 4 GC Global Clock Inputs and up to 15 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank67 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for Bank67. By default, IO voltage of Bank68 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Kintex Ultrascale+ FPGA datasheet.

In the Kintex Ultrascale+ FPGA SOM, Bank67 signals are routed as LVDS IOs to Board-to-Board Connector2. Even though Bank67 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector2 pins 109, 110, 111, 115, 116, 117, 118 and 110 are GC Global Clock Input capable pins of Bank67. Also, Board to Board Connector2 pins 75, 77, 78, 80,

82, 83, 85, 87, 88, 89, 90, 92, 94, 95, 96, 97, 98, 99, 100, 101, 103, 104, 105, 106, 121, 123, 125, 127, 139 and 141 are PLSYSMON auxiliary analog Input capable pins of Bank67.

For more details on HP Bank68 pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
75	PL_AV16_LVDS67_L18N	IO_L18N_T2U_N11_AD2N_67	67	AV16	IO, 1.8V	Bank67 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
77	PL_AU16_LVDS67_L18P	IO_L18P_T2U_N10_AD2P_67	67	AU16	IO, 1.8V	Bank67 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
83	PL_AR13_LVDS67_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_67	67	AR13	IO, 1.8V	Bank67 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
85	PL_AP13_LVDS67_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_67	67	AP13	IO, 1.8V	Bank67 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
87	PL_AR16_LVDS67_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_67	67	AR16	IO, 1.8V	Bank67 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
89	PL_AR15_LVDS67_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_67	67	AR15	IO, 1.8V	Bank67 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
91	PL_AL15_LVDS67_L23P	IO_L23P_T3U_N8_67	67	AL15	IO, 1.8V	Bank67 IO23 differential positive. Same pin can be configured as Single ended I/O.
93	PL_AM15_LVDS67_L23N	IO_L23N_T3U_N9_67	67	AM15	IO, 1.8V	Bank67 IO23 differential negative. Same pin can be configured as Single ended I/O.
95	PL_BD13_LVDS67_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_67	67	BD13	IO, 1.8V	Bank67 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
97	PL_BE13_LVDS67_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_67	67	BE13	IO, 1.8V	Bank67 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
99	PL_AN14_LVDS67_L21P	IO_L21P_T3L_N4_AD8P_67	67	AN14	IO, 1.8V	Bank67 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
101	PL_AN13_LVDS67_L21N	IO_L21N_T3L_N5_AD8N_67	67	AN13	IO, 1.8V	Bank67 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
103	PL_AP15_LVDS67_L20P	IO_L20P_T3L_N2_AD1P_67	67	AP15	IO, 1.8V	Bank67 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
105	PL_AP14_LVDS67_L20N	IO_L20N_T3L_N3_AD1N_67	67	AP14	IO, 1.8V	Bank67 IO29 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
109	PL_AW16_LVDS67_L14P_GC	IO_L14P_T2L_N2_GC_67	67	AW16	IO, 1.8V	Bank67 IO14 differential positive. Same pin can be configured as GC Global Clock differential positive or Single ended I/O.
111	PL_AW15_LVDS67_L14N_GC	IO_L14N_T2L_N3_GC_67	67	AW15	IO, 1.8V	Bank67 IO14 differential negative. Same pin can be configured as GC Global Clock differential negative or Single ended I/O.
115	PL_AY13_LVDS67_L12P_GC	IO_L12P_T1U_N10_GC_67	67	AY13	IO, 1.8V	Bank67 IO12 differential positive. Same pin can be configured as GC Global Clock differential positive or Single ended I/O.
117	PL_BA13_LVDS67_L12N_GC	IO_L12N_T1U_N11_GC_67	67	BA13	IO, 1.8V	Bank67 IO12 differential negative. Same pin can be configured as GC Global Clock differential negative or Single ended I/O.
121	PL_AY15_LVDS67_L9N	IO_L9N_T1L_N5_AD12N_67	67	AY15	IO, 1.8V	Bank67 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
123	PL_AY16_LVDS67_L9P	IO_L9P_T1L_N4_AD12P_67	67	AY16	IO, 1.8V	Bank67 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
125	PL_BE16_LVDS67_L3N	IO_L3N_T0L_N5_AD15N_67	67	BE16	IO, 1.8V	Bank67 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
127	PL_BD16_LVDS67_L3P	IO_L3P_T0L_N4_AD15P_67	67	BD16	IO, 1.8V	Bank67 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
139	PL_BD15_LVDS67_L5P	IO_L5P_T0U_N8_AD14P_67	67	BD15	IO, 1.8V	Bank67 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
141	PL_BD14_LVDS67_L5N	IO_L5N_T0U_N9_AD14N_67	67	BD14	IO, 1.8V	Bank67 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
143	PL_BF15_LVDS67_L2N	IO_L2N_T0L_N3_67	67	BF15	IO, 1.8V	PL Bank67 IO2 differential negative. Same pin can be configured as Single ended I/O.
145	PL_BE15_LVDS67_L2P	IO_L2P_T0L_N2_67	67	BE15	IO, 1.8V	Bank67 IO2 differential positive. Same pin can be configured as Single ended I/O.
80	PL_AY11_LVDS67_L8N	IO_L8N_T1L_N3_AD5N_67	67	AY11	IO, 1.8V	Bank67 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
82	PL_AY12_LVDS67_L8P	IO_L8P_T1L_N2_AD5P_67	67	AY12	IO, 1.8V	Bank67 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
84	PL_BF13_LVDS67_L1N	IO_L1N_T0L_N1_DBC_67	67	BF13	IO, 1.8V	Bank67 IO1 differential negative. Same pin can be configured as Single ended I/O.
86	PL_BF14_LVDS67_L1P	IO_L1P_T0L_N0_DBC_67	67	BF14	IO, 1.8V	Bank67 IO1 differential positive. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
88	PL_BC14_LVDS67_L6P	IO_L6P_T0U_N10_AD6P_67	67	BC14	IO, 1.8V	Bank67 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
90	PL_BC13_LVDS67_L6N	IO_L6N_T0U_N11_AD6N_67	67	BC13	IO, 1.8V	Bank67 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
92	PL_AU13_LVDS67_L15P	IO_L15P_T2L_N4_AD11P_67	67	AU13	IO, 1.8V	Bank67 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
94	PL_AV13_LVDS67_L15N	IO_L15N_T2L_N5_AD11N_67	67	AV13	IO, 1.8V	PL Bank67 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
96	PL_AV14_LVDS67_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_67	67	AV14	IO, 1.8V	Bank67 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
98	PL_AU14_LVDS67_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_67	67	AU14	IO, 1.8V	Bank67 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
100	PL_BB15_LVDS67_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_67	67	BB15	IO, 1.8V	Bank67 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
102	PL_BB14_LVDS67_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_67	67	BB14	IO, 1.8V	Bank67 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
104	PL_BA12_LVDS67_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_67	67	BA12	IO, 1.8V	Bank67 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
106	PL_BB12_LVDS67_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_67	67	BB12	IO, 1.8V	Bank67 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
110	PL_AW14_LVDS67_L13P_GC	IO_L13P_T2L_N0_GC_QBC_67	67	AW14	IO, 1.8V	Bank67 IO7 differential positive. Same pin can be configured as GC Global Clock differential positive or Single ended I/O.
112	PL_AW13_LVDS67_L13N_GC	IO_L13N_T2L_N1_GC_QBC_67	67	AW13	IO, 1.8V	Bank67 IO13 differential negative. Same pin can be configured as GC Global Clock differential negative or Single ended I/O.
116	PL_BA15_LVDS67_L11P_GC	IO_L11P_T1U_N8_GC_67	67	BA15	IO, 1.8V	Bank67 IO11 differential positive. Same pin can be configured as GC Global Clock differential positive or Single ended I/O.
118	PL_BA14_LVDS67_L11N_GC	IO_L11N_T1U_N9_GC_67	67	BA14	IO, 1.8V	Bank67 IO11 differential negative. Same pin can be configured as GC Global Clock differential negative or Single ended I/O.

**IO Type of IOs originating from KU19P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx KU19P FPGA datasheet.*

2.8.3 Power & Reset Input

The Kintex Ultrascale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (pin232) in Board-to-Board Connector1. Also, in Board-to-Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Kintex Ultrascale+ FPGA SOM supports VRTC_3V0 coin cell power input from Board-to-Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,14, 15, 16, 17, 18, 19, 20	VCC_5V	NA	NA	NA	I, 5V Power	Supply Voltage.
21, 23, 37, 43, 49, 55, 73, 107, 113, 119, 129, 167, 173, 179, 185, 191, 197, 203, 209, 215, 221, 227, 233, 239, 22, 24, 30, 74, 108, 114, 120, 130, 168, 174, 180, 186, 192, 198, 204, 210, 216, 222, 228, 234, 240	GND	NA	NA	NA	Power	Ground.
68	VRTC_3V0	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.

2.9 Board to Board Connector3

The Kintex Ultrascale+ FPGA SOM Board to Board connector3 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector3 are explained in the following sections. The Board-to-Board Connector3 (J5) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A from Samtech

Staking Height - 5mm

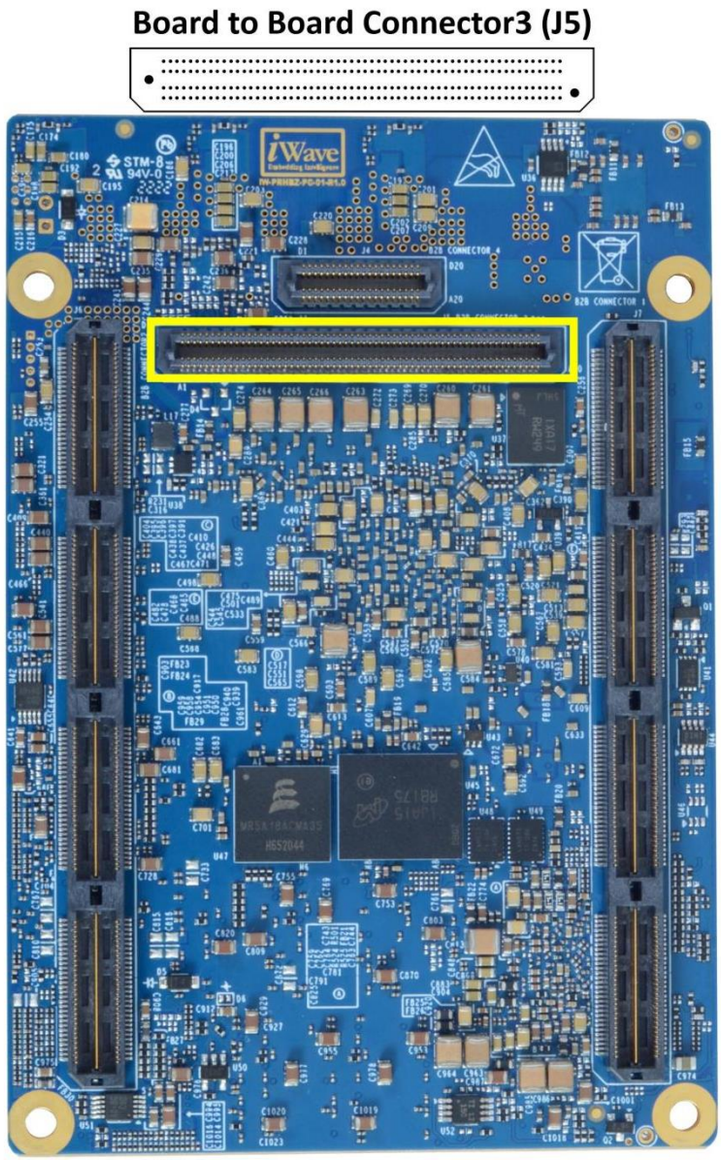


Figure 7: Board to Board Connector3

Table 5: Board to Board Connector3 Pinout

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A1	GTREFCLK1N_232	**B1**	GND	**C1**	NC	**D1**	GND
A2	GTREFCLK1P_232	**B2**	GTYRXN2_230	**C2**	GND	**D2**	B2B_GTREFCLK0P_228
A3	GND	**B3**	GTYRXP2_230	**C3**	GND	**D3**	B2B_GTREFCLK0N_228
A4	GTYRXN0_230	**B4**	GND	**C4**	GTYRXP2_231	**D4**	GND
A5	GTYRXP0_230	**B5**	GND	**C5**	GTYRXN2_231	**D5**	GND
A6	GND	**B6**	GTYRXN3_230	**C6**	GND	**D6**	B2B_GTYRXP3_228
A7	GND	**B7**	GTYRXP3_230	**C7**	GND	**D7**	B2B_GTYRXN3_228
A8	GTYRXN1_230	**B8**	GND	**C8**	GTYRXN0_231	**D8**	GND
A9	GTYRXP1_230	**B9**	GND	**C9**	GTYRXP0_231	**D9**	GND
A10	GND	**B10**	GTYTXN1_230	**C10**	GND	**D10**	GTYRXP2_228
A11	GND	**B11**	GTYTXP1_230	**C11**	GND	**D11**	GTYRXN2_228
A12	GTYTXN3_230	**B12**	GND	**C12**	GTYTXN1_231	**D12**	GND
A13	GTYTXP3_230	**B13**	GND	**C13**	GTYTXP1_231	**D13**	GND
A14	GND	**B14**	GTYTXN0_230	**C14**	GND	**D14**	GTYRXP1_228
A15	GND	**B15**	GTYTXP0_230	**C15**	GND	**D15**	GTYRXN1_228
A16	GTYTXN2_230	**B16**	GND	**C16**	GTREFCLK1N_231	**D16**	GND
A17	GTYTXP2_230	**B17**	GND	**C17**	GTREFCLK1P_231	**D17**	GND
A18	GND	**B18**	GTREFCLK0N_230	**C18**	GND	**D18**	GTYRXP0_228
A19	GND	**B19**	GTREFCLK0P_230	**C19**	GND	**D19**	GTYRXN0_228
A20	GTREFCLK1N_230	**B20**	GND	**C20**	GTREFCLK0P_231	**D20**	GND
A21	GTREFCLK1P_230	**B21**	GND	**C21**	GTREFCLK0N_231	**D21**	GND
A22	GND	**B22**	GTYRXN3_229	**C22**	GND	**D22**	B2B_GTYTXN3_228
A23	GND	**B23**	GTYRXP3_229	**C23**	GND	**D23**	B2B_GTYTXP3_228

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A24	GTYRXN2_229	**B24**	GND	**C24**	GTYRXN3_231	**D24**	GND
A25	GTYRXP2_229	**B25**	GND	**C25**	GTYRXP3_231	**D25**	GND
A26	GND	**B26**	GTYTXP3_229	**C26**	GND	**D26**	GTYTXN2_228
A27	GND	**B27**	GTYTXN3_229	**C27**	GND	**D27**	GTYTXP2_228
A28	GTYTXP2_229	**B28**	GND	**C28**	GTYRXN1_231	**D28**	GND
A29	GTYTXN2_229	**B29**	GND	**C29**	GTYRXP1_231	**D29**	GND
A30	GND	**B30**	GTYTXP1_229	**C30**	GND	**D30**	GTYTXN1_228
A31	GND	**B31**	GTYTXN1_229	**C31**	GND	**D31**	GTYTXP1_228
A32	GTYTXP0_229	**B32**	GND	**C32**	GTYTXN3_231	**D32**	GND
A33	GTYTXN0_229	**B33**	GND	**C33**	GTYTXP3_231	**D33**	GND
A34	GND	**B34**	GTREFCLK1P_229	**C34**	GND	**D34**	GTYTXN0_228
A35	GND	**B35**	GTREFCLK1N_229	**C35**	GND	**D35**	GTYTXP0_228
A36	GTYRXP1_229	**B36**	GND	**C36**	GTYTXN2_231	**D36**	GND
A37	GTYRXN1_229	**B37**	GND	**C37**	GTYTXP2_231	**D37**	GND
A38	GND	**B38**	GTREFCLK0P_229	**C38**	GND	**D38**	GTREFCLK1N_228
A39	GND	**B39**	GTREFCLK0N_229	**C39**	GND	**D39**	GTREFCLK1P_228
A40	GTYRXP0_229	**B40**	GND	**C40**	GTYTXN0_231	**D40**	GND
A41	GTYRXN0_229	**B41**	GND	**C41**	GTYTXP0_231	**D41**	GND
A42	GND	**B42**	NC	**C42**	GND	**D42**	GTYRXN1_232
A43	GND	**B43**	NC	**C43**	GND	**D43**	GTYRXP1_232
A44	NC	**B44**	GND	**C44**	GTYRXN2_232	**D44**	GND
A45	NC	**B45**	GND	**C45**	GTYRXP2_232	**D45**	GND
A46	GND	**B46**	NC	**C46**	GND	**D46**	GTYRXN3_232
A47	GND	**B47**	NC	**C47**	GND	**D47**	GTYRXP3_232
A48	NC	**B48**	GND	**C48**	GTREFCLK0P_232	**D48**	GND

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A49	NC	**B49**	GND	**C49**	GTREFCLK0N_232	**D49**	GND
A50	GND	**B50**	NC	**C50**	GND	**D50**	GTYRXN0_232
A51	GND	**B51**	NC	**C51**	GND	**D51**	GTYRXP0_232
A52	NC	**B52**	GND	**C52**	GTYTXP0_232	**D52**	GND
A53	NC	**B53**	GND	**C53**	GTYTXN0_232	**D53**	GND
A54	GND	**B54**	NC	**C54**	GND	**D54**	GTYTXP2_232
A55	GND	**B55**	NC	**C55**	GND	**D55**	GTYTXN2_232
A56	NC	**B56**	GND	**C56**	GTYTXN1_232	**D56**	GND
A57	NC	**B57**	GND	**C57**	GTYTXP1_232	**D57**	GND
A58	GND	**B58**	NC	**C58**	GND	**D58**	GTYTXP3_232
A59	NC	**B59**	NC	**C59**	GND	**D59**	GTYTXN3_232
A60	NC	**B60**	GND	**C60**	NC	**D60**	GND

2.9.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector3 from Kintex Ultrascale+ FPGA's PL is explained in the following section.

2.9.1.1 GTY High Speed Transceivers

The Kintex Ultrascale+ FPGA (KU19P) supports 20 GTY transceivers through Four transceiver Quad (Bank 228, 229, 230, 231 & 232) with line rate from 500Mbps to 32.75Gbps based on the speed grade of the FPGA. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

In Kintex Ultrascale+ FPGA SOM, on board reference clock to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required peripheral standards on GTY transceivers. Also, On board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommend.

For more details on GTY transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
Bank228 Transceiver Quad Pins						
D2	B2B_GTREFCLK0P_228*	MGTREFCLK0P_228	228	AH11	I, DIFF	GTY Bank228 channel0 High speed differential reference clock0 positive.
D3	B2B_GTREFCLK0N_228*	MGTREFCLK0N_228	228	AH10	I, DIFF	GTY Bank228 channel0 High speed differential reference clock0 negative.
D6	B2B_GTYRXP3_228*	MGTYRXP3_228	228	AF2	I, DIFF	GTY Bank228 channel3 High speed differential receiver positive.
D7	B2B_GTYRXN3_228*	MGTYRXN3_228	228	AF1	I, DIFF	GTY Bank228 channel3 High speed differential receiver negative.
D10	GTYRXP2_228	MGTYRXP2_228	228	AG4	I, DIFF	GTY Bank228 channel2 High speed differential receiver positive.
D11	GTYRXN2_228	MGTYRXN2_228	228	AG3	I, DIFF	GTY Bank228 channel2 High speed differential receiver negative.
D14	GTYRXP1_228	MGTYRXP1_228	228	AH2	I, DIFF	GTY Bank228 channel1 High speed differential receiver positive.
D15	GTYRXN1_228	MGTYRXN1_228	228	AH1	I, DIFF	GTY Bank228 channel1 High speed differential receiver negative.
D18	GTYRXP0_228	MGTYRXP0_228	228	AJ4	I, DIFF	GTY Bank228 channel0 High speed differential receiver positive.
D19	GTYRXN0_228	MGTYRXN0_228	228	AJ3	I, DIFF	GTY Bank228 channel0 High speed differential receiver negative.
D22	B2B_GTYTXN3_228*	MGTYTXN3_228	228	AF6	O, DIFF	GTY Bank228 channel3 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
D23	B2B_GTYTXP3_228*	MGTYTXP3_228	228	AF7	O, DIFF	GTY Bank228 channel3 High speed differential transmitter positive.
D26	GTYTXN2_228	MGTYTXN2_228	228	AG8	O, DIFF	GTY Bank228 channel2 High speed differential transmitter negative.
D27	GTYTXP2_228	MGTYTXP2_228	228	AG9	O, DIFF	GTY Bank228 channel2 High speed differential transmitter positive.
D30	GTYTXN1_228	MGTYTXN1_228	228	AH6	O, DIFF	GTY Bank228 channel1 High speed differential transmitter negative.
D31	GTYTXP1_228	MGTYTXP1_228	228	AH7	O, DIFF	GTY Bank228 channel1 High speed differential transmitter positive.
D34	GTYTXN0_228	MGTYTXN0_228	228	AJ8	O, DIFF	GTY Bank228 channel0 High speed differential transmitter negative.
D35	GTYTXP0_228	MGTYTXP0_228	228	AJ9	O, DIFF	GTY Bank228 channel0 High speed differential transmitter positive.
D38	GTREFCLK1N_228	MGTREFCLK1N_228	228	AF10	I, DIFF	GTY Bank228 channel1 High speed differential reference clock1 negative.
D39	GTREFCLK1P_228	MGTREFCLK1P_228	228	AF11	I, DIFF	GTY Bank228 channel1 High speed differential reference clock1 positive.
Bank229 Transceiver Quad Pins						
A24	GTYRXN2_229	MGTYRXN2_229	229	W3	I, DIFF	GTY Bank229 channel2 High speed differential receiver negative.
A25	GTYRXP2_229	MGTYRXP2_229	229	W4	I, DIFF	GTY Bank229 channel2 High speed differential receiver positive.
A28	GTYTXP2_229	MGTYTXP2_229	229	W9	O, DIFF	GTY Bank229 channel2 High speed differential transmitter positive.
A29	GTYTXN2_229	MGTYTXN2_229	229	W8	O, DIFF	GTY Bank229 channel2 High speed differential transmitter negative.
A32	GTYTXP0_229	MGTYTXP0_229	229	AA9	O, DIFF	GTY Bank229 channel0 High speed differential transmitter positive.
A33	GTYTXN0_229	MGTYTXN0_229	229	AA8	O, DIFF	GTY Bank229 channel0 High speed differential transmitter negative.
A36	GTYRXP1_229	MGTYRXP1_229	229	Y2	I, DIFF	GTY Bank229 channel1 High speed differential receiver positive.
A37	GTYRXN1_229	MGTYRXN1_229	229	Y1	I, DIFF	GTY Bank229 channel1 High speed differential receiver negative.
A40	GTYRXP0_229	MGTYRXP0_229	229	AA4	I, DIFF	GTY Bank229 channel0 High speed differential receiver positive.
A41	GTYRXN0_229	MGTYRXN0_229	229	AA3	I, DIFF	GTY Bank229 channel0 High speed differential receiver negative.
B22	GTYRXN3_229	MGTYRXN3_229	229	V1	I, DIFF	GTY Bank229 channel3 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
B23	GTYRXP3_229	MGTYRXP3_229	229	V2	I, DIFF	GTY Bank229 channel3 High speed differential receiver positive.
B26	GTYTXP3_229	MGTYTXP3_229	229	V7	O, DIFF	GTY Bank229 channel3 High speed differential transmitter positive.
B27	GTYTXN3_229	MGTYTXN3_229	229	V6	O, DIFF	GTY Bank229 channel3 High speed differential transmitter negative.
B30	GTYTXP1_229	MGTYTXP1_229	229	Y7	O, DIFF	GTY Bank229 channel1 High speed differential transmitter positive.
B31	GTYTXN1_229	MGTYTXN1_229	229	Y6	O, DIFF	GTY Bank229 channel1 High speed differential transmitter negative.
B34	GTREFCLK1P_229	MGTREFCLK1P_229	229	V11	I, DIFF	GTY Bank229 channel1 High speed differential reference clock1 positive.
B35	GTREFCLK1N_229	MGTREFCLK1N_229	229	V10	I, DIFF	GTY Bank229 channel1 High speed differential reference clock1 negative.
B38	GTREFCLK0P_229	MGTREFCLK0P_229	229	Y11	I, DIFF	GTY Bank229 channel0 High speed differential reference clock0 positive.
B39	GTREFCLK0N_229	MGTREFCLK0N_229	229	Y10	I, DIFF	GTY Bank229 channel0 High speed differential reference clock0 negative.
Bank230 Transceiver Quad Pins						
A4	GTYRXN0_230	MGTYRXN0_230	230	U3	I, DIFF	GTY Bank230 channel0 High speed differential receiver negative.
A5	GTYRXP0_230	MGTYRXP0_230	230	U4	I, DIFF	GTY Bank230 channel0 High speed differential receiver positive.
A8	GTYRXN1_230	MGTYRXN1_230	230	T1	I, DIFF	GTY Bank230 channel1 High speed differential receiver negative.
A9	GTYRXP1_230	MGTYRXP1_230	230	T2	I, DIFF	GTY Bank230 channel1 High speed differential receiver positive.
A12	GTYTXN3_230	MGTYTXN3_230	230	P6	O, DIFF	GTY Bank230 channel3 High speed differential transmitter negative.
A13	GTYTXP3_230	MGTYTXP3_230	230	P7	O, DIFF	GTY Bank230 channel3 High speed differential transmitter positive.
A16	GTYTXN2_230	MGTYTXN2_230	230	R8	O, DIFF	GTY Bank230 channel2 High speed differential transmitter negative.
A17	GTYTXP2_230	MGTYTXP2_230	230	R9	O, DIFF	GTY Bank230 channel2 High speed differential transmitter positive.
A20	GTREFCLK1N_230	MGTREFCLK1N_230	230	P10	I, DIFF	GTY Bank230 channel1 High speed differential reference clock1 negative.
A21	GTREFCLK1P_230	MGTREFCLK1P_230	230	P11	I, DIFF	GTY Bank230 channel1 High speed differential reference clock1 positive.
B2	GTYRXN2_230	MGTYRXN2_230	230	R3	I, DIFF	GTY Bank230 channel2 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
B3	GTYRXP2_230	MGTYRXP2_230	230	R4	I, DIFF	GTY Bank230 channel2 High speed differential receiver positive.
B6	GTYRXN3_230	MGTYRXN3_230	230	P1	I, DIFF	GTY Bank230 channel3 High speed differential receiver negative.
B7	GTYRXP3_230	MGTYRXP3_230	230	P2	I, DIFF	GTY Bank230 channel3 High speed differential receiver positive.
B10	GTYTXN1_230	MGTYTXN1_230	230	T6	O, DIFF	GTY Bank230 channel1 High speed differential transmitter negative.
B11	GTYTXP1_230	MGTYTXP1_230	230	T7	O, DIFF	GTY Bank230 channel1 High speed differential transmitter positive.
B14	GTYTXN0_230	MGTYTXN0_230	230	U8	O, DIFF	GTY Bank230 channel0 High speed differential transmitter negative.
B15	GTYTXP0_230	MGTYTXP0_230	230	U9	O, DIFF	GTY Bank230 channel0 High speed differential transmitter positive.
B18	GTREFCLK0N_230	MGTREFCLK0N_230	230	T10	I, DIFF	GTY Bank230 channel0 High speed differential reference clock0 negative.
B19	GTREFCLK0P_230	MGTREFCLK0P_230	230	T11	I, DIFF	GTY Bank230 channel0 High speed differential reference clock0 positive.
Bank231 Transceiver Quad Pins						
C4	GTYRXP2_231	MGTYRXP2_231	231	L4	I, DIFF	GTY Bank231 channel2 High speed differential receiver positive.
C5	GTYRXN2_231	MGTYRXN2_231	231	L3	I, DIFF	GTY Bank231 channel2 High speed differential receiver negative.
C8	GTYRXN0_231	MGTYRXN0_231	231	N3	I, DIFF	GTY Bank231 channel0 High speed differential receiver negative.
C9	GTYRXP0_231	MGTYRXP0_231	231	N4	I, DIFF	GTY Bank231 channel0 High speed differential receiver positive.
C12	GTYTXN1_231	MGTYTXN1_231	231	M6	O, DIFF	GTY Bank231 channel1 High speed differential transmitter negative.
C13	GTYTXP1_231	MGTYTXP1_231	231	M7	O, DIFF	GTY Bank231 channel1 High speed differential transmitter positive.
C16	GTREFCLK1N_231	MGTREFCLK1N_231	231	K10	I, DIFF	GTY Bank231 channel1 High speed differential reference clock1 negative.
C17	GTREFCLK1P_231	MGTREFCLK1P_231	231	K11	I, DIFF	GTY Bank231 channel1 High speed differential reference clock1 positive.
C20	GTREFCLK0P_231	MGTREFCLK0P_231	231	M11	I, DIFF	GTY Bank231 channel0 High speed differential reference clock0 positive.
C21	GTREFCLK0N_231	MGTREFCLK0N_231	231	M10	I, DIFF	GTY Bank231 channel0 High speed differential reference clock0 negative.
C24	GTYRXN3_231	MGTYRXN3_231	231	K1	I, DIFF	GTY Bank231 channel3 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
C25	GTYRXP3_231	MGTYRXP3_231	231	K2	I, DIFF	GTY Bank231 channel3 High speed differential receiver positive.
C28	GTYRXN1_231	MGTYRXN1_231	231	M1	I, DIFF	GTY Bank231 channel1 High speed differential receiver negative.
C29	GTYRXP1_231	MGTYRXP1_231	231	M2	I, DIFF	GTY Bank231 channel1 High speed differential receiver positive.
C32	GTYTXN3_231	MGTYTXN3_231	231	K6	O, DIFF	GTY Bank231 channel3 High speed differential receiver negative.
C33	GTYTXP3_231	MGTYTXP3_231	231	K7	O, DIFF	GTY Bank231 channel3 High speed differential receiver positive.
C36	GTYTXN2_231	MGTYTXN2_231	231	L8	O, DIFF	GTY Bank231 channel2 High speed differential receiver negative.
C37	GTYTXP2_231	MGTYTXP2_231	231	L9	O, DIFF	GTY Bank231 channel2 High speed differential receiver positive.
C40	GTYTXN0_231	MGTYTXN0_231	231	N8	O, DIFF	GTY Bank231 channel0 High speed differential receiver negative.
C41	GTYTXP0_231	MGTYTXP0_231	231	N9	O, DIFF	GTY Bank231 channel0 High speed differential receiver positive.
Bank232 Transceiver Quad Pins						
A1	GTREFCLK1N_232	MGTREFCLK1N_232	232	F10	I, DIFF	GTY Bank232 channel1 High speed differential reference clock1 negative.
A2	GTREFCLK1P_232	MGTREFCLK1P_232	232	F11	I, DIFF	GTY Bank232 channel1 High speed differential reference clock1 positive.
C44	GTYRXN2_232	MGTYRXN2_232	232	G3	I, DIFF	GTY Bank232 channel2 High speed differential receiver negative.
C45	GTYRXP2_232	MGTYRXP2_232	232	G4	I, DIFF	GTY Bank232 channel2 High speed differential receiver positive.
C48	GTREFCLK0P_232	MGTREFCLK0P_232	232	H11	I, DIFF	GTY Bank232 channel0 High speed differential reference clock0 positive.
C49	GTREFCLK0N_232	MGTREFCLK0N_232	232	H10	I, DIFF	GTY Bank232 channel0 High speed differential reference clock0 negative.
C52	GTYTXP0_232	MGTYTXP0_232	232	J9	O, DIFF	GTY Bank232 channel0 High speed differential transmitter positive.
C53	GTYTXN0_232	MGTYTXN0_232	232	J8	O, DIFF	GTY Bank232 channel0 High speed differential transmitter negative.
C56	GTYTXN1_232	MGTYTXN1_232	232	H6	O, DIFF	GTY Bank232 channel1 High speed differential transmitter negative.
C57	GTYTXP1_232	MGTYTXP1_232	232	H7	O, DIFF	GTY Bank232 channel1 High speed differential transmitter positive.
D42	GTYRXN1_232	MGTYRXN1_232	232	H1	I, DIFF	GTY Bank232 channel1 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
D43	GTYRXP1_232	MGTYRXP1_232	232	H2	I, DIFF	GTY Bank232 channel1 High speed differential receiver positive.
D46	GTYRXN3_232	MGTYRXN3_232	232	F1	I, DIFF	GTY Bank232 channel3 High speed differential receiver negative.
D47	GTYRXP3_232	MGTYRXP3_232	232	F2	I, DIFF	GTY Bank232 channel3 High speed differential receiver positive.
D50	GTYRXN0_232	MGTYRXN0_232	232	J3	I, DIFF	GTY Bank232 channel0 High speed differential receiver negative.
D51	GTYRXP0_232	MGTYRXP0_232	232	J4	I, DIFF	GTY Bank232 channel0 High speed differential receiver positive.
D54	GTYTXP2_232	MGTYTXP2_232	232	G9	O, DIFF	GTY Bank232 channel2 High speed differential transmitter positive.
D55	GTYTXN2_232	MGTYTXN2_232	232	G8	O, DIFF	GTY Bank232 channel2 High speed differential transmitter negative.
D58	GTYTXP3_232	MGTYTXP3_232	232	F7	O, DIFF	GTY Bank232 channel3 High speed differential transmitter positive.
D59	GTYTXN3_232	MGTYTXN3_232	232	F6	O, DIFF	GTY Bank232 channel3 High speed differential transmitter negative.

*One GTY transceiver link is connected with on-SOM PCIe transceiver.

2.9.2 Power

The Kintex Ultrascale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector3, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
A3, A6, A7, A10, A11, A14, A15, A18, A19, A22, A23, A26, A27, A30, A31, A34, A35, A38, A39, A42, A43, A46, A47, A50, A51, A54, A55, A58, B1, B4, B5, B8, B9, B12, B13, B16, B17, B20, B21, B24, B25, B28, B29, B32, B33, B36, B37, B40, B41, B44, B45, B48, B49, B52, B53, B56, B57, B60, C2, C3, C6, C7, C10, C11, C14, C15, C18, C19, C22, C23, C26, C27, C30, C31, C34, C35, C38, C39, C42, C43, C46, C47, C50, C51, C54, C55, C58, C59, D1, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, D24, D25, D28, D29, D32, D33, D36, D37, D40, D41, D44, D45, D48, D49, D52, D53, D56, D57, D60,	GND	NA	NA	NA	Power	Ground.

2.10 Board to Board Connector4

The Kintex Ultrascale+ FPGA SOM Board to Board connector4 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector4 are explained in the following sections. The Board-to-Board Connector4 (J4) is physically located on bottom side of the SOM as shown below.

Number of Pins - 80

Connector Part Number - ADM6-20-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-20-03.5-L-4-2-A from Samtech

Staking Height - 5mm

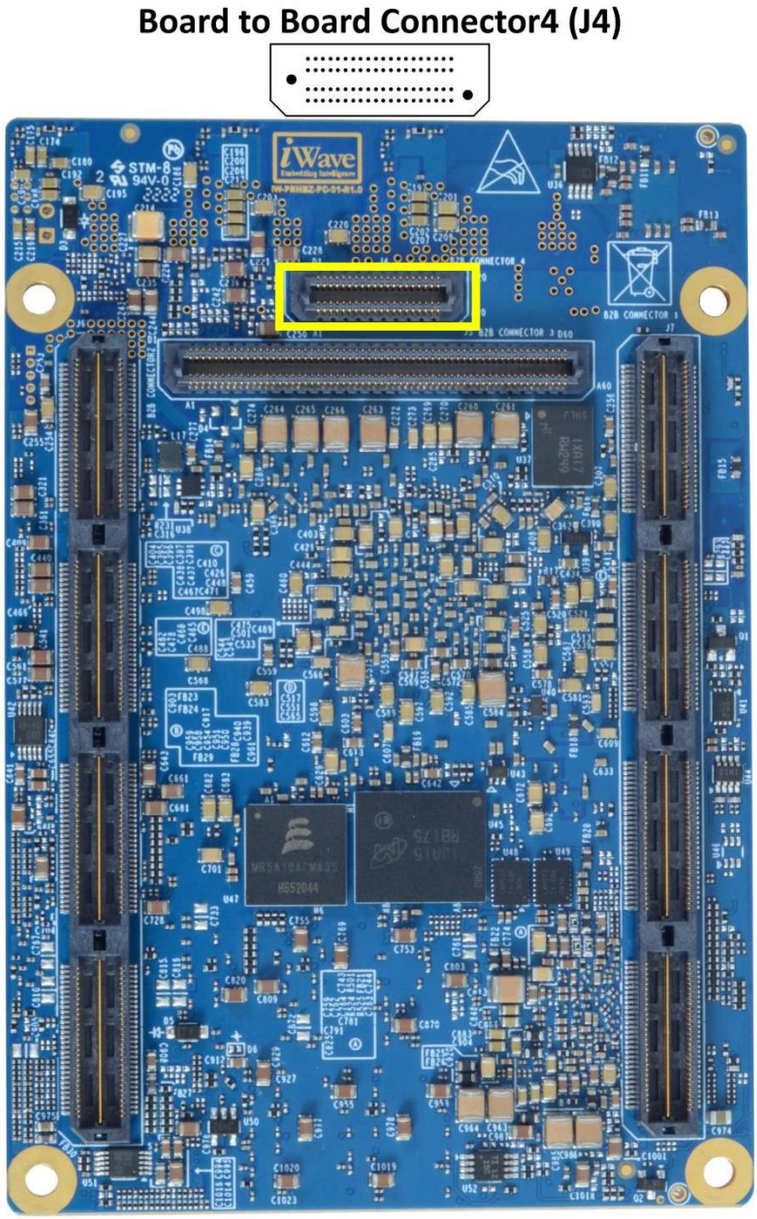


Figure 8: Board to Board Connector4

Table 6: Board to Board Connector4 Pinout

B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name
A1	GND	**B1**	GTREFCLK1N_227	**C1**	GND	**D1**	NC
A2	GTYRXN1_227	**B2**	GTREFCLK1P_227	**C2**	NC	**D2**	GND
A3	GTYRXP1_227	**B3**	GND	**C3**	NC	**D3**	GND
A4	GND	**B4**	GTYRXN3_227	**C4**	GND	**D4**	NC
A5	GND	**B5**	GTYRXP3_227	**C5**	GND	**D5**	NC
A6	GTREFCLK0P_227	**B6**	GND	**C6**	NC	**D6**	GND
A7	GTREFCLK0N_227	**B7**	GND	**C7**	NC	**D7**	GND
A8	GND	**B8**	GTYRXN2_227	**C8**	GND	**D8**	NC
A9	GND	**B9**	GTYRXP2_227	**C9**	GND	**D9**	NC
A10	GTYTXP0_227	**B10**	GND	**C10**	NC	**D10**	GND
A11	GTYTXN0_227	**B11**	GND	**C11**	NC	**D11**	GND
A12	GND	**B12**	GTYTXP3_227	**C12**	GND	**D12**	NC
A13	GND	**B13**	GTYTXN3_227	**C13**	GND	**D13**	NC
A14	GTYTXP1_227	**B14**	GND	**C14**	NC	**D14**	GND
A15	GTYTXN1_227	**B15**	GND	**C15**	NC	**D15**	GND
A16	GND	**B16**	GTYRXN0_227	**C16**	GND	**D16**	NC
A17	GND	**B17**	GTYRXP0_227	**C17**	GND	**D17**	NC
A18	GTYTXP2_227	**B18**	GND	**C18**	NC	**D18**	GND
A19	GTYTXN2_227	**B19**	GND	**C19**	NC	**D19**	NC
A20	GND	**B20**	NC	**C20**	GND	**D20**	NC

2.10.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector4 from Kintex Ultrascale+ FPGA's PL is explained in the following section.

2.10.1.1 GTY High Speed Transceivers

The Kintex Ultrascale+ FPGA SOM Supports 4 GTY transceivers along with reference clock inputs from Bank227 on Board-to-Board Connector4.

For more details on GTY transceiver pinouts on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector4 Signal Name	FPGA Pin Name	FPGA Pin Name	FPGA Pin Name	Signal Type/ Termination	Description
Bank227 Transceiver Quad Pins						
A2	GTYRXN1_227	MGTYRXN1_227	227	AM1	I, DIFF	GTY Bank227 channel1 High speed differential receiver negative.
A3	GTYRXP1_227	MGTYRXN1_228	227	AH1	I, DIFF	GTY Bank227 channel1 High speed differential receiver positive.
A6	GTREFCLK0P_227	MGTREFCLK0P_227	227	AM11	I, DIFF	GTY Bank227 channel0 High speed differential reference clock0 positive.
A7	GTREFCLK0N_227	MGTREFCLK0N_227	227	AM10	I, DIFF	GTY Bank227 channel0 High speed differential reference clock0 negative.
A10	GTYTXP0_227	MGTYTXP0_227	227	AN9	O, DIFF	GTY Bank227 channel0 High speed differential transmitter positive.
A11	GTYTXN0_227	MGTYTXN0_227	227	AN8	O, DIFF	GTY Bank227 channel0 High speed differential transmitter negative.
A14	GTYTXP1_227	MGTYTXP1_227	227	AM7	O, DIFF	GTY Bank227 channel1 High speed differential transmitter positive.
A15	GTYTXN1_227	MGTYTXN1_227	227	AM6	O, DIFF	GTY Bank227 channel1 High speed differential transmitter negative.
A18	GTYTXP2_227	MGTYTXP2_227	227	AL9	O, DIFF	GTY Bank227 channel2 High speed differential transmitter positive.
A19	GTYTXN2_227	MGTYTXN2_227	227	AL8	O, DIFF	GTY Bank227 channel2 High speed differential transmitter negative.
B1	GTREFCLK1N_227	MGTREFCLK1N_227	227	AK10	I, DIFF	GTY Bank227 channel1 High speed differential reference clock1 positive.
B2	GTREFCLK1P_227	MGTREFCLK1P_227	227	AK11	I, DIFF	GTY Bank227 channel1 High speed differential reference clock1 positive.
B4	GTYRXN3_227	MGTYRXN3_227	227	AK1	I, DIFF	GTY Bank227 channel3 High speed differential receiver negative.
B5	GTYRXP3_227	MGTYRXP3_227	227	AK2	I, DIFF	GTY Bank227 channel3 High speed differential receiver positive.

B2B-4 Pin No	B2B Connector4 Signal Name	FPGA Pin Name	FPGA Pin Name	FPGA Pin Name	Signal Type/ Termination	Description
B8	GTYRXN2_227	MGTYRXN2_227	227	AL3	I, DIFF	GTY Bank227 channel2 High speed differential receiver negative.
B9	GTYRXP2_227	MGTYRXP2_227	227	AL4	O, DIFF	GTY Bank227 channel2 High speed differential receiver positive.
B12	GTYTXP3_227	MGTYTXP3_227	227	AK7	O, DIFF	GTY Bank227 channel3 High speed differential transmitter positive.
B13	GTYTXN3_227	MGTYTXN3_227	227	AK6	O, DIFF	GTY Bank227 channel3 High speed differential transmitter negative.
B16	GTYRXN0_227	MGTYRXN0_227	227	AN3	I, DIFF	GTY Bank227 channel0 High speed differential transmitter negative.
B17	GTYRXP0_227	MGTYRXP0_227	227	AN4	I, DIFF	GTY Bank227 channel0 High speed differential transmitter positive.

2.10.2 Power

The Kintex Ultrascale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector4, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector4 Pin Name	FPGA Pin Name	FPGA Pin Name	FPGA Pin Name	Signal Type/ Termination	Description
A1, A4, A5, A8, A9, A12, A13, A16, A17, A20, B3, B6, B7, B10, B11, B14, B15, B18, B19, C1, C4, C5, C8, C9, C12, C13, C16, C17, C20, D2, D3, D6, D7, D10, D11, D14, D15, D18,	GND	NA	NA	NA	Power	Ground.

2.11 LS1021A Processor Pin Multiplexing on Board-to-Board Connectors

The Kintex Ultrascale+ FPGA SOM's LS1021A Processor IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of IO pins can be configured as GPIO if required. The below table provides the details of LS1021A processor's pin connections on Kintex Ultrascale+ FPGA (KU19P) SOM with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring LS1021A Datasheet. To know the complete available alternate functions, refer the LS1021A latest datasheet.

Table 7: LS1021A IOMUX on Kintex Ultrascale+ FPGA SOM

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
Integrated Flash Controller	NA	IFC_A16/QSPI_CS_A0	IFC_A16	QSPI_CS_A0						
	NA	IFC_A17/QSPI_CS_A1	IFC_A17	QSPI_CS_A1						
	NA	IFC_A18/QSPI_CK_A	IFC_A18	QSPI_CK_A						
	NA	IFC_A19/QSPI_CS_B0	IFC_A19	QSPI_CS_B0						
	NA	IFC_A20/QSPI_CS_B1	IFC_A20	QSPI_CS_B1						
	NA	IFC_A21/QSPI_CK_B/cfg_dram_type	IFC_A21	QSPI_CK_B	cfg_dram_type					
	NA	IFC_A22/QSPI_DIO_A0/IFC_WP1_B	IFC_A22	QSPI_DIO_A0		IFC_WP1_B				
	NA	IFC_A23/QSPI_DIO_A1/IFC_WP2_B	IFC_A23	QSPI_DIO_A1		IFC_WP2_B				
	NA	IFC_A24/QSPI_DIO_A2/IFC_WP3_B	IFC_A24	QSPI_DIO_A2		IFC_WP3_B				
	NA	IFC_A25/GPIO2_25/QSPI_DIO_A3/FTM5_CH0/IFC_RB2_B/IFC_CS4_B	IFC_A25	QSPI_DIO_A3	IFC_RB2_B	IFC_CS4_B	FTM5_CH0			
	NA	IFC_A26/GPIO2_26/FTM5_CH1/IFC_RB3_B/IFC_CS5_B	IFC_A26	GPIO2_26	IFC_RB3_B	IFC_CS5_B	FTM5_CH1			
	NA	IFC_A27/GPIO2_27/FTM5_EXTCLK/IFC_CS6_B	IFC_A27	GPIO2_27		IFC_CS6_B	FTM5_EXTCLK			
	NA	IFC_AD00/cfg_gpinput0	IFC_AD00		cfg_gpinput0					
	NA	IFC_AD01/cfg_gpinput1	IFC_AD01		cfg_gpinput1					
	NA	IFC_AD02/cfg_gpinput2	IFC_AD02		cfg_gpinput2					
	NA	IFC_AD03/cfg_gpinput3	IFC_AD03		cfg_gpinput3					
	NA	IFC_AD04/cfg_gpinput4	IFC_AD04		cfg_gpinput4					
	NA	IFC_AD05/cfg_gpinput5	IFC_AD05		cfg_gpinput5					
	NA	IFC_AD06/cfg_gpinput6	IFC_AD06		cfg_gpinput6					

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	IFC_AD07/cfg_gpinput7	IFC_AD07		cfg_gpinput7					
	NA	IFC_AD08/cfg_rcw_src0/SPI1_PCS1	IFC_AD08	SPI1_PCS1	cfg_rcw_src0					
	NA	IFC_AD09/cfg_rcw_src1/SPI1_PCS2	IFC_AD09	SPI1_PCS2	cfg_rcw_src1					
	NA	IFC_AD10/cfg_rcw_src2/SPI1_PCS3	IFC_AD10	SPI1_PCS3	cfg_rcw_src2					
	NA	IFC_AD11/cfg_rcw_src3/SPI1_PCS4	IFC_AD11	SPI1_PCS4	cfg_rcw_src3					
	NA	IFC_AD12/cfg_rcw_src4/SPI1_PCS5	IFC_AD12	SPI1_PCS5	cfg_rcw_src4					
	NA	IFC_AD13/cfg_rcw_src5/SPI1_SOUT	IFC_AD13	SPI1_SOUT	cfg_rcw_src5					
	NA	IFC_AD14/cfg_rcw_src6	IFC_AD14		cfg_rcw_src6					
	NA	IFC_AD15/cfg_rcw_src7	IFC_AD15		cfg_rcw_src7					
	NA	IFC_AVD	IFC_AVD							
	NA	IFC_BCTL	IFC_BCTL							
	NA	IFC_CLE/cfg_rcw_src8	IFC_CLE		cfg_rcw_src8					
	NA	IFC_CLK0	IFC_CLK0							
	NA	IFC_CLK1	IFC_CLK1							
	NA	IFC_CS0_B	IFC_CS0_B							
	NA	IFC_CS1_B/GPIO2_10/SPI1_PCS0/FTM7_CH0	IFC_CS1_B	GPIO2_10	SPI1_PCS0		FTM7_CH0			
	NA	IFC_CS2_B/GPIO2_11/SPI1_SCK/FTM7_CH1/ IIC3_SCL	IFC_CS2_B	GPIO2_11	SPI1_SCK		FTM7_CH1	IIC3_SCL		
	NA	IFC_CS3_B /GPIO2_12/QSPI_DIO_B3/IIC3_SDA/FTM7_EXTCLK	IFC_CS3_B	GPIO2_12	IIC3_SDA	QSPI_DIO_B3	FTM7_EXTCLK			
	NA	IFC_NDDDR_CLK	IFC_NDDDR_CLK							
	NA	IFC_NDDQS	IFC_NDDQS							
	NA	IFC_OE_B/cfg_eng_use1	IFC_OE_B		cfg_eng_use1					
	NA	IFC_PAR0/GPIO2_13/QSPI_DIO_B0/FTM6_CH0	IFC_PAR0	GPIO2_13		QSPI_DIO_B0	FTM6_CH0			

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	IFC_PAR1/GPIO2_14/QSPI_DIO_B 1/FTM6_CH1	IFC_PAR1	GPIO2_14		QSPI_DIO_B1	FTM6_CH1			
	NA	IFC_PERR_B/GPIO2_15/QSPI_DIO _B2/FTM6_EXTCLK	IFC_PERR_B	GPIO2_15		QSPI_DIO_B2	FTM6_EXTCLK			
	NA	IFC_RB0_B	IFC_RB0_B							
	NA	IFC_RB1_B/SPI1_SIN	IFC_RB1_B		SPI1_SIN					
	NA	IFC_TE/cfg_ifc_te	IFC_TE		cfg_ifc_te					
	NA	IFC_WE0_B/cfg_eng_use0	IFC_WE0_B		cfg_eng_use0					
	NA	IFC_WP0_B/cfg_eng_use2	IFC_WP0_B		cfg_eng_use2					
RGMII1	NA	EC1_GTX_CLK/GPIO3_07/ EC1_TX_CLK/ SAI2_TX_BCLK/ FTM1_EXTCLK	EC1_GTX_CLK	GPIO3_07		SAI2_TX_BCLK	EC1_TX_CLK			FTM1_EXTCLK
	NA	EC1_GTX_CLK125/ GPIO3_08/EC1_RX_ER/ EXT_AUDIO_MCLK2	EC1_GTX_CLK125	GPIO3_08	EXT_AUDIO_ MCLK2		EC1_RX_ER			
	NA	EC1_RX_CLK/GPIO3_13/ SAI1_RX_BCLK/ FTM1_QD_PHA	EC1_RX_CLK	GPIO3_13		SAI1_RX_BCLK				FTM1_QD_PHA
	NA	EC1_RX_DV/GPIO3_14/ SAI2_RX_BCLK/ FTM1_QD_PHB	EC1_RX_DV	GPIO3_14		SAI2_RX_BCLK				FTM1_QD_PHB
	NA	EC1_RXD0/GPIO3_12/ SAI2_RX_SYNC/FTM1_CH0	EC1_RXD0	GPIO3_12		SAI2_RX_SYNC				FTM1_CH0
	NA	EC1_RXD1/GPIO3_11/ SAI1_RX_SYNC/FTM1_CH1	EC1_RXD1	GPIO3_11		SAI1_RX_SYNC				FTM1_CH1
	NA	EC1_RXD2/GPIO3_10/ CAN1_RX/SAI2_RX_DATA/ FTM1_CH6	EC1_RXD2	GPIO3_10	CAN1_RX	SAI2_RX_DATA				FTM1_CH6
	NA	EC1_RXD3/GPIO3_09/ CAN2_RX/SAI1_RX_DATA/ FTM1_CH4	EC1_RXD3	GPIO3_09	CAN2_RX	SAI1_RX_DATA				FTM1_CH4
	NA	EC1_TX_EN/GPIO3_06/ SAI1_TX_BCLK/FTM1_FAULT	EC1_TX_EN	GPIO3_06		SAI1_TX_BCLK				FTM1_FAULT
	NA	EC1_TXD0/GPIO3_05/ SAI2_TX_SYNC/FTM1_CH2	EC1_TXD0	GPIO3_05		SAI2_TX_SYNC				FTM1_CH2
	NA	EC1_TXD1/GPIO3_04/ SAI1_TX_SYNC/FTM1_CH3	EC1_TXD1	GPIO3_04		SAI1_TX_SYNC				FTM1_CH3

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	EC1_TXD2/GPIO3_03/ CAN1_TX/SAI2_TX_DATA/ FTM1_CH7	EC1_TXD2	GPIO3_03	CAN1_TX	SAI2_TX_DATA				FTM1_CH7
	NA	EC1_TXD3/GPIO3_02/ CAN2_TX/SAI1_TX_DATA/ FTM1_CH5	EC1_TXD3	GPIO3_02	CAN2_TX	SAI1_TX_DATA				FTM1_CH5
RGMII3	NA	EC3_GTX_CLK/GPIO4_01/ EC2_TX_ER/FTM3_CH0/ EC3_TX_CLK	EC3_GTX_CLK	GPIO4_01			EC2_TX_ER	EC3_TX_CLK		FTM3_CH0
	NA	EC3_GTX_CLK125GPIO4_02/EC2_ COL/ USB2_DRVVBUS/ EC3_RX_ER	EC3_GTX_CLK125	GPIO4_02		USB2_DRVVBUS	EC2_COL	EC3_RX_ER		
	NA	EC3_RX_CLK/GPIO4_07/ TSEC_1588_CLK_IN/ FTM3_QD_PHA	EC3_RX_CLK	GPIO4_07					TSEC_1588_CLK_IN	FTM3_QD_PHA
	NA	EC3_RX_DV/GPIO4_08/ TSEC_1588_TRIG_IN1/ FTM3_QD_PHB	EC3_RX_DV	GPIO4_08					TSEC_1588_TRIG_IN1	FTM3_QD_PHB
	NA	EC3_RXD0/GPIO4_06/ TSEC_1588_TRIG_IN2/ EC2_CRS/FTM3_CH2	EC3_RXD0	GPIO4_06			EC2_CRS		TSEC_1588_TRIG_IN2	FTM3_CH2
	NA	EC3_RXD1/GPIO4_05/ TSEC_1588_PULSE_OUT1/ FTM3_CH3	EC3_RXD1	GPIO4_05					TSEC_1588_PULSE_OUT1	FTM3_CH3
	NA	EC3_RXD2/GPIO4_04/ EC1_COL/FTM3_EXTCLK	EC3_RXD2	GPIO4_04			EC1_COL			FTM3_EXTCLK
	NA	EC3_RXD3/GPIO4_03/ EC1_CRS/FTM3_FAULT	EC3_RXD3	GPIO4_03			EC1_CRS			FTM3_FAULT
	NA	EC3_TX_EN/GPIO4_00/ EC1_TX_ER/FTM3_CH1	EC3_TX_EN	GPIO4_00			EC1_TX_ER			FTM3_CH1
	NA	EC3_TXD0/GPIO3_31/ TSEC_1588_PULSE_OUT2/ FTM3_CH4	EC3_TXD0	GPIO3_31					TSEC_1588_PULSE_OUT2	FTM3_CH4
	NA	EC3_TXD1/GPIO3_30/ TSEC_1588_CLK_OUT/ FTM3_CH5	EC3_TXD1	GPIO3_30					TSEC_1588_CLK_OUT	FTM3_CH5
	NA	EC3_TXD2/GPIO3_29/ TSEC_1588_ALARM_OUT1/ FTM3_CH6	EC3_TXD2	GPIO3_29					TSEC_1588_ALARM_OUT1	FTM3_CH6
	NA	EC3_TXD3/GPIO3_28/ TSEC_1588_ALARM_OUT2/ FTM3_CH7	EC3_TXD3	GPIO3_28					TSEC_1588_ALARM_OUT2	FTM3_CH7

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
Ethernet Management Interface 1	212	EMI1_MDC/GPIO3_00	EMI1_MDC	GPIO3_00						
	214	EMI1_MDIO/GPIO3_01	EMI1_MDIO	GPIO3_01						
Programmable Interrupt Controller	NA	EVT9_B/GPIO2_24	EVT9_B	GPIO2_24						
	NA	IRQ0	IRQ0							
	NA	IRQ1	IRQ1							
	NA	IRQ2	IRQ2							
	NA	IRQ3/GPIO1_23	IRQ3	GPIO1_23	Ethernet INT					
	NA	IRQ4/GPIO1_24/SDHC_VS	IRQ4	GPIO1_24		SDHC_VS				
LPUART Interface	NA	SDHC_CLK/GPIO2_09/ LPUART3_CTS_B/ LPUART6_SIN	SDHC_CLK	GPIO2_09	LPUART6_SIN	LPUART3_CTS_B				
	NA	SDHC_DAT3/GPIO2_08/ LPUART3_RTS_B/ LPUART6_SOUT	SDHC_DAT3	GPIO2_08	LPUART6_SOUT	LPUART3_RTS_B				
SPI2	NA	UART1_CTS_B/GPIO1_21/ UART3_SIN/LPUART2_SIN/ SPI2_SIN/2D-ACE_VSYNC	UART1_CTS_B	GPIO1_21	LPUART2_SIN		UART3_SIN	SPI2_SIN	2D-ACE_VSYNC	
	NA	UART1_RTS_B/GPIO1_19/ UART3_SOUT/ LPUART2_SOUT/ SPI2_SOUT/2D-ACE_HSYNC	UART1_RTS_B	GPIO1_19	LPUART2_SOUT		UART3_SOUT	SPI2_SOUT	2D-ACE_HSYNC	
	NA	UART2_CTS_B/GPIO1_22/ UART4_SIN/SPI2_SCK/LPUART1_ CTS_B/ LPUART4_SIN	UART2_CTS_B	GPIO1_22	LPUART1_CTS_B	LPUART4_SIN	UART4_SIN	SPI2_SCK		
	NA	UART2_SIN/GPIO1_18/ LPUART1_SIN/SPI2_PCS1	UART2_SIN	GPIO1_18	LPUART1_SIN			SPI2_PCS1		
	NA	UART2_SOUT/GPIO1_16/ SPI2_PCS0/LPUART1_SOUT	UART2_SOUT	GPIO1_16	LPUART1_SOUT			SPI2_PCS0		
GPIO	NA	EC2_GTX_CLK/GPIO3_20/ EC2_TX_CLK/USB2_CLK/ FTM2_EXTCLK	EC2_GTX_CLK	GPIO3_20		USB2_CLK	EC2_TX_CLK			FTM2_EXTCLK
	NA	EC2_GTX_CLK125GPIO3_21/EC2_ RX_ER/ USB2_PWRFAULT	EC2_GTX_CLK125	GPIO3_21		USB2_PWRFAULT	EC2_RX_ER			
	NA	EC2_RX_CLK/GPIO3_26/ USB2_DIR/FTM2_QD_PHA	EC2_RX_CLK	GPIO3_26		USB2_DIR				FTM2_QD_PHA

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	EC2_RX_DV/GPIO3_27/ USB2_NXT/FTM2_QD_PHB	EC2_RX_DV	GPIO3_27		USB2_NXT				FTM2_QD_PHB
	NA	EC2_RXD0/GPIO3_25/ USB2_D0/FTM2_CH0	EC2_RXD0	GPIO3_25		USB2_D0				FTM2_CH0
	NA	EC2_RXD2/GPIO3_23/ CAN3_RX/USB2_D2/ FTM2_CH6	EC2_RXD2	GPIO3_23	CAN3_RX	USB2_D2				FTM2_CH6
	NA	IRQ5/GPIO1_25/ SDHC_CLK_SYNC_IN/ SPI2_PCS5	IRQ5	GPIO1_25	SPI2_PCS5	SDHC_CLK_SYNC_IN				
	NA	SDHC_DAT4/GPIO4_23/ SDHC_CLK_SYNC_OUT	SDHC_DAT4	GPIO4_23		SDHC_CLK_SYNC_OUT				
	NA	CLK10/GPIO4_20/BRGO3/ SAI3_RX_SYNC/ FTM4_QD_PHB/2D-ACE_D11	CLK10	GPIO4_20	BRGO3		SAI3_RX_SYNC	2D-ACE_D11	FTM4_QD_PHB	
	NA	CLK11/GPIO4_21/BRGO4/ SAI4_RX_SYNC/ FTM8_CH0/2D-ACE_DE	CLK11	GPIO4_21	BRGO4		SAI4_RX_SYNC	2D-ACE_DE	FTM8_CH0	
	NA	CLK12/GPIO4_22/BRGO1/ FTM8_CH1/2DACE_ CLK_OUT	CLK12	GPIO4_22	BRGO1			2D-ACE_CLK_OUT	FTM8_CH1	
	NA	TDMA_RQ/GPIO4_13/ UC1_CDB_RXER/ EXT_AUDIO_MCLK1/ FTM4_CH3/2D-ACE_D04	TDMA_RQ	GPIO4_13		UC1_CDB_RXER	EXT_AUDIO_MCLK1	2D-ACE_D04	FTM4_CH3	
	NA	TDMA_RSYNC/GPIO4_10/ UC1_CTSB_RXDV/ SAI3_TX_BCLK/ FTM4_CH6/2D-ACE_D01	TDMA_RSYNC	GPIO4_10		UC1_CTSB_RXDV	SAI3_TX_BCLK	2D-ACE_D01	FTM4_CH6	
	NA	TDMA_TXD/GPIO4_11/ UC1_TXD7/SAI3_TX_DATA/ FTM4_CH5/2D-ACE_D02	TDMA_TXD	GPIO4_11		UC1_TXD7	SAI3_TX_DATA	2D-ACE_D02	FTM4_CH5	
Board to Board Connectorr1 Interfaces from LS1021A										
GPIO	32	EC2_RXD1/GPIO3_24/ USB2_D1/FTM2_CH1	EC2_RXD1	GPIO3_24		USB2_D1				FTM2_CH1
	18	EC2_RXD3/GPIO3_22/ CAN4_RX/USB2_D3/ FTM2_CH4	EC2_RXD3	GPIO3_22	CAN4_RX	USB2_D3				FTM2_CH4
	38	EC2_TX_EN/GPIO3_19/ USB2_STP/FTM2_FAULT	EC2_TX_EN	GPIO3_19		USB2_STP				FTM2_FAULT
	28	EC2_TXD0/GPIO3_18/ USB2_D4/FTM2_CH2	EC2_TXD0	GPIO3_18		USB2_D4				FTM2_CH2

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	30	EC2_TXD1/GPIO3_17/ USB2_D5/FTM2_CH3	EC2_TXD1	GPIO3_17		USB2_D5				FTM2_CH3
	34	TDMA_RXD/GPIO4_09/ UC1_RXD7/SAI3_RX_DATA/ FTM4_CH7/2D-ACE_D00	TDMA_RXD	GPIO4_09		UC1_RXD7	SAI3_RX_DATA	2D-ACE_D00	FTM4_CH7	
Board to Board Connector2 Interfaces from LS1021A										
I2C	48	IIC1_SCL	IIC1_SCL							
	46	IIC1_SDA	IIC1_SDA							
	76	IIC2_SCL/GPIO4_27/ SDHC_CD_B/SPI2_PCS3	IIC2_SCL	GPIO4_27	SPI2_PCS3	SDHC_CD_B				
	78	IIC2_SDA/GPIO4_28/ SDHC_WP/SPI2_PCS4	IIC2_SDA	GPIO4_28	SPI2_PCS4	SDHC_WP				
LPUART	50	SDHC_CMD/GPIO2_04/ LPUART3_SOUT	SDHC_CMD	GPIO2_04	LPUART3_SOUT					
	52	SDHC_DAT0/GPIO2_05/ LPUART3_SIN	SDHC_DAT0	GPIO2_05	LPUART3_SIN					
	81	SDHC_DAT1/GPIO2_06/ LPUART2_RTS_B/ LPUART5_SOUT	SDHC_DAT1	GPIO2_06	LPUART5_SOUT	LPUART2_RTS_B				
	79	SDHC_DAT2/GPIO2_07/ LPUART2_CTS_B/ LPUART5_SIN	SDHC_DAT2	GPIO2_07	LPUART5_SIN	LPUART2_CTS_B				
Data UART	56	UART1_SIN/GPIO1_17	UART1_SIN	GPIO1_17						
	54	UART1_SOUT/GPIO1_15	UART1_SOUT	GPIO1_15						
GPIO	32	EC2_TXD2/GPIO3_16/ CAN3_TX/USB2_D6/ FTM2_CH7	EC2_TXD2	GPIO3_16	CAN3_TX	USB2_D6				FTM2_CH7
	61	EC2_TXD3/GPIO3_15/ CAN4_TX/USB2_D7/ FTM2_CH5	EC2_TXD3	GPIO3_15	CAN4_TX	USB2_D7				FTM2_CH5
	72	SDHC_DAT5/GPIO4_24/ SDHC_CMD_DIR	SDHC_DAT5	GPIO4_24		SDHC_CMD_DIR				
	65	SDHC_DAT6/GPIO4_25/ USB1_DRVVBUS/ SDHC_DAT0_DIR	SDHC_DAT6	GPIO4_25	USB1_DRVVBUS	SDHC_DAT0_DIR				
	42	SDHC_DAT7/GPIO4_26/ USB1_PWRFAULT/ SDHC_DAT123_DIR	SDHC_DAT7	GPIO4_26	USB1_PWRFAULT	SDHC_DAT123_DIR				

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	62	CLK09/GPIO4_19/BRGO2/ SAI3_RX_BCLK/ FTM4_QD_PHA/2D-ACE_D10	CLK09	GPIO4_19	BRGO2		SAI3_RX_BCLK	2D-ACE_D10	FTM4_QD_PHA	
	71	TDMA_TSYNC/GPIO4_12/ UC1_RTSB_TXEN/ SAI3_TX_SYNC/ FTM4_CH4/2D-ACE_D03	TDMA_TSYNC	GPIO4_12		UC1_RTSB_TXEN	SAI3_TX_SYNC	2D-ACE_D03	FTM4_CH4	
	69	TDMB_RQ/GPIO4_18/ UC3_CDB_RXER/ SPDIF_EXTCLK/ SAI4_RX_BCLK/ FTM4_EXTCLK/2D-ACE_D09	TDMB_RQ	GPIO4_18	SPDIF_EXTCLK	UC3_CDB_RXER	SAI4_RX_BCLK	2D-ACE_D09	FTM4_EXTCLK	
	66	TDMB_RSYNC/GPIO4_15/ UC3_CTSB_RXDV/ SPDIF_PLOCK/ SAI4_TX_BCLK/ FTM4_CH1/2D-ACE_D06	TDMB_RSYNC	GPIO4_15	SPDIF_PLOCK	UC3_CTSB_RXDV	SAI4_TX_BCLK	2D-ACE_D06	FTM4_CH1	
	64	TDMB_RXD/GPIO4_14/ UC3_RXD7/SPDIF_IN/ SAI4_RX_DATA/ FTM4_CH2/2D-ACE_D05	TDMB_RXD	GPIO4_14	SPDIF_IN	UC3_RXD7	SAI4_RX_DATA	2D-ACE_D05	FTM4_CH2	
	44	TDMB_TXD/GPIO4_16/ UC3_TXD7/SPDIF_OUT/ SAI4_TX_DATA/ FTM4_CH0/2D-ACE_D07	TDMB_TXD	GPIO4_16	SPDIF_OUT	UC3_TXD7	SAI4_TX_DATA	2D-ACE_D07	FTM4_CH0	

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Kintex Ultrascale+ FPGA (KU19P) SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Kintex Ultrascale+ FPGA (KU19P) SOM.

Table 8: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[2]	0V	3V	3.15V	±20mV

[1] Kintex Ultrascale+ FPGA (KU19P) SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector2.

[2] Kintex Ultrascale+ FPGA (KU19P) SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

The Kintex Ultrascale+ FPGA (KU19P) SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOMPWR_EN signal from Board to Board Connector1 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board to Board Connector1 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

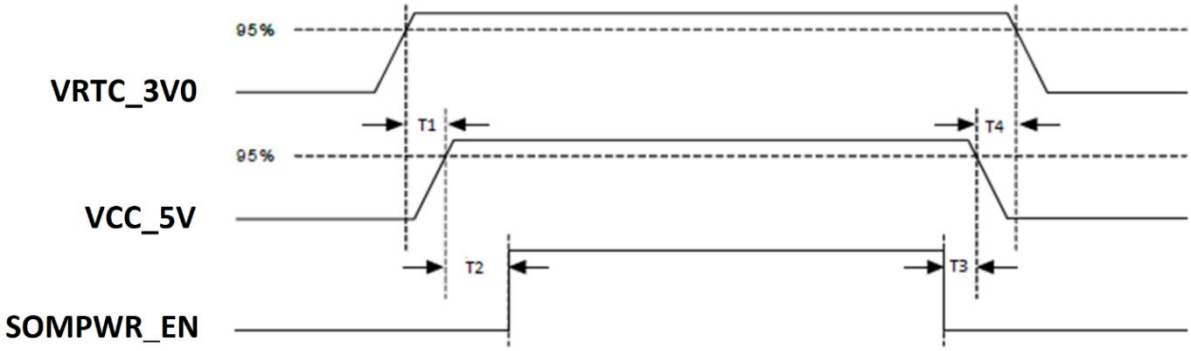


Figure 9: Power Input Sequencing

Table 9: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.

Important Note: VCC_5V input power to other all the powers are getting stable around 50ms in SOM, Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.3 Power Consumption

TBD

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Kintex Ultrascale+ FPGA (KU19P) SOM.

Table 10: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS2 Compliance

iWave's Kintex Ultrascale+ FPGA (KU19P) SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

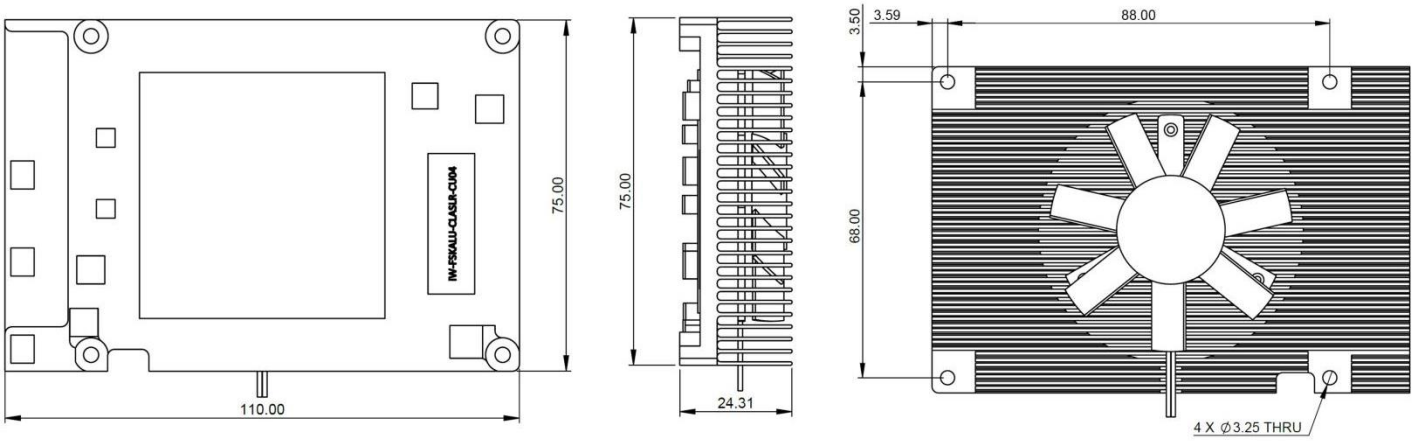
3.2.3 Electrostatic Discharge

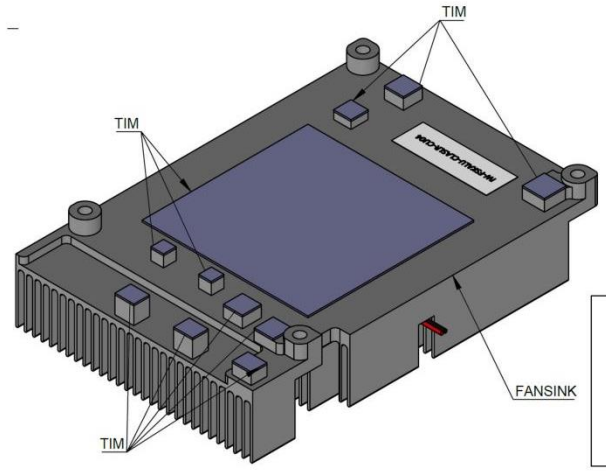
iWave's Kintex Ultrascale+ FPGA (KU19P) SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System on Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.





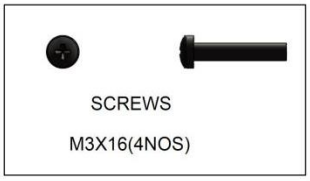


TABLE 1.1: FAN SPECIFICATIONS	
PART NO.	T056010BHZC0U3aR
DIMENSIONS	60X60X10.5mm
AIR FLOW	18.14CFM 0.51m3/min
STATIC PRESSURE	3.00mmH2O
RATED VOLTAGE	5V
LIFE EXPECTANCY	50,000hours at 40°C (WITH 15~65% RH)
ROHS	YES
CONNECTOR PART NO	510210200
CABLE LENGTH	150mm

TABLE1.2: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
THERMAL CONDUCTIVITY	6.5W/mK
FLAME RATING	UL 94 V-0
HARDNESS	27 Shore 00
WORKING TEMP.	-40~+160 °C
ROHS	YES

Figure 10: Heat Sink

3.3 Mechanical Characteristics

3.3.1 Kintex Ultrascale+ FPGA SOM Mechanical Dimensions

Kintex Ultrascale+ FPGA (KU19P) SOM PCB size is 110mm x 75mm x 2.64mm and weight is 125g. SOM mechanical dimension is shown below.

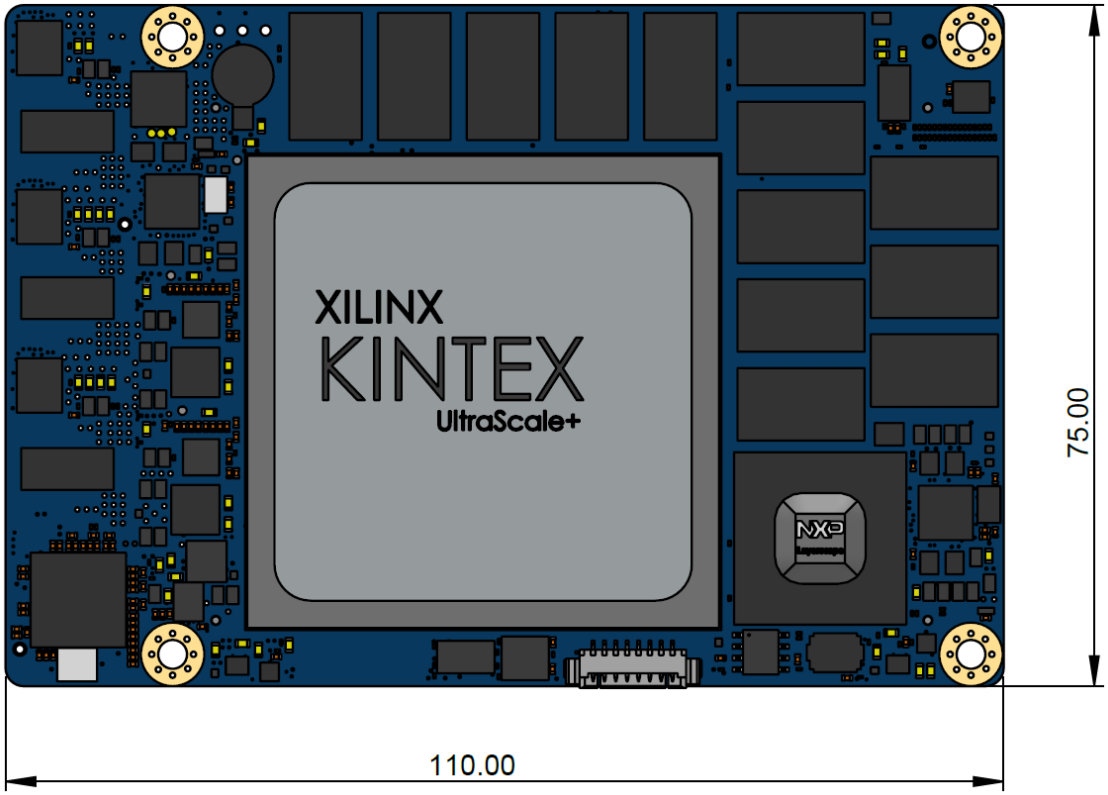


Figure 11: Mechanical dimension of Kintex Ultrascale+ FPGA SOM - Top View

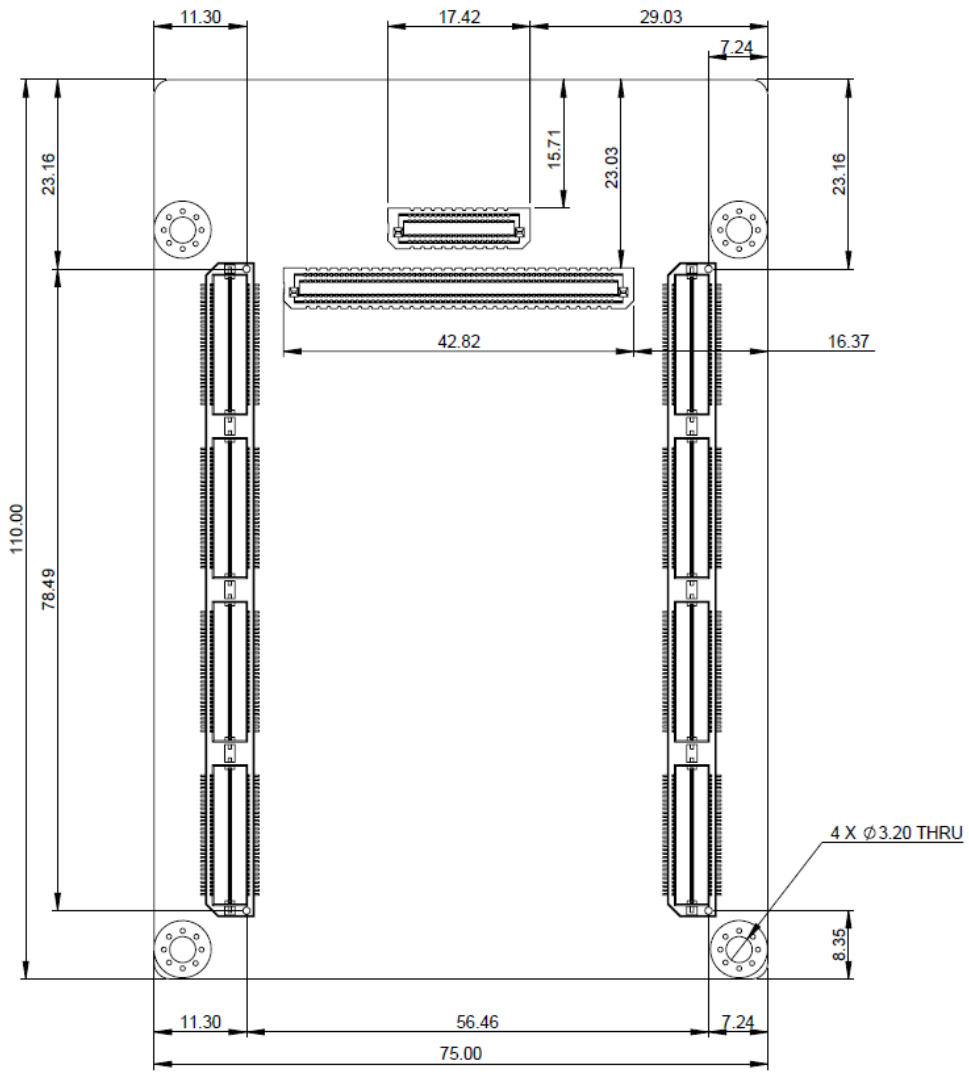


Figure 12: Mechanical dimension of Kintex Ultrascale+ FPGA SOM - Bottom View

Kintex Ultrascale+ FPGA (KU19P) PCB thickness is 2.64mm±0.1mm, top side maximum height component is Inductors L1, L2, L3 (6mm) and bottom side maximum height component is Board to Board connector 1 & 2 (4.27mm) followed by Board-to-Board connector 3(4.02mm). Please refer the below figure which gives height details of the Kintex Ultrascale+ FPGA SOM.

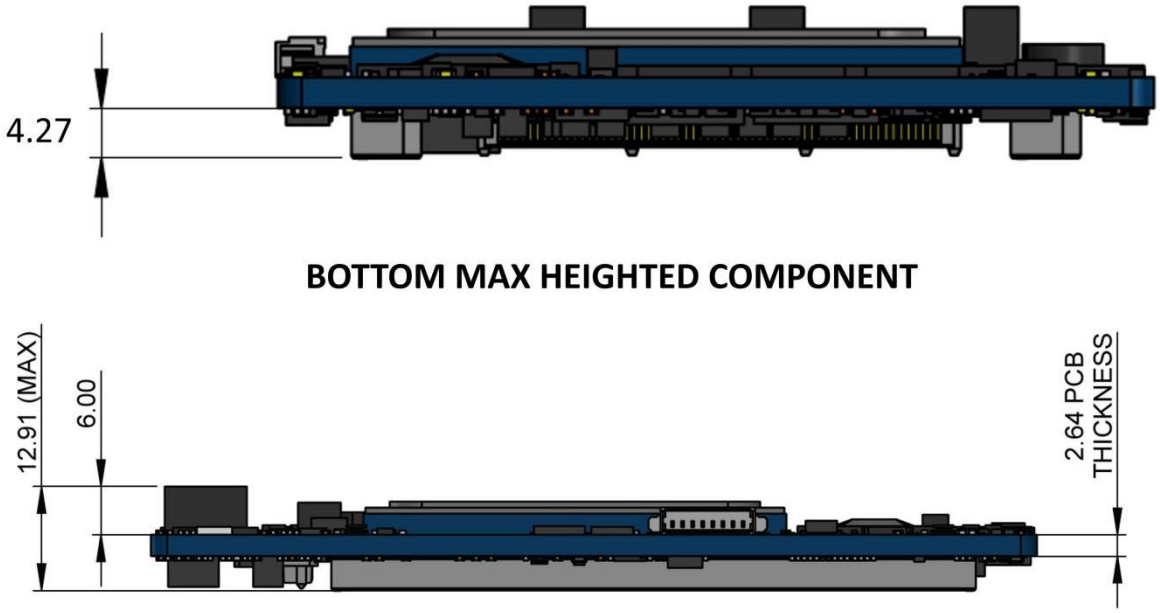


Figure 13: Mechanical dimension of Kintex Ultrascale+ FPGA SOM - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Kintex Ultrascale+ FPGA (KU19P) SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 11: Orderable Product Part Numbers

Product Part Number	Description	Temperature
TBD	TBD	TBD

5. APPENDIX

5.1 Kintex Ultrascale+ FPGA SOM Development Platform

iWave Systems supports iW-RainboW-G47D– Kintex Ultrascale+ FPGA SOM Development Platform which is targeted for quick validation of Kintex Ultrascale+ FPGA (KU19P) based SOM. iWave's Kintex Ultrascale+ FPGA Development Board incorporates Kintex Ultrascale+ FPGA (KU19P) SOM and High-performance Carrier board with complete BSP support.

Contact us for more details on Kintex Ultrascale+ FPGA (KU19P) SOM Development Platform.

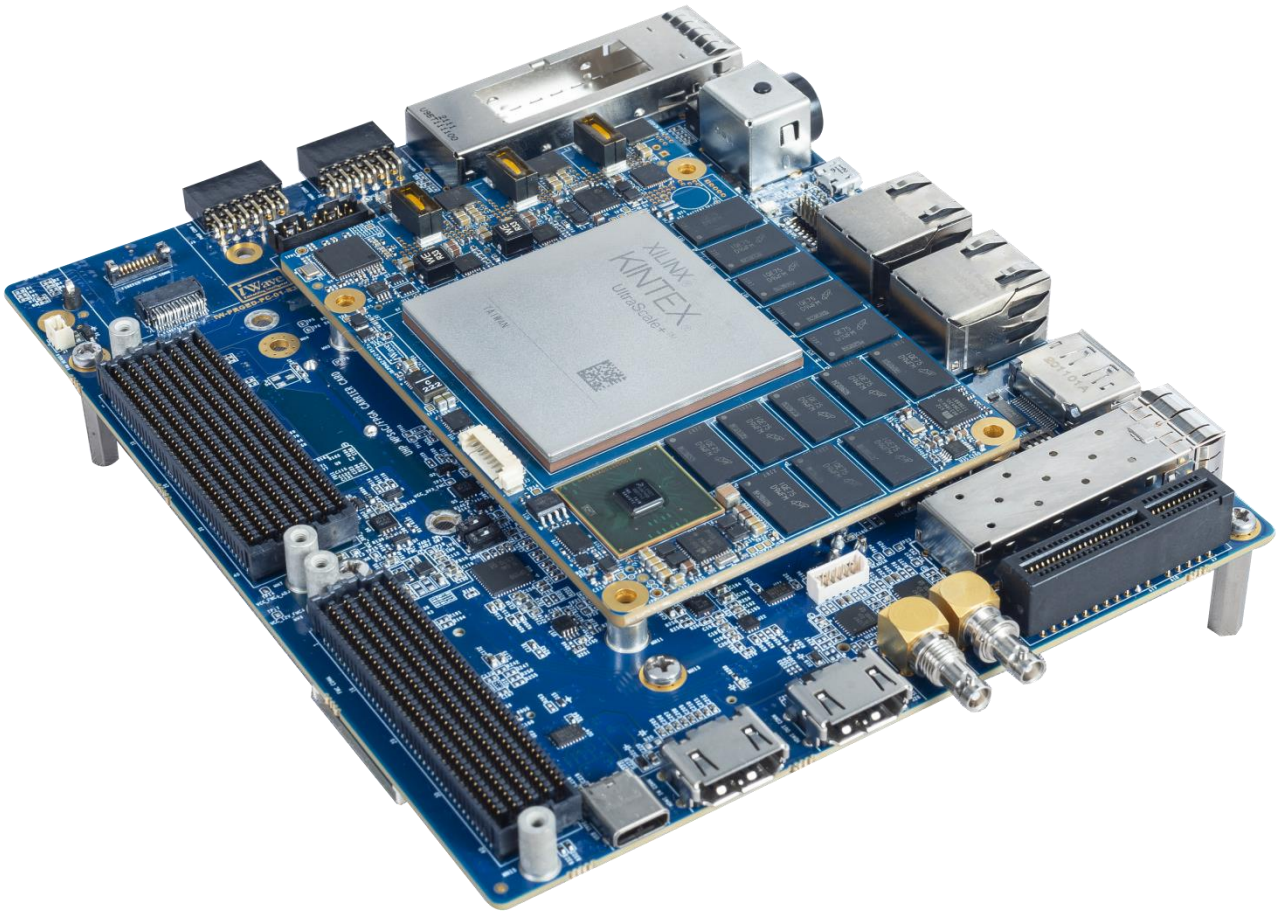


Figure 14 Kintex Ultrascale+ FPGA (KU19P) Development Platform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