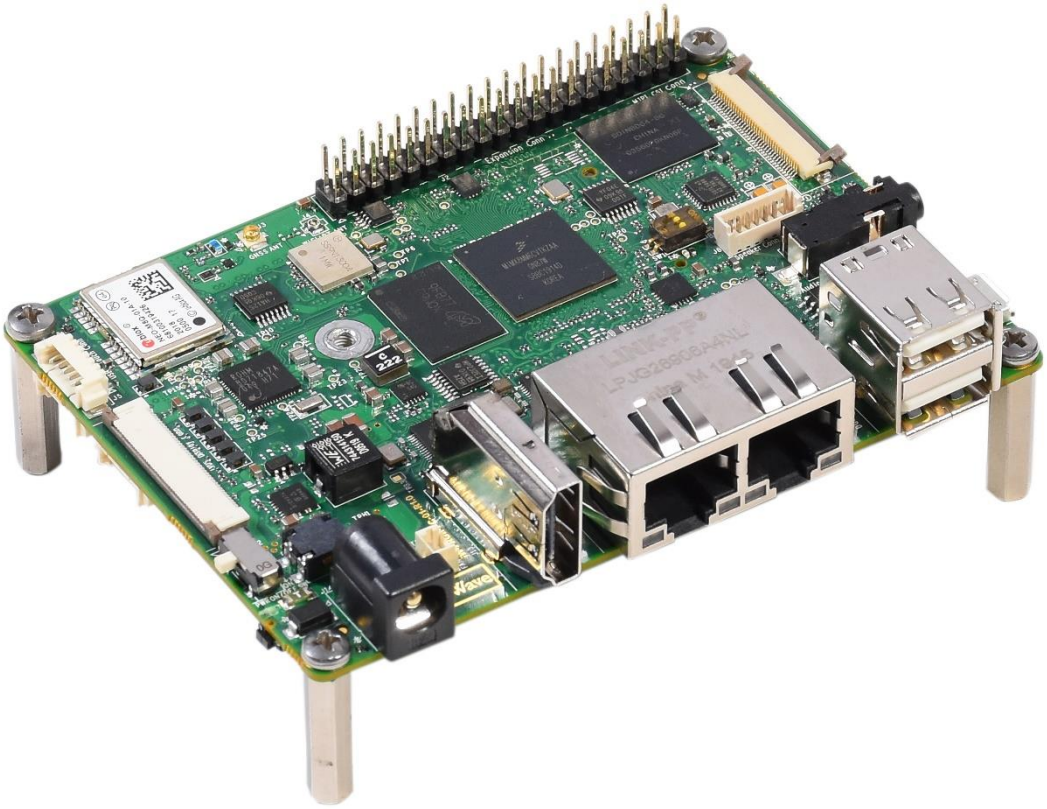
iW-RainboW-G34S
i.MX 8M Mini or i.MX 8M Nano Pico ITX Single Board Computer
Hardware User Guide



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0.1	12th May 2021	Initial Draft Release
0.2	03rd Dec 2021	• Removed G37S • Made RS485 as default support and RS232 as Optional
0.3	02nd Feb 2022	BD71847AMWV-E2 common PMIC for both Mini and Nano

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Pico ITX Single Board Computer based on the NXP's i.MX 8M Mini or i.MX 8M Nano Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC from a Hardware Systems perspective.

1.2 Pico ITX SBC Overview

The Pico ITX is a versatile small form factor SBC (Single Board Computer) definition targeting application that require low power, low costs, and high performance. The SBCs are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE, GNSS module and LVDS/HDMI display are concentrated on the Module.

NXP's i.MX 8M Mini or i.MX 8M Nano SoC based Pico ITX Single Board computer is rich with i.MX 8M Mini or i.MX 8M Nano features along with, eMMC, Dual Ethernet PHY, USB2.0 Hub, GNSS module, Wi-Fi & BT module and comes in compact 100mm x 72mm form factor.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound

Acronyms	Abbreviations
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LVDS	Low Voltage Differential Signal
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OTG	On-The-Go
PCB	Printed Circuit Sheet
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SBC	Single Board Computer
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on SBC.

1.5 References

- i.MX 8M Mini SoC
  - IMX8MMIEC_Revx.x.pdf
  - IMX_8M_Mini_RM_Revx.x.pdf

- i.MX 8M Nano SoC
  - IMX8MNIEC_Revx.x.pdf
  - IMX_8M_Nano_RM_Revx.x.pdf

1.6 Important Note

In this document, wherever i.MX 8M Mini or i.MX 8M Nano SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_9)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO1_9*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC features and Hardware architecture with high level block diagram.

2.1 i.MX 8M Mini or i.MX 8M Nano Pico ITX Block Diagram

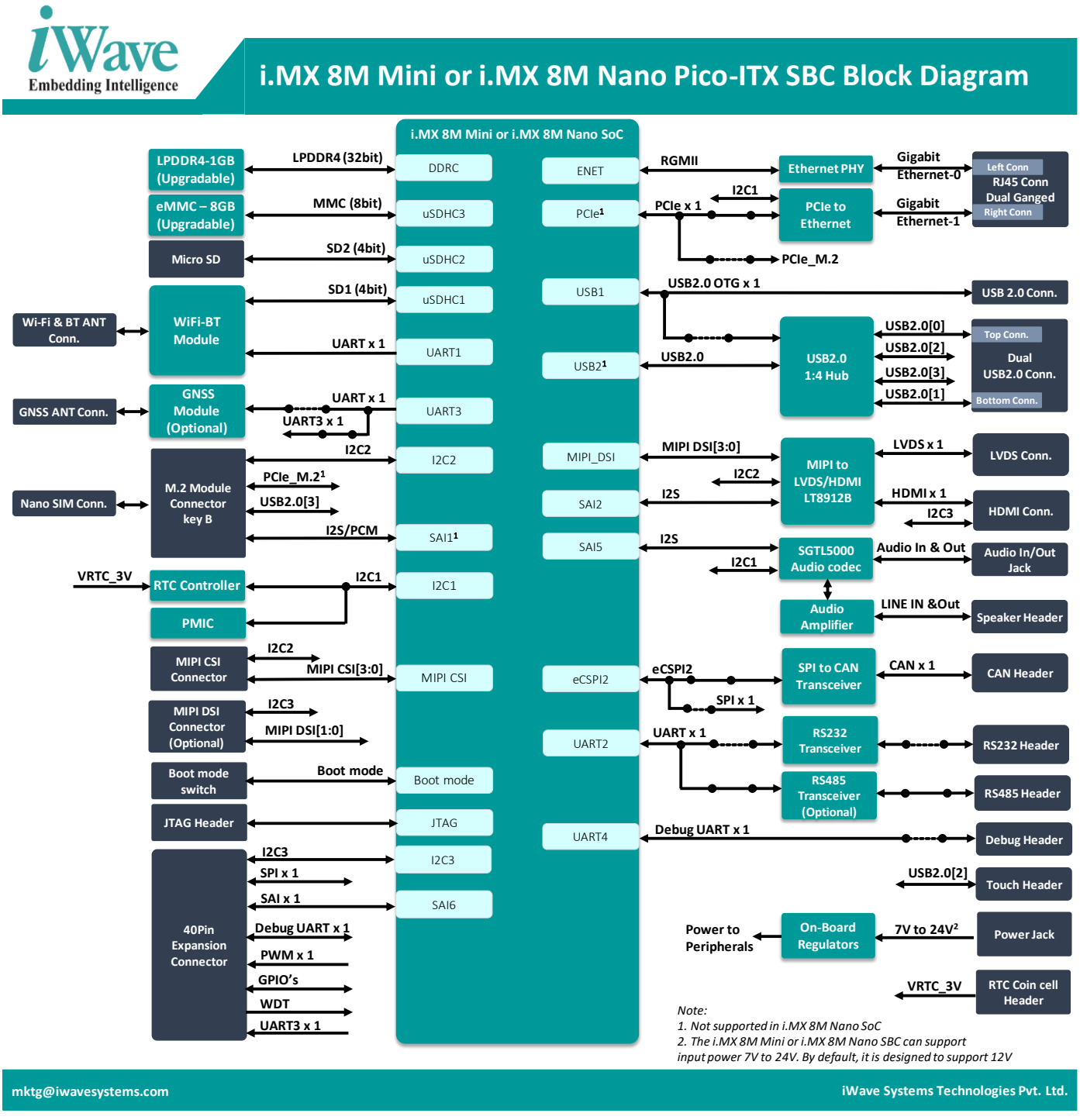

Figure 1 : i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Block Diagram

2.2 i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Features

i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports the following features.

CPU

- i.MX 8M MiniQ/QL/D/DL/S/SLProcessor[1]:
  - i.MX 8M Mini Quad : 4 x Cortex- A53,1 x Cortex-M4
  - i.MX 8M Mini Quad Lite : 4 x Cortex- A53,1 x Cortex-M4(VPU not supported)
  - i.MX 8M Mini Dual : 2 x Cortex- A53,1 x Cortex-M4
  - i.MX 8M Mini Dual Lite : 2 x Cortex- A53,1 x Cortex-M4(VPU not supported)
  - i.MX 8M Mini Solo : 1 x Cortex- A53, 1 x Cortex-M4
  - i.MX 8M Mini Solo Lite : 1 x Cortex- A53,1 x Cortex-M4(VPU not supported)
- i.MX 8M Nano Q/QL/D/DL/S/SL Processor[1]:
  - i.MX 8M Nano Quad : 4 x Cortex- A53,1 x Cortex-M7
  - i.MX 8M Nano Quad Lite : 4 x Cortex- A53,1 x Cortex-M7 (GPU not supported)
  - i.MX 8M Nano Dual : 2 x Cortex- A53,1 x Cortex-M7
  - i.MX 8M Nano Dual Lite : 2 x Cortex- A53,1 x Cortex-M7 (GPU not supported)
  - i.MX 8M Nano Solo : 1 x Cortex- A53, 1 x Cortex-M7
  - i.MX 8M Nano Solo Lite : 1 x Cortex- A53,1 x Cortex-M7 (GPU not supported)

Power

- BD71847AMWV-E2 PMIC

Memory

- i.MX 8M Mini SBC
  - LPDDR4 - 1GB (Expandable up to 8GB)[2,3]
- i.MX 8M Nano SBC
  - LPDDR4 - 1GB (Expandable up to 2GB)[2,3]
- eMMC Flash - 8GB (Expandable)[3]
- Micro SD slot

Network & Communication

- WiFi 802.11a/b/g/n/ac + Bluetooth 5.0 Module
- Gigabit Ethernet PHY Transceiver
- PCIe to Ethernet PHY[4]
- USB 2.0 Hub through dual stack Type-A Connector[5]
- USB 2.0 OTG port through - microAB Receptacle Connector[5]
- RS485 x 1
- CAN x 1

- GNSS Module (Optional)
- RS232 x 1 (Optional)

Audio/Video Features

- HDMI Output through HDMI (Type A) Connector[6]
- 10.1" LVDS Display[6]
- I2S Audio Codec
- 3.5mm Audio IN/OUT
- MIPI CSI x 1 Channel
- 2 Lane MIPI DSI Display (Optional)

Expansion Connector Interfaces

- SPI x 1 Port (Optional)
- UART x 1 Port
- I2C x 1 Port (Optional)
- SAI x1 Port (Optional)
- Debug UART x 1 Port
- PWM x 1 Port

Miscellaneous Interfaces

- Debug UART Connector (Optional)
- JTAG Header
- RTC Battery Connector
- M.2 Connector Key B
    - PCIe × 1 (Optional) [4]
    - USB 2.0 x 1
    - I2S x 1
    - I2C x 1
    - Nano SIM Connector

General Specification

- Power Supply : 12V, 2A[7]
- Form Factor : 100mm X 72mm

1. *There are six configurations of i.MX 8M Mini or i.MX 8M Nano SoC supported by NXP, hence in this document i.MX 8M Mini or i.MX 8M NanoQ/QL/D/DL/S/SLis used to represent either of one based on SBC Part Number.*

2. *The i.MX 8M Mini CPU can support up to 8GB RAM but considering the available LPDDR4 Chips, SBC can support up to 4GB (32Gb) RAM.*
3. *Memory Size will differ based on iWave's SBC Product Part Number.*
4. *PCIe is not supported in i.MX 8M Nano SoC.*
5. *Since USB2 is NC in i.MX 8M Nano SoC, USB2.0 lines are supported through a switch.*
6. *Either HDMI or LVDS can be supported. By default, HDMI display is supported.*
7. *The i.MX 8M Mini or i.MX 8M Nano SBC can support wide range input power from 7V to 24V. By default, it is designed to support 12V.*

2.3 CPU

iW-RainboW-G34S i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC can support different i.MX 8M Mini or i.MX 8M Nano SoCs from NXP.

2.3.1 i.MX 8M Mini CPU

The i.MX 8M Mini Family consists of six processors: i.MX 8M Mini Quad, Quad Lite, Dual, Dual Lite, Solo, Solo Lite.

The Major difference between i.MX 8M Mini SoCs are:

- i.MX 8M Mini Quad : 4 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Quad Lite : 4 x Cortex- A53, 1 x Cortex-M4(VPU not supported)
- i.MX 8M Mini Dual : 2 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Dual Lite : 2 x Cortex- A53, 1 x Cortex-M4(VPU not supported)
- i.MX 8M Mini Solo : 1 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Solo Lite : 1 x Cortex- A53, 1 x Cortex-M4(VPU not supported)

The i.MX 8M Mini Family supports ARM Cortex-A53 Core @ 1.6 GHz, ARM Cortex-M4F Core @ 400 MHz, 1080p, VPU, and dual failover-ready display controllers, 1× 1080pdisplay, including MIPI-DSI. Memory interfaces supporting LPDDR4, DDR4, DDR3L, Quad SPI/Octal SPI (Flex SPI), eMMC 5.1, RAW NAND and SD, and a wide range of peripheral I/Os such as PCIe 2.0 provide wide flexibility.

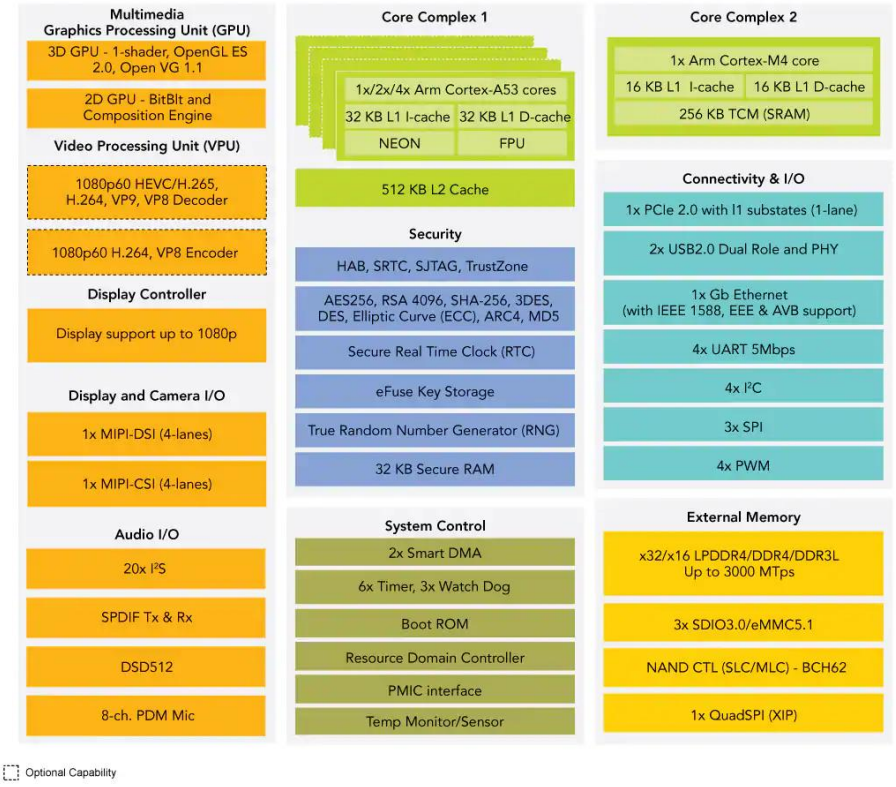

Figure 2: i.MX 8M Mini Block Diagram

2.3.2 i.MX 8M Nano SoC

The i.MX 8M Nano Family consists of six processors: i.MX 8M Nano Quad, Quad Lite, Dual, Dual Lite, Solo, Solo Lite. The Major difference between i.MX 8M Nano SoCs are:

- i.MX 8M Nano Quad : 4 x Cortex- A53, 1 x Cortex-M7
- i.MX 8M Nano Quad Lite : 4 x Cortex- A53, 1 x Cortex-M7 (VPU not supported)
- i.MX 8M Nano Dual : 2 x Cortex- A53, 1 x Cortex-M7
- i.MX 8M Nano Dual Lite : 2 x Cortex- A53, 1 x Cortex-M7 (VPU not supported)
- i.MX 8M Nano Solo : 1 x Cortex- A53, 1 x Cortex-M7
- i.MX 8M Nano Solo Lite : 1 x Cortex- A53, 1 x Cortex-M7 (VPU not supported)

The i.MX 8M Nano Family supports ARM Cortex-A53 Core @ 1.4 GHz, ARM Cortex-M7 Core @ 600 MHz, 1080p, and dual failover-ready display controllers, 1× 1080p display, including MIPI-DSI. Memory interfaces supporting LPDDR4, DDR4, DDR3L, Quad SPI/Octal SPI (Flex SPI), eMMC 5.1, RAW NAND and SD, and a wide range of peripheral I/Os.

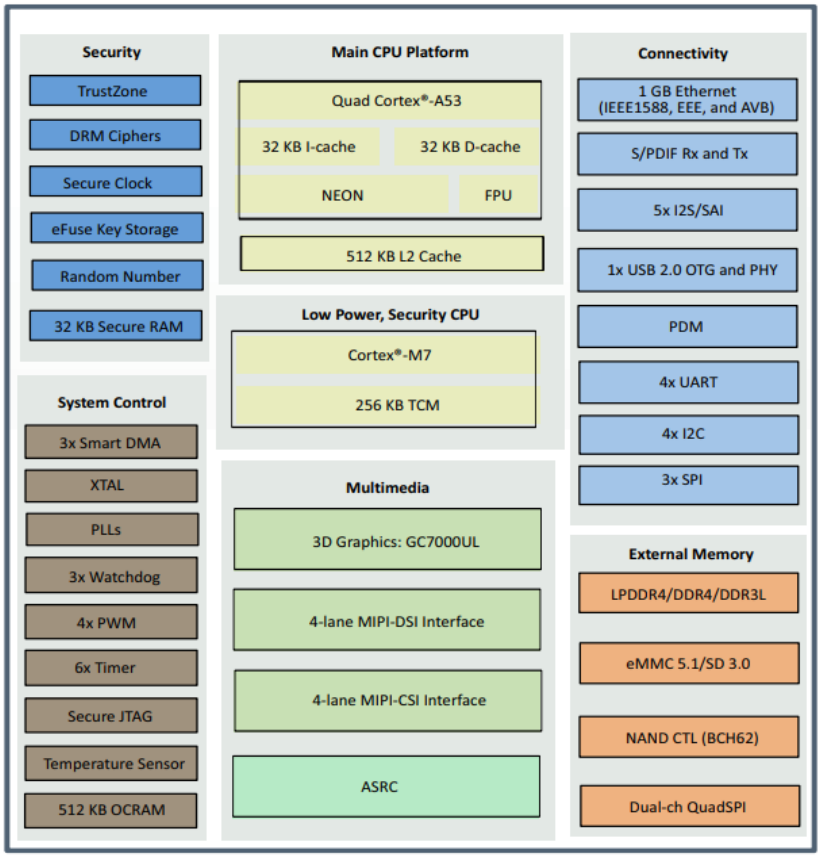

Figure 3: i.MX 8MNano Block Diagram

Note: The i.MX 8M Mini or i.MX 8M Nano processor offers numerous advanced features, please refer the latest i.MX 8M Mini or i.MX 8M Nano Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PMIC

i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Rohm's BD71847AMWV on-board PMIC for Power management of i.MX 8M Mini or i.MX 8M Nano SBCs. The BD71847AMWV is a Power Management Integrated Circuit (PMIC) designed specifically for powering single-core, dual-core, and quad-core SoC's such as NXP-i.MX 8M Mini.

The BD71847AMWV features six high efficiency buck converters and six linear regulators (LDOs) for powering the processor, memory and miscellaneous peripherals. Built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through I2C1 after start up offering flexibility for different system states. The BD71847AMWV(U12) comes in 56pin QFN Package and placed on top side of SBC.

2.5 Memory

2.5.1 LPDDR4 RAM

This SBC supports 1GB RAM using 32bit LPDDR4 IC for i.MX 8M Mini and 1GB RAM using 16bit LPDDR4 IC for i.MX 8M Nano connected to DDR controller of CPU to support LPDDR4 clock up to 1.5 GHz in Mini and up to 1.6GHz in Nano. The LPDDR4 IC(U14) placed on Top side of the SBC. The RAM size can be expandable up to maximum of 8GB in Mini and up to 2GB in Nano. To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports 8GB eMMC as default boot device and storage device. This is connected to eMMC0 version 5.1v controller of the i.MX 8M Mini or i.MX 8M Nano SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash (U8) memory is physically located on top side of the SBC. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD Connector

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports Micro SD slot which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J20) is directly connected to the USDHC2 controller of the i.MX 8M Mini or i.MX 8M Nano SoC. The main power to Micro SD Card Connector is 3.3 Voltage. The Micro SD Connector is physically located on bottom side of the i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC as shown below.

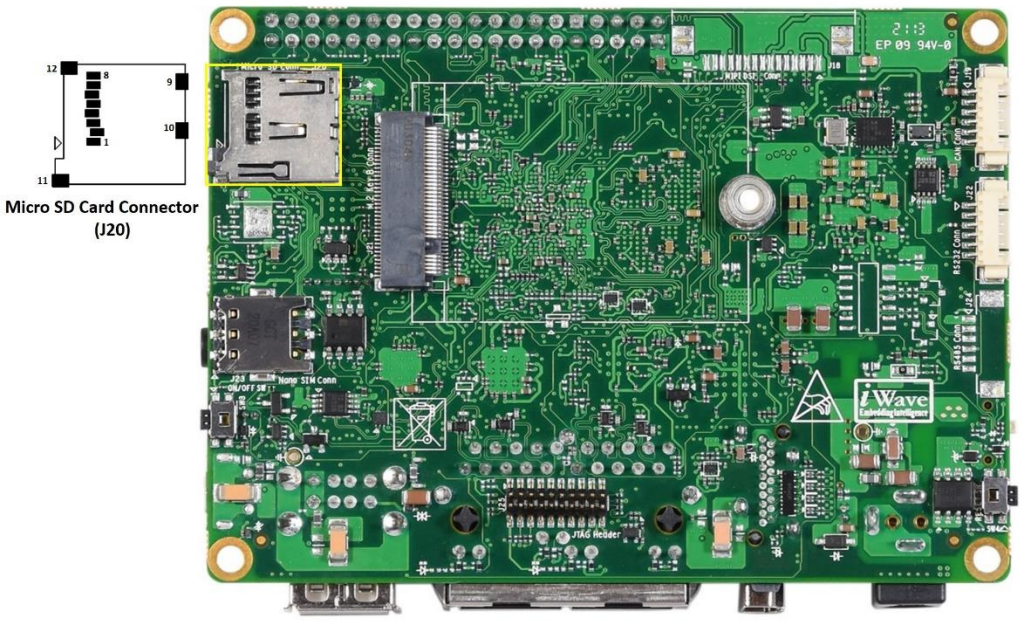

Figure 4: Micro SD Card Connector

2.6 RTC Controller

The i.MX 8M Mini or i.MX 8M Nano SBC supports external RTC Controller “PCF85263” for Real time clock support. This external RTC Controller IC (U27) is connected to i.MX 8M Mini or i.MX 8M Nano SBC through I2C1 Interface and operates at 3.3V voltage level. In SBC power off condition, this device will take power from (VRTC_3V0) coin cell power input and continues to keep the current time.

2.7 Boot Media Setting

i.MX 8M Mini or i.MX 8M Nano SoC boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. i.MX 8M Mini SoC Boot ROM code uses the state of the internal register BOOT_MODE [1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device.

Note: Contact iWave if different boot media support is required other than eMMC flash.

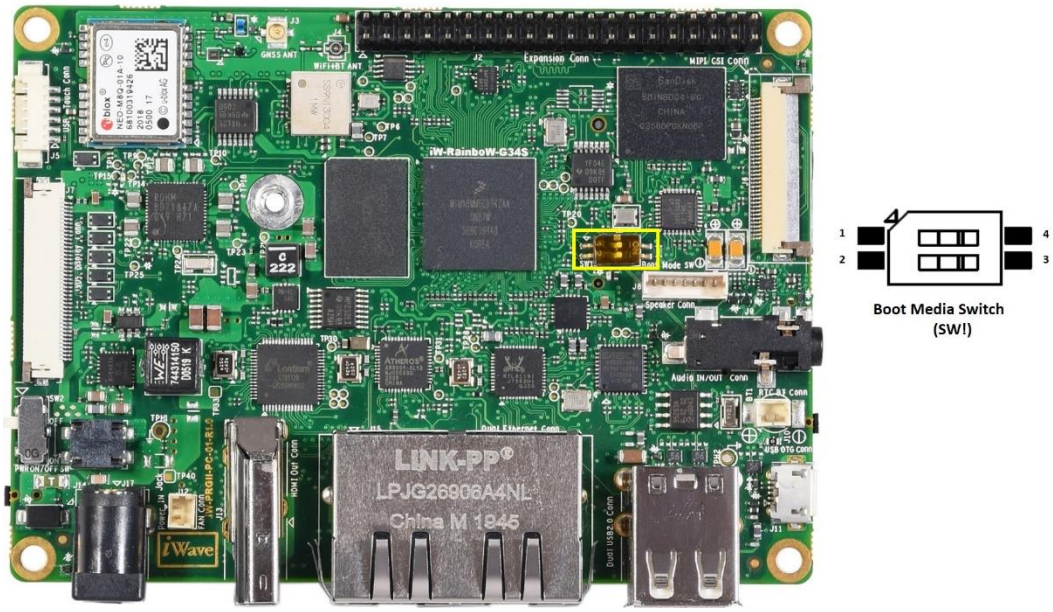

Figure 5: Boot Media Switch

Table 3: Boot Media Switch Settings

Boot Media	SW1 (2 Position Switch)	
	POS1	POS2
Boot from Fuse	ON	ON
USB Serial Download	ON	OFF
eMMC	OFF	ON
Reserved	OFF	OFF

Table 4: Boot Mode Pin Settings Truth Table

BOOT_MODE [1]	BOOT_MODE [0]	Boot Type	Description
1	0	Internal Boot Mode	In this mode, i.MX 8M Mini or i.MX 8M Nano boots from eMMC.
0	1	Serial Downloader Mode	In this mode, i.MX 8M Mini or i.MX 8M Nano boot media can be Programmed through its USB OTG interface using UUU tool supported by NXP.

2.8 Network & Communication

2.8.1 Wi-Fi and Bluetooth Interface

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC is integrated with Murata's "LBEE5HY1MW" based Wi-Fi& Bluetooth module. The LBEE5HY1MW module is a very high-performance module based on Cypress CYW43455 combo chipset which supports WiFi IEEE 802.11a/b/g/n/ac + Bluetooth 5.0 BR/EDR/LE standard.

The LBEE5HY1MW module utilizes highly optimized IEEE 802.11 Bluetooth coexistence protocols and supports single stream 1x1 IEEE 802.11a/b/g/n/ac mode providing up to 390Mbps. The LBEE5HY1MW module features small form factor when integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive switch, Power Management. The LBEE5HY1MW module need external Antenna but it requires a 32.768 kHz clock for sleep operation.

The LBEE5HY1MW module (U7) provides Secure Digital Input Output (SDIO) for interfacing with the host controller for Wi-Fi and UART interface for Bluetooth. The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC uses processor's UART1 interface for Bluetooth and USDHC1 interface for Wi-Fi in default configuration. In i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC, antenna pin of Wi-Fi & Bluetooth module is connected to J4 Connector.

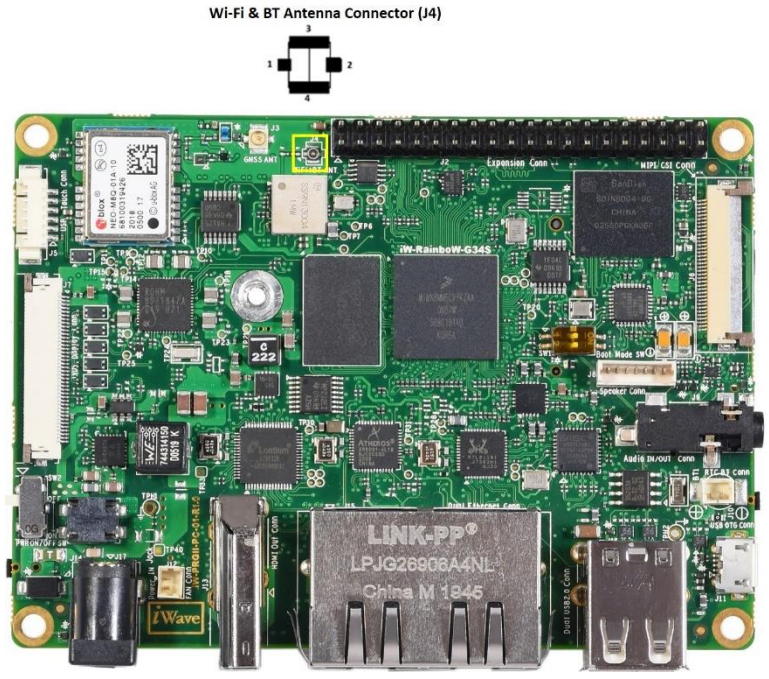

Figure 6: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number : MM4829-2702RA4from Murata Electronics.

Antenna Part Number : 2042811100 from Molex/FXP830.24.0100B from Taoglas Limited

Note: The LBEE5HY1MW module supports operating temperature -30°C to 85°C with the default module's firmware. To set the module temperature to industrial grade in firmware, please contact iWave.

2.8.2 Gigabit Ethernet Interface

The i.MX 8M Mini or i.MX 8M Nano PICO ITX SBC supports Dual Ethernet Port interface through external Ethernet PHY and PCIe to Ethernet PHY.

The Ethernet PHY AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. The SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

Second Ethernet port is supported through PCIe to Ethernet controller "RTL8119" from Realtek. This Ethernet controller is interfaced with i.MX 8M Mini using PCIe Lane. This controller combines IEEE 802.3 compliant MAC and Ethernet transceiver.

The Ethernet PHY and PCIe to Ethernet PHY's output signals are directly connected to Dual RJ45 Magjack (J14), Left & Right connector respectively. Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. The Dual RJ45 Magjack connector is physically located at the top of the board as shown below.

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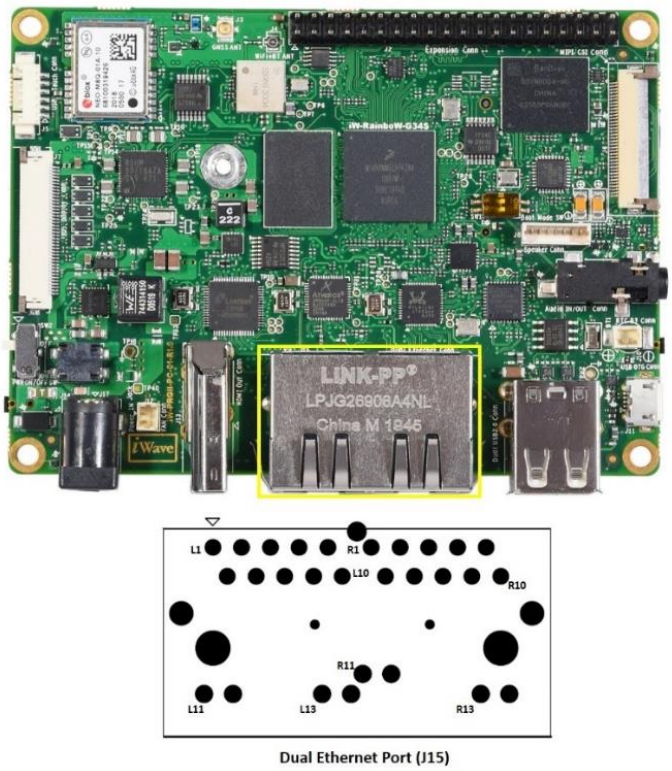

Figure 7: Dual RJ45 Magjack

Note: Since PCIe is not supported in i.MX 8M Nano SoC only 1 Ethernet port can be supported.

2.8.3 USB2.0 Host Interface

The i.MX8M Mini SoC supports two USB2.0 OTG, whereas i.MX 8M Nano supports single USB2.0 OTG. Hence for i.MX 8M Nano Pico ITX SBC, USB 2.0 lines are supported through a switch.

In i.MX 8M Nano SBC, USB OTG will be supported only in Flash mode. In Boot mode only USB2.0 host is supported.

The Dual stack USB2.0 Type-A connector is physically located at the top of the board as shown below.

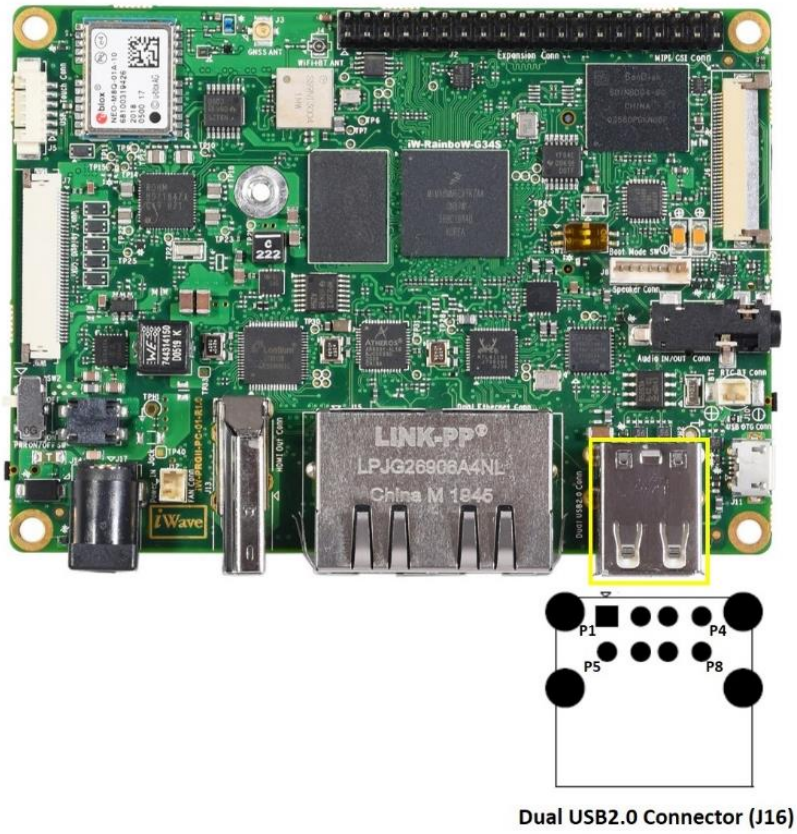

Figure 8: Dual Stack USB2.0 Type A connector

2.8.4 USB2.0 OTG Interface

The i.MX 8M Mini or i.MX 8M Nano PICO ITX SBC supports USB2.0 High Speed OTG interface through SoC's USB_OTG1 interface. This USB2.0 signals of i.MX 8M Mini SoC is directly connected to USB2.0 MicroAB connector (J11). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status.

This USB2.0 OTG connector is physically located at the top of the board as shown below.

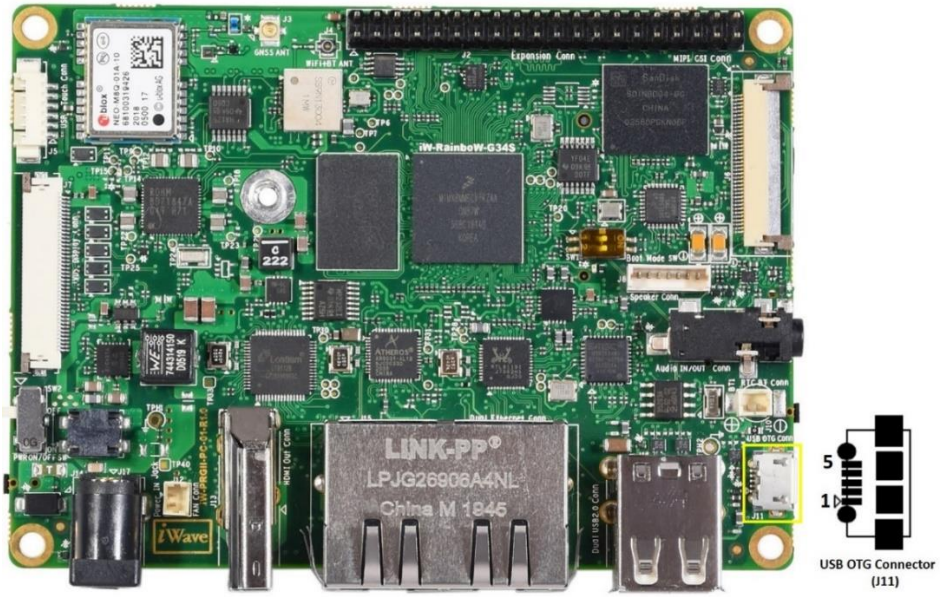

Figure 9: USB OTG Connector

2.8.5 GNSS Module (Optional)

The i.MX 8M Mini or i.MX 8M Nano PICO ITX SBC optionally supports u-blox's "NEO-M8Q-01A" based GNSS module. The NEO-M8Q-01A module is built on the exceptional performance of the u-blox M8 GNSS engine in the industry proven NEO form factor. It utilizes concurrent reception of up to three GNSS systems (GPS/Galileo together with BeiDou or GLONASS) for more reliable positioning.

The NEO-M8Q-01A provides high sensitivity and minimal acquisition times while maintaining low system power. The NEO-M8Q-01A combines a high level of robustness and integration capability along with flexible connectivity options via USB, I2C UART and SPI. The DDC (I2C compatible) interface provides connectivity and enables synergies with most u-blox cellular modules.

The i.MX 8M Mini or i.MX 8M Nano PICO ITX SBC makes use of the UART3 interface which is by default connected to the SMARC Edge connector for communication between the Host and Device. The Antenna pin of the module can be connected to the J6 Antenna connector through an Active or Passive Path as per the requirement.

Connector Part Number : 734120110 from Molex.

Antenna Part Number : TBD

2.8.6 CAN Interface

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports a Control Area Network Flexible Data rate (CAN FD) Port through SPI to CAN FD Controller. The CAN FD Controller (TCAN4550) has integrated CAN FD Transceiver and supports upto 5Mbps data rate. CANL & CANH of the transceiver are connected to J19 (CAN) connector.

This Connector is placed on bottom side of the Board.

Number of Pins : 6

Connector Part Number : 532610671 from Molex

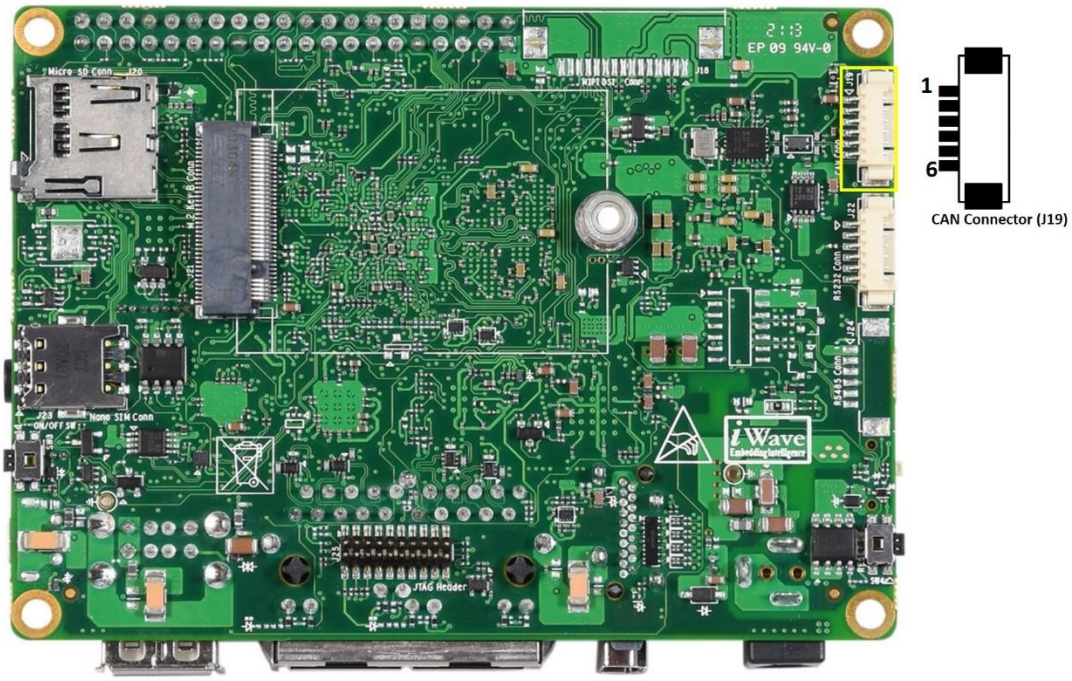

Figure 10: CAN Connector

Table 5: CAN Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*NC.*
3	CANL	FD_CAN_L	IO, DIFF	CAN Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	FD_CAN_H	IO, DIFF	CAN High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.9 Serial Interface Features

2.9.1 Debug UART Interface

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports debug interface through SoC's UART4 interface. This UART4 signals from the SoC is connected to Debug UART header (J1) through 1.8V to 3.3V level Translator. This Debug UART header is optional. By default, debug UART signals are connected to Expansion Connector (J2).

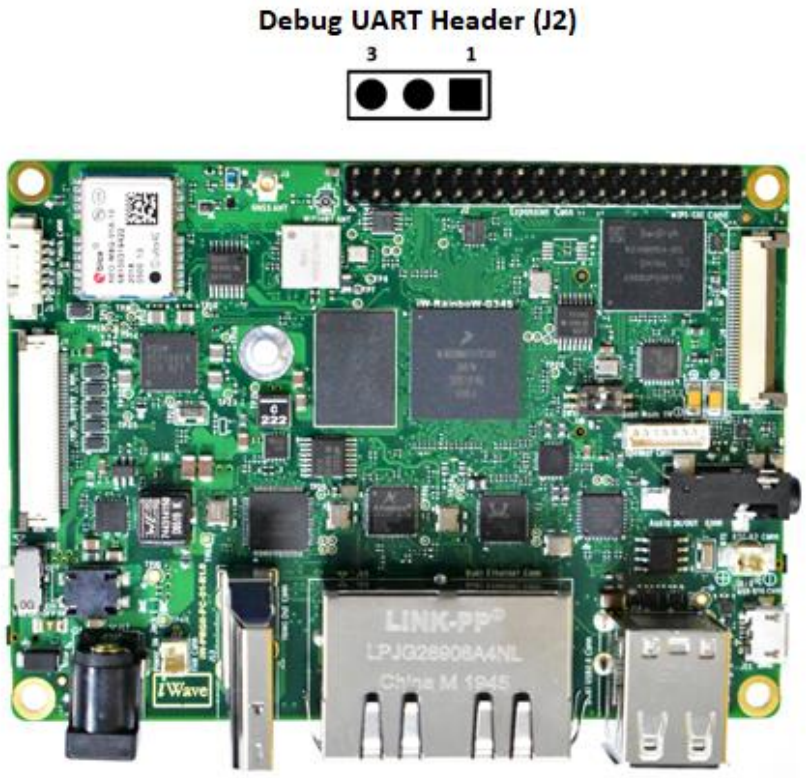

Figure 11: Debug UART Header (Optional)

Table 6: Debug UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	RX	UART4_RXD	O, 3.3V CMOS	UART4 interface Receive signal.
2	TX	UART4_TXD	I, 3.3V CMOS	UART0 interface Transmit signal.
3	GND	GND	Power	Ground.

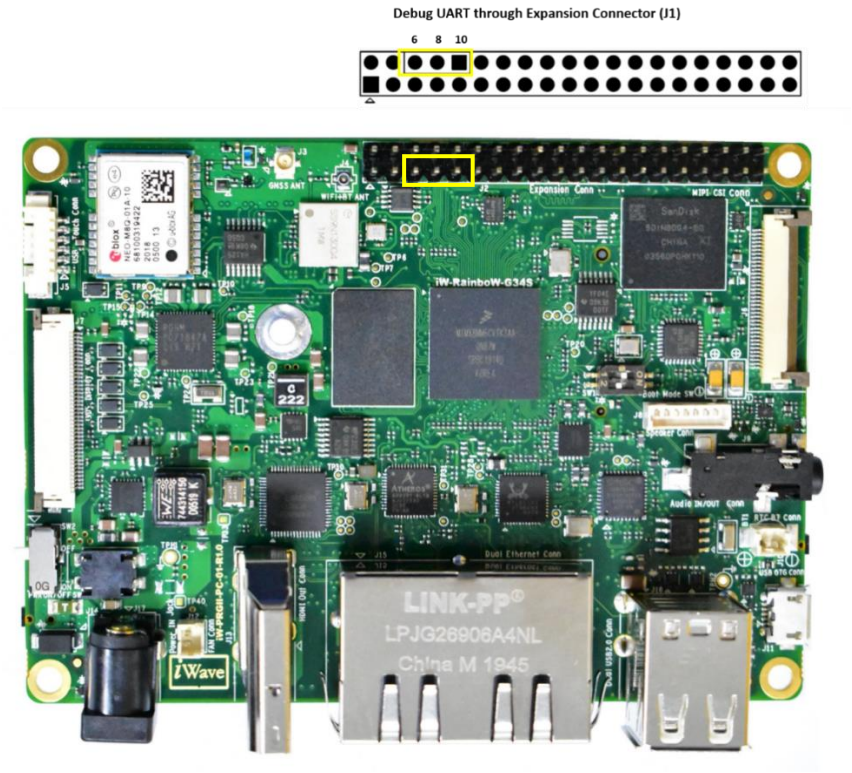

Figure 12: Debug UART through Expansion Connector

Table 7: Debug UART through Expansion Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
6	GND	GND	Power	Ground.
8	TX	UART4_TXD	I, 3.3V CMOS	UART0 interface Transmit signal.
10	RX	UART4_RXD	O, 3.3V CMOS	UART4 interface Receive signal.

2.9.2 RS232 Data UART Interface (Optional)

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC optionally supports RS232 Data Interface through SoC's UART2 interface. By default, this UART2 signals from the SoC is connected to "MAX3232" RS-232 Line Driver and Receiver via 1.8V to 3.3V level Translator. The RS232 Signals are connected from MAX3232 to RS232 Header (J22), which is physically located at the bottom of the board as shown below.

Number of Pins : 6

Connector Part number : 532610671from Molex

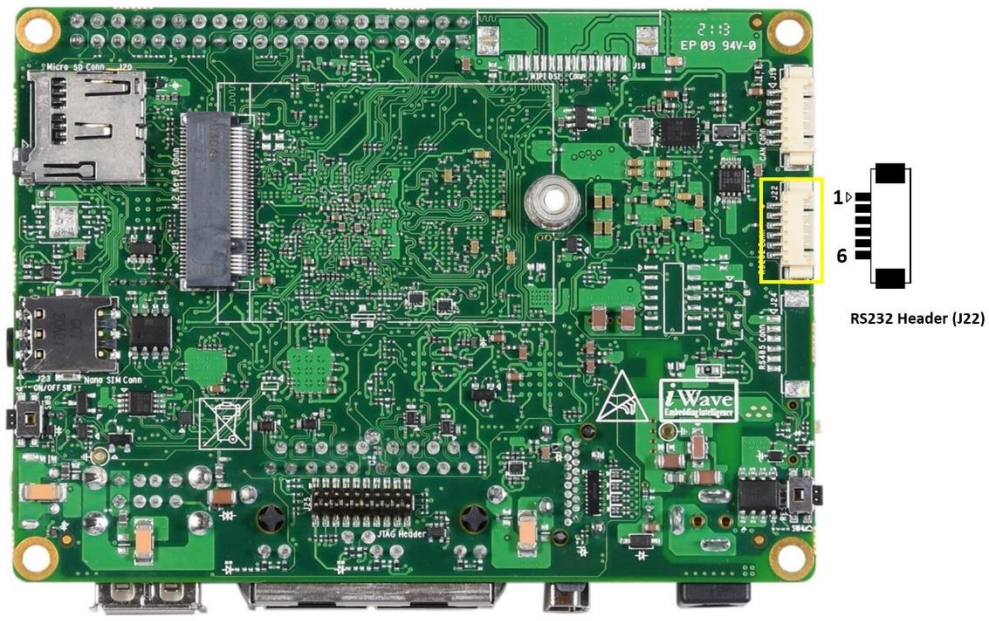

Figure 13: RS232 Header

Table 8: RS232 Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS	RS232_RTS	I, RS232	RS232 interface Clear to Send signal.
3	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	TXD	RS232_RXD	O, RS232	RS232 interface Receive signal.
5	RXD	RS232_TXD	I, RS232	RS232 interface Transmit signal.
6	RTS	RS232_CTS	O, RS232	RS232 interface Ready to Send signal.

2.9.3 RS485 Data UART Interface

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports RS485 Data Interface through SoC's UART2 interface. The RS485 Signals are connected from SN65HVD73DR transceiver to RS485 Header (J24), which is physically located at the bottom of the board as shown below.

Number of Pins : 6

Connector Part Number : 532610671 from Molex

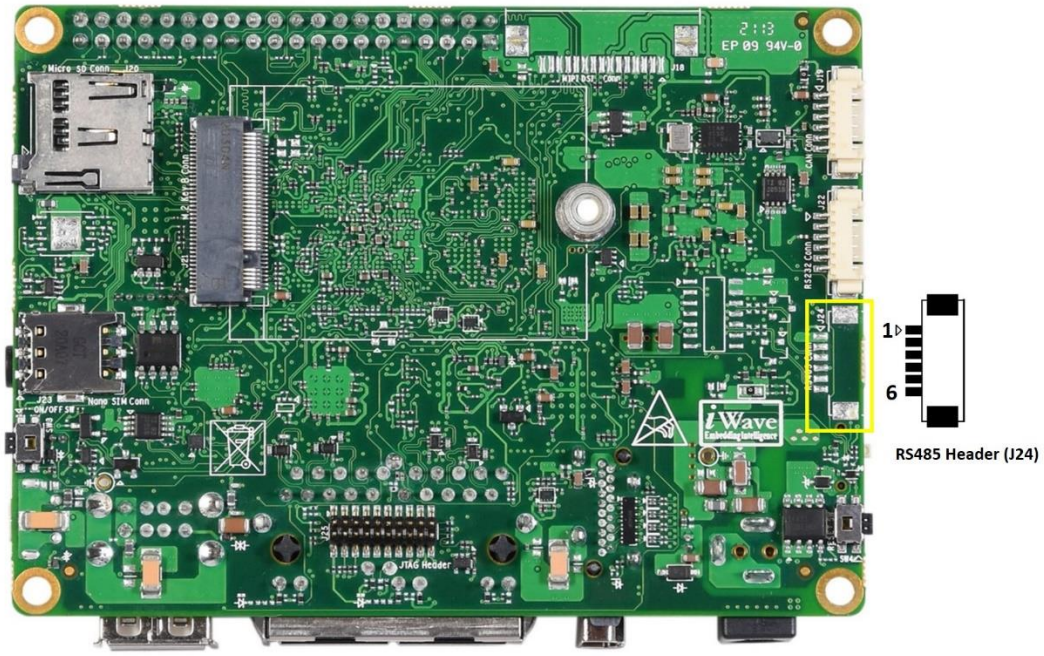

Figure 14: RS485 Header

Table 9: RS485 Data UART Header Pinout

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC	VCC_3V3	Power	3.3V Supply Voltage.
2	A	RS485_RXA	I, RS485	RS485 Receive (Complementary to B)
3	B	RS485_RXB	I, RS485	RS485 Receive (Complementary to A)
4	GND	GND	Power	Ground.
5	Z	RS485_TXZ	O, RS232	RS485 Transmit (Complementary to Y)
6	Y	RS485_TXY	O, RS232	RS485 Transmit (Complementary to Z)

Note: At a time either RS232 or RS485 can be supported. By default, RS485 is supported.

2.10 Audio/Video Features

2.10.1 MIPI CSI Connector

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports one 4-lane MIPI CSI 2.0 serial camera interface. The i.MX 8M Mini or i.MX 8M Nano SoC is compliant to D-PHY specification v1.2 and MIPI CSI2 Specification v1.3 except for C-PHY feature. The D-PHY interface Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The D-PHY interface Controller takes care of all packet formatting details and transmission over the MIPI bus.

Note: MIPI CSI Camera in i.MX 8M Mini or i.MX 8M Nano SBC can be supported through iWave's OV5640 MIPI Camera daughter Board.

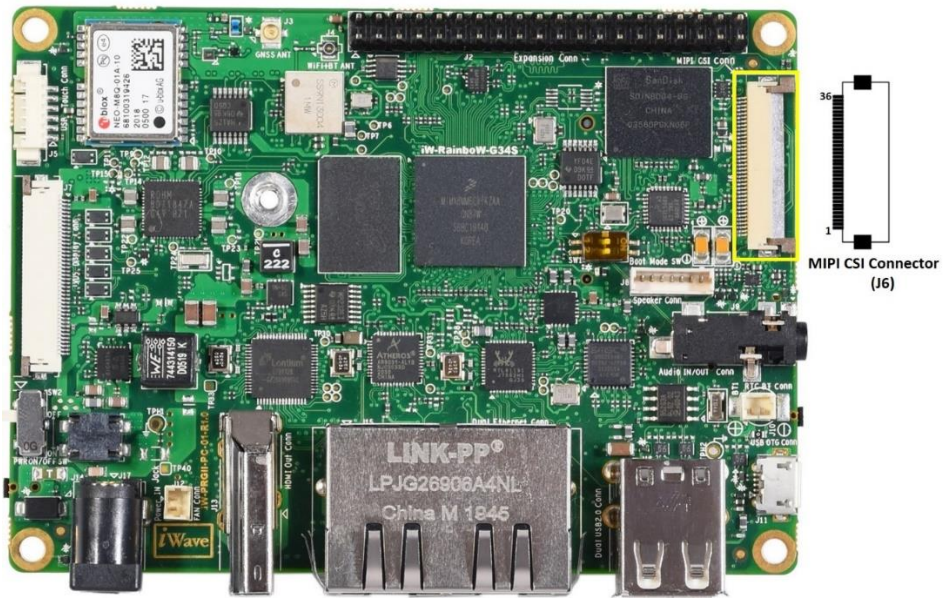

Figure 15: 36 pin MIPI CSI Connector

Number of Pins: 36

Connector Part : FH12A-36S-0.5SH(55) from Hirose Electric Co Ltd

Table 10: MIPI CSI Connector Pinouts

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	CAM_PWR	NA	Power	3V3 Camera Power
2	CAM_PWR	NA	Power	3V3 Camera Power
3	MIPI_CSI_DATA0_P	MIPI_CSI_D0_P/ B14	I, MIPI	MIPI CSI differential data lane 0 positive.
4	MIPI_CSI_DATA0_N	MIPI_CSI_D0_N/ A14	I, MIPI	MIPI CSI differential data lane 0 negative.
5	GND	NA	Power	Ground.
6	MIPI_CSI_DATA1_P	MIPI_CSI_D1_P/	I, MIPI	MIPI CSI differential data lane 1

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
		B15		positive.
7	MIPI_CSI_DATA1_N	MIPI_CSI_D1_N/ A15	I, MIPI	MIPI CSI differential data lane 1 negative.
8	GND	NA	Power	Ground.
9	MIPI_CSI_DATA2_P	MIPI_CSI_D2_P/ B17	I, MIPI	MIPI CSI differential data lane 2 positive.
10	MIPI_CSI_DATA2_N	MIPI_CSI_D2_N/ A17	I, MIPI	MIPI CSI differential data lane 2 negative.
11	CAM0_RST(GPIO3_06)	NAND_DATA00/ P23	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal
12	MIPI_CSI_DATA3_P	MIPI_CSI_D3_P/ B18	I, MIPI	MIPI CSI differential data lane 3 positive.
13	MIPI_CSI_DATA3_N	MIPI_CSI_D3_N/ A18	I, MIPI	MIPI CSI differential data lane 3 negative.
14	GND	NA	Power	Ground.
15	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P/ B16	I, MIPI	MIPI CSI differential Clock positive.
16	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N/ A16	I, MIPI	MIPI CSI differential Clock negative.
17	GND	NA	Power	Ground.
18	I2C2_SCL_1V8	NA	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI Camera.
19	I2C2_SDA_1V8	NA	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI Camera.
20	CAM0_EN(GPIO3_08)	NAND_DATA02/ K23	I, 1.8V CMOS/10K PU	Camera 0 Enable (active low).
21	MCLK (GPIO4_20)	SAI1_MCLK/ AB18	I, 1.8V CMOS	Master Clock.
22	NC	NA	-	NC.
23	NC	NA	-	NC.
24	NC	NA	-	NC.
25	GND	NA	Power	Ground.
26	NC	NA	-	NC.
27	NC	NA	-	NC.
28	GND	NA	Power	Ground.
29	NC	NA	-	NC.
30	NC	NA	-	NC.
31	NC	NA	-	NC.
32	NC	NA	-	NC.
33	NC	NA	-	NC.
34	GND	NA	Power	Ground.
35	CAM0_GPIO(GPIO3_07)	NAND_DATA02/ K24	I/O, 1.8V CMOS	GPIO for Camera 0
36	CAM1_GPIO(GPIO4_01)	SAI1_RXC/ AF16	I/O, 1.8V CMOS	GPIO for Camera 1

2.10.2 I2S Audio Interface

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports Audio IN/OUT through SoC's SAI5 interface which can support I2S format. This four wire I2S signals from the SoC is connected to I2S Audio Codec "SGTL5000" to support CTIA configuration Headphone Stereo output and Mono Mic input through Single 3.5mm audio Jack (J9).

The Audio IN/OUT Jack is physically located at the top of the board as shown below.

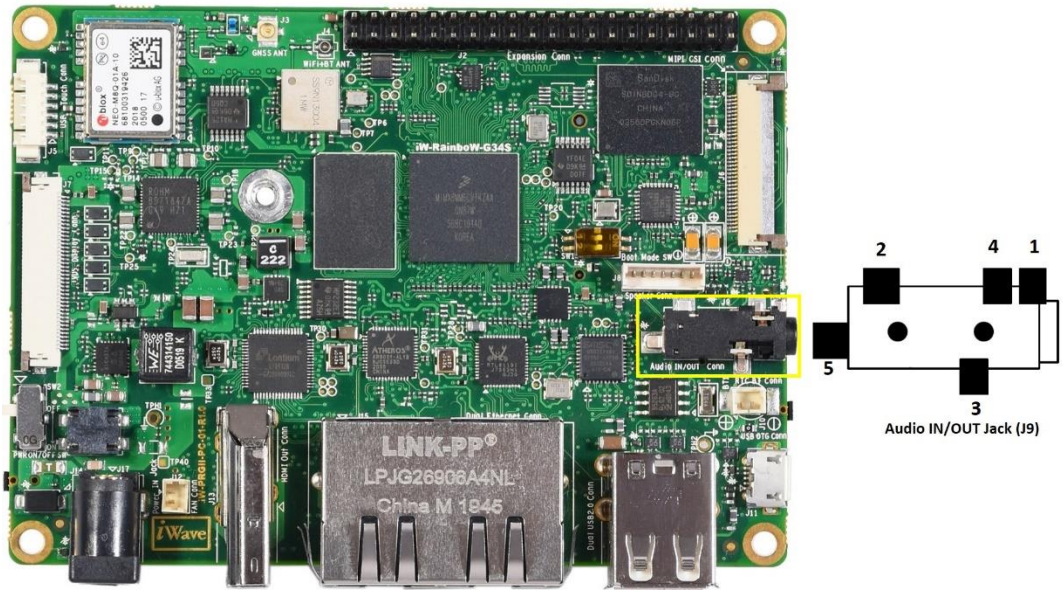

Figure 16: Audio IN/OUT Jack

2.10.3 Audio Amplifier

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports 3.2W Audio Amplifier. The LINEOUT signals from "SGTL5000" is connected to an Audio Amplifier. The Output signals from the Amplifier is connected to Speaker Header (J8). The Speaker Header is physically located at the top of the board as shown below.

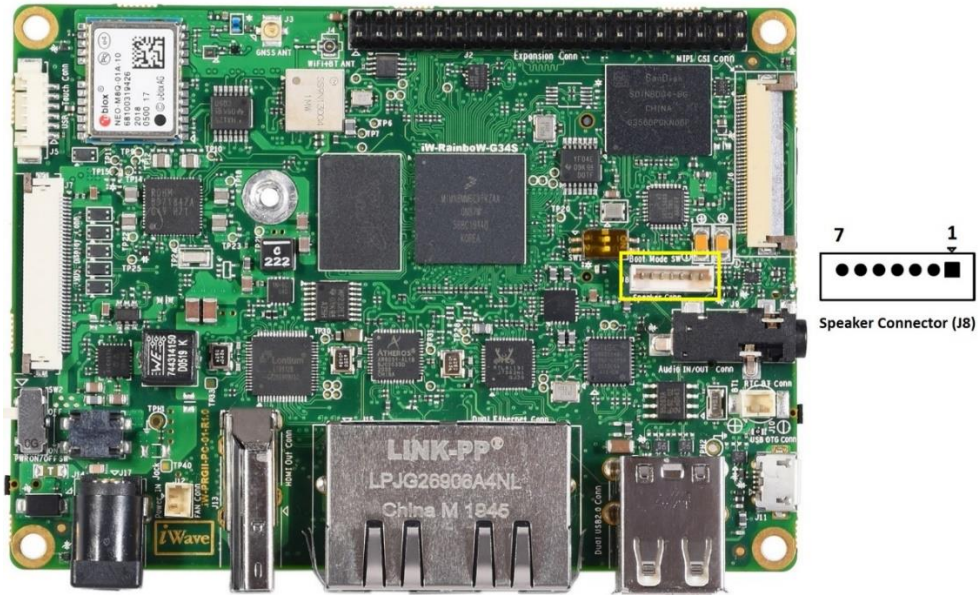

Figure 17: Speaker Header

Number of Pins : 7

Connector Part : 53047-0710 from Molex

Table 11: Speaker Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	LN_L	LINE_IN_L	I, Analog Audio	Line IN Left.
2	LN_R	LINE_IN_R	I, Analog Audio	Line IN Right
3	GND	GND	Power	Ground.
4	SPL+	SPKR_L+	O, Analog Audio	Speaker Left Positive.
5	SPL-	SPKR_L-	O, Analog Audio	Speaker Left Negative.
6	SPR+	SPKR_R+	O, Analog Audio	Speaker Right Positive.
7	SPR-	SPKR_R-	O, Analog Audio	Speaker Right Negative.

2.10.4 HDMI/LVDS Display Interface

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports LVDS or HDMI display through MIPI DSI to LVDS/HDMI Bridge. The MIPI_DSI to LVDS/HDMI Bridge (LT8912B) features a single-channel MIPI® D-PHY receiver with 4 data lanes per channel operating at 1.5Gbps per data lane and a maximum input bandwidth of 6Gbps. HDMI Signals from the bridge is connected to Standard HDMI Type-A Flag connector with ESD protection circuitry. HDMI Output connector (J13) is physically located on top of the board as shown below.

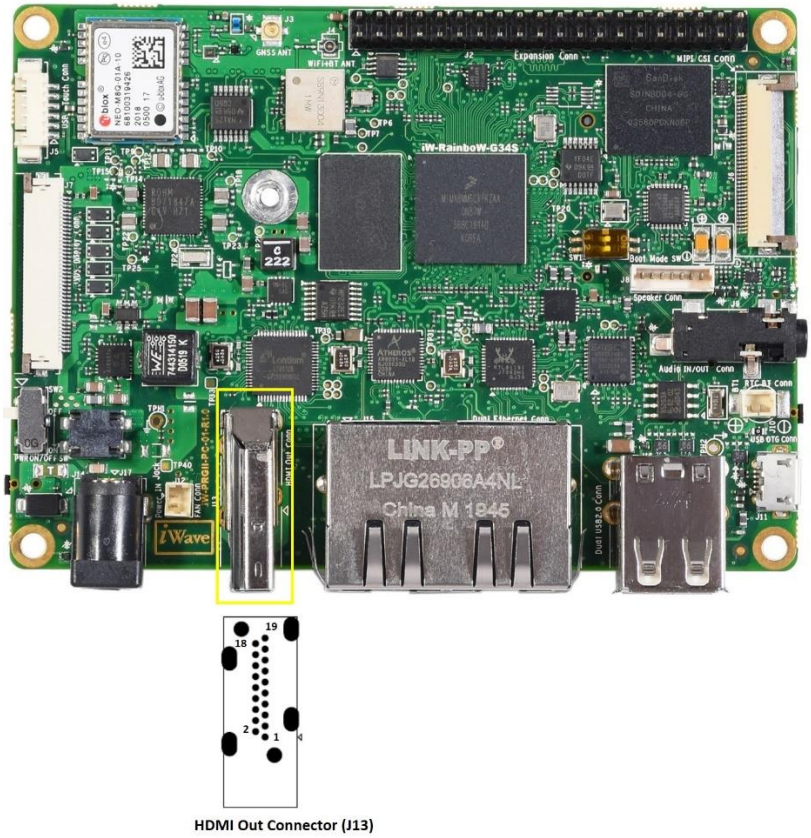

Figure 18: HDMI Out Connector

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports 10.1" LVDS display with USB touch. The LVDS Display (J7) and Touch Connectors (J5) are located at top side of the board as shown.

Number of Pins : 40

Connector Part : 541044033 from Molex

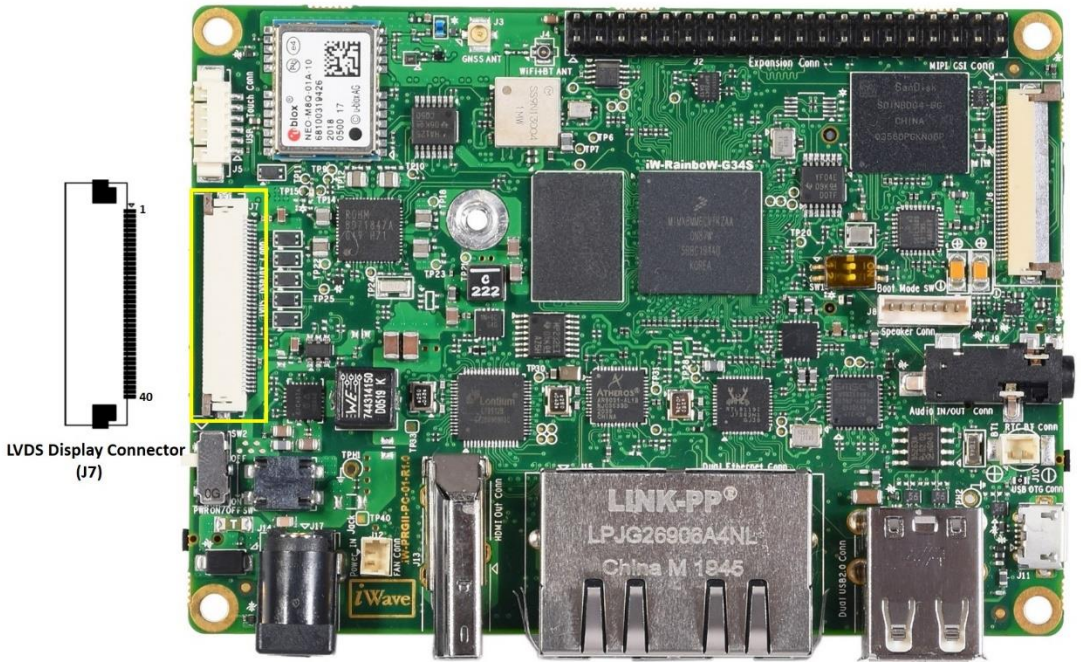

Figure 19: 40 pin LVDS Display Connector

Table 12: 40 Pin 10.1" LVDS Display Pinout

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	NC1	-	-	*NC*
2	VDD1	VCC_3V3	Power	3.3V Supply Voltage
3	VDD2	VCC_3V3	Power	3.3V Supply Voltage
4	NC2	-	-	*NC*
5	NC3	-	-	*NC*
6	NC4	-	-	*NC*
7	NC5	-	-	*NC*
8	LV0N-	LVDS_CH0_N	O, LVDS	LVDS Channel0 negative
9	LV0N+	LVDS_CH0_P	O, LVDS	LVDS Channel0 positive
10	GND1	GND	Power	Ground
11	LV1N-	LVDS_CH1_N	O, LVDS	LVDS Channel1negative
12	LV1N+	LVDS_CH1_P	O, LVDS	LVDS Channel1 positive
13	GND2	GND	Power	Ground
14	LV2N-	LVDS_CH2_N	O, LVDS	LVDS Channel2negative
15	LV2N+	LVDS_CH2_P	O, LVDS	LVDS Channel2 positive
16	GND3	GND	Power	Ground
17	LVCLK-	LVDS_CLK_N	O, LVDS	LVDS Channel0 clock negative
18	LVCLK+	LVDS_CLK_P	O, LVDS	LVDS Channel0 clock positive
19	GND4	GND	Power	Ground
20	LV3N-	LVDS_CH3_N	O, LVDS	LVDS Channel3negative
21	LV3N+	LVDS_CH3_P	O, LVDS	LVDS Channel3 positive
22	GND5	GND	Power	Ground
23	LED_GND1	GND	Power	Ground
24	LED_GND2	GND	Power	Ground
25	LED_GND3	GND	Power	Ground

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
26	NC6	-	-	*NC*
27	LED_PWM	PWM1_OUT(GPIO5_21)	O, 3.3V	PWM control signal
28	LED_EN	GPIO_LVDS_BLEN(GPIO5_05)	O, 3.3V	Backlight Enable signal
29	NC7	-	-	*NC*
30	NC8	-	-	*NC*
31	LED_VCC1	VCC_12V_LVDS	Power	12V Supply Voltage
32	LED_VCC2	VCC_12V_LVDS	Power	12V Supply Voltage
33	LED_VCC3	VCC_12V_LVDS	Power	12V Supply Voltage
34	NC9	-	-	*NC*
35	BIST	-	-	*NC*
36	NC10	-	-	*NC*
37	NC11	-	-	*NC*
38	NC12	-	-	*NC*
39	NC13	-	-	*NC*
40	NC14	-	-	*NC*

2.10.5 USB Touch Connector

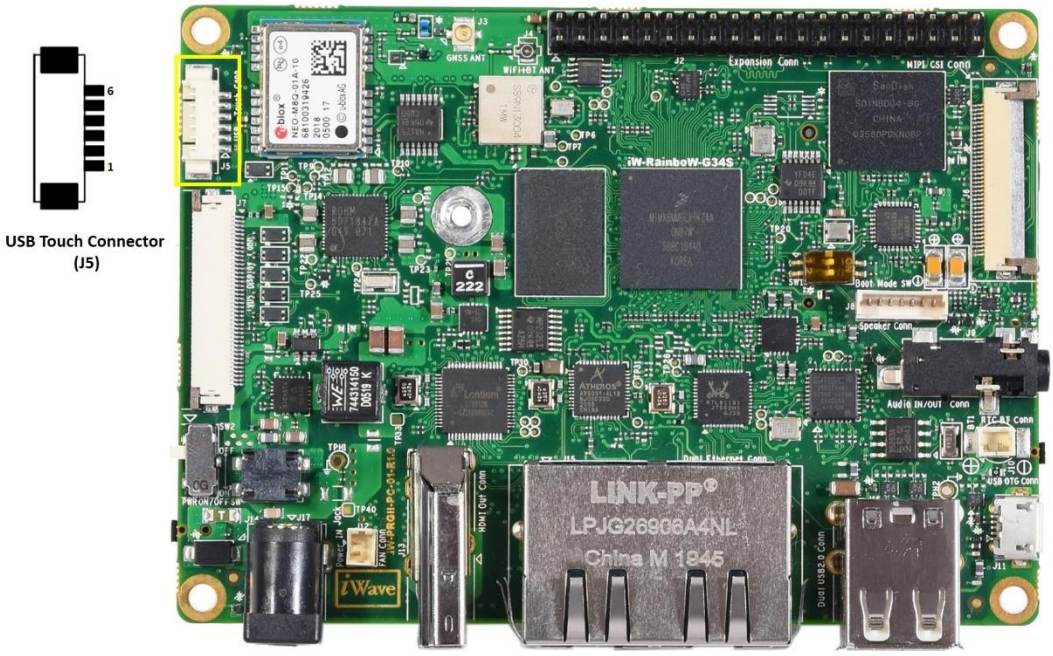

Figure 20: USB Touch Connector

Number of Pins : 6

Connector Part : 532610671 from Molex

Table 13: LVDS Display Touch Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	1	VBUS_HOST_TP	Power	Supply Voltage.
2	2	USB_HUB3OUT_DP	I, USB	Differential USB Positive.
3	3	USB_HUB3OUT_DM	I, USB	Differential USB Negative.
4	4	NC	-	NC.
5	5	GND	Power	Ground.
6	6	NC	-	NC.

2.10.6 MIPI DSI Display (Optional)

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC optionally supports 2-lane MIPI DSI Display. By default, MIPI DSI signals are connected to MIPI_DSI to LVDS/HDMI Bridge.

Number of Pins : 15

Connector Part : 1-84952-5 from TE Connectivity AMP Connectors

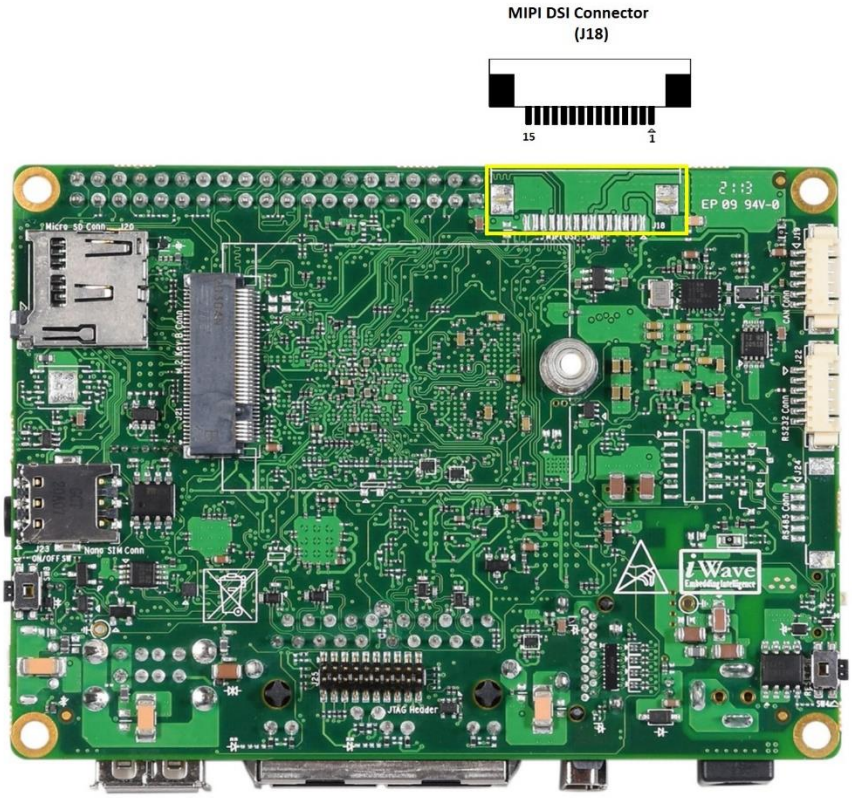

Figure 21: MIPI DSI Connector

Table 14: MIPI DSI Connector Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND1	GND	Power	Ground.
2	DATA1-	MIPI_DSI_DATA1_N	O, MIPI	MIPI DSI differential data lane 1negative
3	DATA1+	MIPI_DSI_DATA1_P	O, MIPI	MIPI DSI differential data lane 1 positive
4	GND2	GND	Power	Ground.
5	CLK-	MIPI_DSI_CLK_N	O, MIPI	MIPI DSI differential Clock negative
6	CLK+	MIPI_DSI_CLK_P	O, MIPI	MIPI DSI differential Clock positive
7	GND3	GND	Power	Ground.
8	DATA0-	MIPI_DSI_DATA0_N	O, MIPI	MIPI DSI differential data lane 0negative
9	DATA0+	MIPI_DSI_DATA0_P	O, MIPI	MIPI DSI differential data lane 0 positive
10	GND4	GND	Power	Ground.
11	SCL	I2C3_SCL(GPIO5_19)	I,3.3V CMOS/4.7K PU	I2C Clock.
12	SDA	I2C3_SDA(GPIO5_18)	IO,3,3V CMOS/4.7K PU	I2C Data
13	GND5	GND	Power	Ground.
14	VCC1	VCC_3V3	Power	3.3V Supply Voltage.
15	VCC2	VCC_3V3	Power	3.3V Supply Voltage.

2.11 M.2 Key B Connector

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports M.2 B key socket. M.2 B key socket is the Next Generation Form Factor (NGFF) which is designed to support multiple modules and make the M.2 more suitable in application like solid-state storage, WWAN. The M.2 Key B Connector supports PCIe ×1(Optional), USB 2.0, audio, UIM, I2C and SMBus. The M.2 Key-B Connector (J21) is placed at the bottom side of the board.

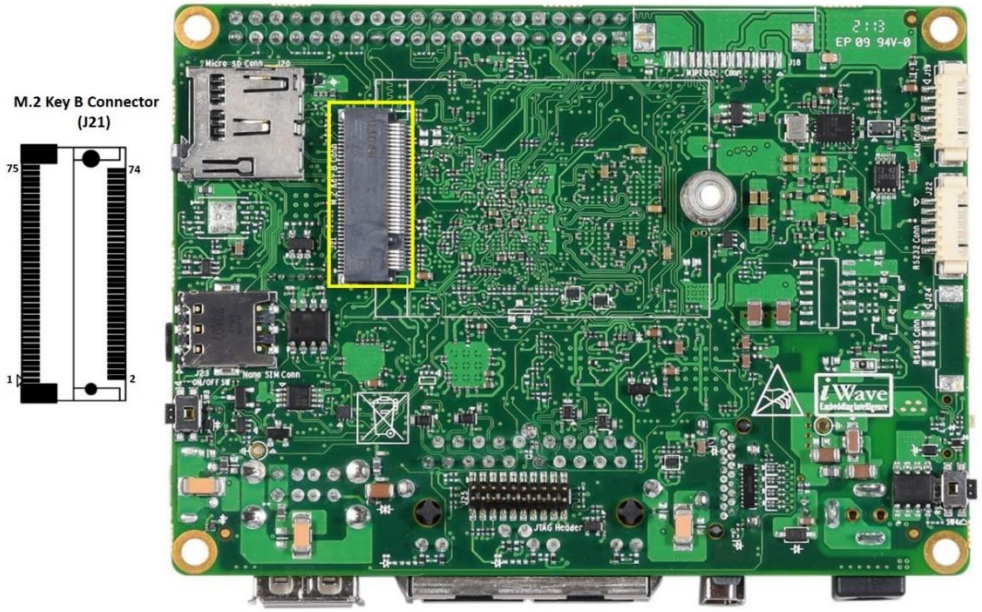

Figure 22: M.2 Key B Connector

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports a Nano SIM connector to support the WWAN M.2 Modules. The Nano SIM connector (J23) is physically located on the bottom of the board.

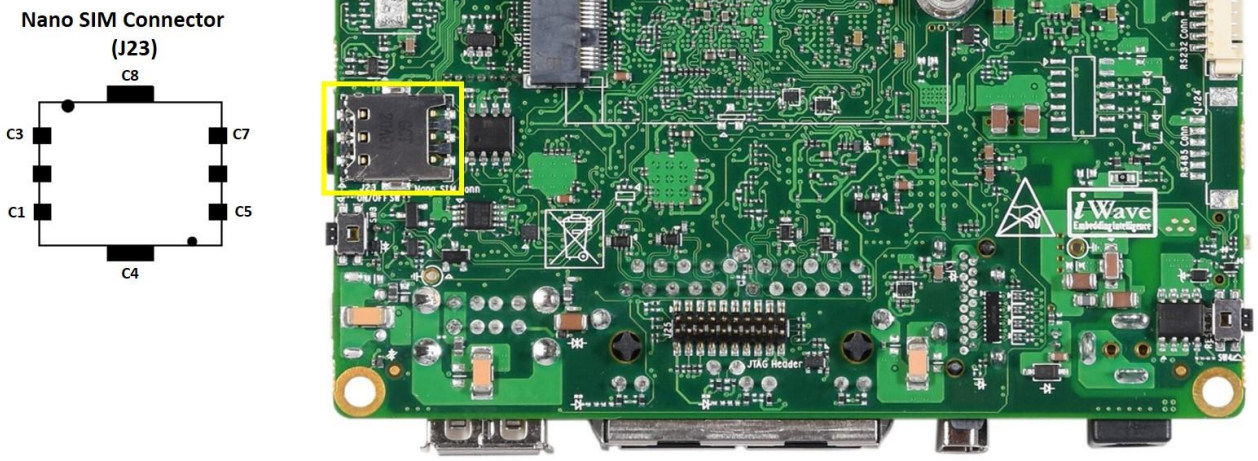

Figure 23: Nano SIM Connector

Table 15: M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	M.2_PWR_OFF#	O, 3.3V CMOS	M.2 Full card Power off Signal.
7	USB_D+	M.2_USB_D+	IO, USB	USB2.0 Port0 Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	M.2_W_DISABLE1#	O, 3.3V CMOS	M.2 Wireless Disable Signal
9	USB_D-	M.2_USB_D-	IO, USB	USB2.0 Port0 Data Minus.
10	GPIO9(LED1#/DAS_DSS#) (I/0)(0/3.3V)	M.2_LED	O, 3.3V CMOS	Provide status indicators via LED.
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	M.2_SAI1_TXC	IO, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel1 Clock
21	CONFIG_0	M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	M.2_SAI1_RXD0	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	NC	NC	NC.
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	M.2_SAI1_TXD0	O, 1.8V CMOS	Serial Audio Interface Channel1 Data Output
25	DPR (O) (0/1.8V)	M.2_DPR	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	NC	NC	NC.
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	M.2_SAI1_TXFS	IO, 1.8V CMOS	Serial Audio Interface Channel1 Left Right Clock
29	PERN1/USB30_RX-/SSIC_RX-	NC	NC	NC.
30	UIM-RESET (I)	M2_UIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	NC	NC	NC.
32	UIM-CLK (I)	M2_UIM_CLK	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	M2_UIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NC	NC.
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NC	NC.
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_S	I2C2_SCL_1V8	O, 1.8V CMOS	I2C CLK.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
	CL/SIM_DET2)(I/O)(0/1.8 V)			
41	PERN0/SATA_B+	PCIE_RXN	I,PCIe/SATA	PCIe Port 0 Receive Lane Positive. *Note: Optionally connected*
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	I2C2_SDA_1V8	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	PCIE_RXP	I,PCIe/SATA	PCIe Port 0 Receive Lane Negative. *Note: Optionally connected*
44	GPIO2_(ALERT# /GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	GPIO_SMBUS_ALERT (GPIO2_11)	IO, 1.8V CMOS	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/ UIM_RST2) (I/O)(0/1.8V)	M.2_GPIO3(GPIO5_24)	IO, 1.8V CMOS	General Purpose Input Output.
47	PETN0/SATA_A-	PCIE_TXN	O,PCIe/SATA	PCIe Port 0 Transmit Lane Negative. *Note: Optionally connected*
48	GPIO4(TX_BLK/GNSS_1/ UIM_PWR2)(I/O)(0/1.8V)	M.2_GPIO4(GPIO4_22)	IO, 1.8V CMOS	General Purpose Input Output.
49	PETP0/SATA_A+	PCIE_TXP	O,PCIe/SATA	PCIe Port 0 Transmit pair Negative. *Note: Optionally connected*
50	PERST# (O)(0/3.3V)	PCIE_M.2_RST	O, 3.3V CMOS	PCIe Resets Signal.
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	M.2_CLKREQ	IO, 3.3V CMOS	M.2 Clock Request Pin
53	REFCLKN	PCIE_REFCLK_DM	O,PCIe	PCIe Channel-A Clock Positive. *Note: Optionally connected from External Oscillator.*
54	PEWAKE# (I/O)(0/3.3V)	PCIE_WAKE_B(GPIO1_07)	O, 3.3V CMOS	PCIe Wake Signal
55	REFCLKP	PCIE_REFCLK_DP	O,PCIe	PCIe Channel-A Clock Negative. *Note: Optionally connected from External Oscillator.*
56	MFG_DATA	I2C2_SDA	IO, 3.3V CMOS	NC. *Optionally connected I2C Data.*
57	GND	GND	Power	Ground.
58	MFG_CLOCK	I2C2_SCL	O, 3.3V CMOS	NC. *Optionally connected I2C Clock.*
59	ANTCTL0 (I)(0/1.8 V)	NC	NC	NC.
60	COEX3 (I/O)(0/1.8V)	NC	NC	NC.
61	ANTCTL1 (I)(0/1.8 V)	NC	NC	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
62	COEX_TXD (O)(0/1.8V)	NC	NC	NC.
63	ANTCTL2 (I)(0/1.8 V)	NC	NC	NC.
64	COEX_RXD (I)(0/1.8V)	NC	NC	NC.
65	ANTCTL3 (I)(0/1.8 V)	NC	NC	NC.
66	SIM_DETECT (I)	M.2_SIM_DETECT	NC	NC
67	RESET# (O)(0/1.8V)	M.2_RESET(GPIO5_25)	I, 1.8V	M.2 Reset Signal
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK	I, 32.768kHz Clock Supply	*Note: Optionally connected 32.768kHz Clock output*
69	CONFIG_1	M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

Below are the steps for Inserting an M.2 Key B Module to the i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC M.2 Connector

Step 1: Move the Module against housing Chamber.

Step 2: Rotate the Module to 25 Degree and insert until the bottom of the module surface reaches the ramp.

Step 3: Rotate the Module to horizontal Position by hand

Step 4: Fix the module with M3 x4 Screw

Figure 24: M.2 Module Insertion Guide

2.12 Expansion Connector

The interfaces which are available at 40 Pin Expansion connector are explained in the following section. This Expansion Connector (J2) is physically located at the top of the SBC as shown below.

Number of Pins : 40

Connector Part : 61304021121 from Wurth Electronics Inc

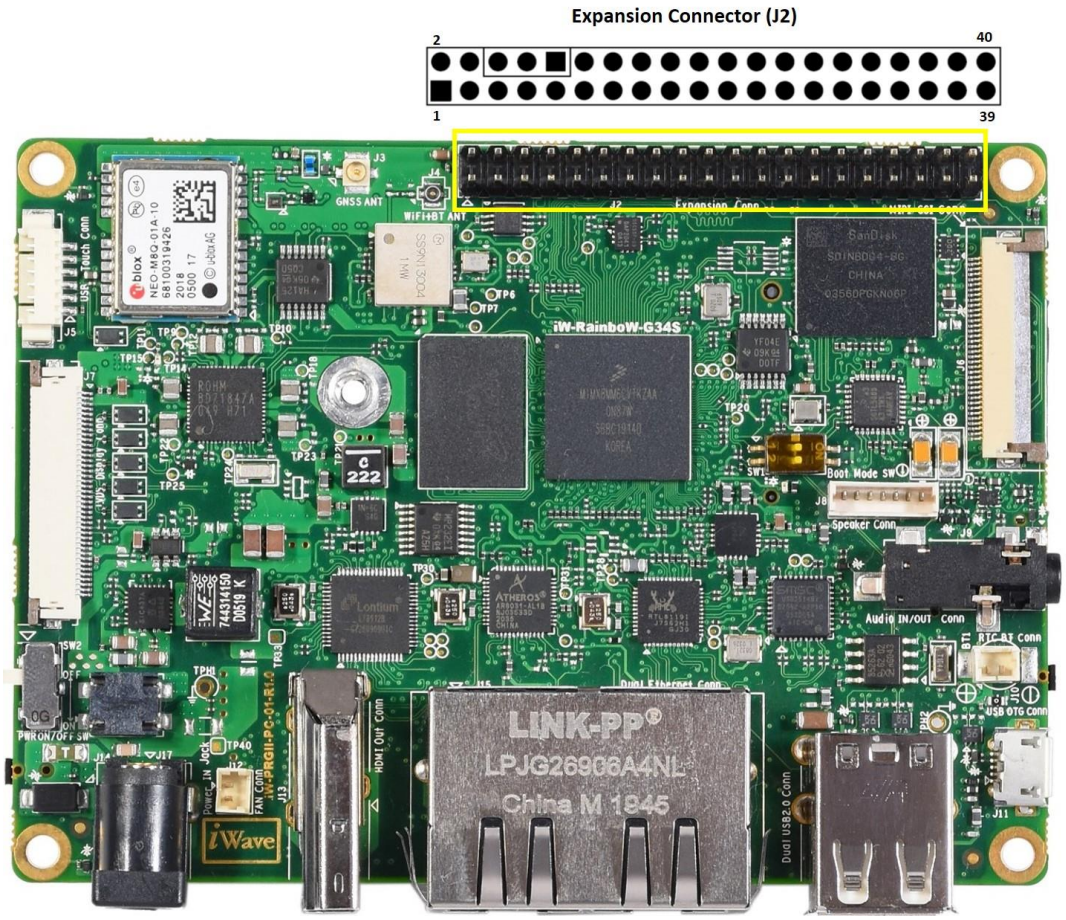

Figure 25: Expansion Connector

Table 16: Expansion Connector Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_3V3	-	Power	3.3V Power Supply
2	VCC_5V	-	Power	5V Power Supply
3	I2C3_SDA(GPIO5_18)	I2C3_SDA/F10	IO, 3.3V CMOS/4.7K PU	I2C Data
4	VCC_5V	-	Power	5V Power Supply
5	I2C3_SCL(GPIO5_19)	I2C3_SCL/E10	O, 3.3V CMOS/4.7K PU	I2C Clock
6	GND	-	Power	Ground
7	GPIO5_IO1(GPIO5_1)	SAI3_TXD/AF6	IO, 3.3V	For i.MX 8M Nano used as GPIO for USB Switch

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
8	B_UART4_TX(GPIO5_29)	UART4_TX/F18	O, 3.3V	Debug UART Transmit
9	GND	-	Power	Ground
10	B_UART4_RX(GPIO5_28)	UART4_RX/F19	I, 3.3V	Debug UART Receive
11	CEC(GPIO1_3)	GPIO1_IO03/AF13	IO, 3.3V	Optional *By default used CEC for HDMI*
12	SAI6_TX_BCLK(GPIO4_16)	SAI1_TXD4/AG22	IO, 1.8V	*NC in i.MX 8M Nano SBC*
13	ENET_INT(GPIO3_19)	SAI5_RXFS/AB15	IO, 3.3V	Optional *By default used as Interrupt for Ethernet*
14	GND	-	Power	Ground
15	GPIO4_00	SAI1_RXFS/AG16	IO, 1.8V	Not supported in i.MX 8M Nano SBC
16	UART3_RX(GPIO5_06)	ECSPI1_SCLK/D6	I, 3.3V	Optional *By default used for GNSS module*
17	VCC_3V3	-	Power	3.3V Power Supply
18	UART3_TX(GPIO5_07)	ECSPI1_MOSI/B7	O, 3.3V	Optional *By default used for GNSS module*
19	ECSPI2_MOSI(GPIO5_11)	ECSPI2_MOSI/B8	O, 3.3V	Optional *By default connected to CAN FD Controller*
20	GND	-	Power	Ground
21	ECSPI2_MISO(GPIO5_12)	ECSPI2_MOSI/A8	I, 3.3V	Optional *By default connected to CAN FD Controller*
22	MCLK (GPIO4_20)	SAI1_MCLK/AB18	O, 1.8V	Also connected to MIPI_CSI Connector *NC in i.MX 8M Nano SBC*
23	ECSPI2_SCLK(GPIO5_10)	ECSPI2_SCLK/E6	O, 3.3V	Optional *By default connected to CAN FD Controller*
24	ECSPI2_SS0(GPIO5_13)	ECSPI2_SS0/A6	I, 3.3V	Optional *By default connected to CAN FD Controller*
25	GND	-	Power	Ground
26	M.2_W_DISABLE1#(GPIO5_08)	ECSPI1_MISO/A7	IO, 3.3V	Optional *By default connected to M.2 Connector*
27	EX_WDTRIG_B	-	-	Watchdog
28	I2C2_SCL	I2C2_SCL/D10	O, 3.3V/4.7K PU	I2C Clock
29	GPIO5_04(GPIO 5)	SPDIF_RX/AG9	IO, 3.3V	General purpose IO
30	GND	-	Power	Ground
31	CAM1_GPIO(GPIO4_01)	SAI1_RXC/AF16	IO, 1.8V	*NC in i.MX 8M Nano SBC*
32	GPIO5_20(PWM2_OUT)	I2C4_SCL/D13	IO, 3.3V	General purpose IO
33	PWM1_OUT(GPIO5_21)	I2C4_SDA/E13	IO, 3.3V	Optional *By default used as PWM for LVDS Display*

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
34	GND	-	Power	Ground
35	SAI6_TX_SYNC(GPIO4_18)	SAI1_TXD6/AG23	O, 1.8V	*NC in i.MX 8M Nano SBC*
36	UART3_RTS(GPIO5_09)	ECSPI1_SS0/B6	O, 3.3V	Optional *By default used as GPIO for Audio Jack detection*
37	GPIO1_15	GPIO1_IO15/AB9	IO, 3.3V	Optional *By default used as GPIO for Audio Jack detection*
38	SAI6_TX_DATA0(GPIO4_17)	SAI1_TXD5/AF22	O, 1.8V	*NC in i.MX 8M Nano SBC*
39	GND	-	Power	Ground
40	SAI6_RX_DATA0(GPIO4_07)	SAI1_RXD4/AG18	I, 1.8V	*NC in i.MX 8M Nano SBC*

*Note: Refer GPIO Column under **"i.MX 8M Mini Pin Multiplexing on Expansion Connector" & "i.MX 8M Nano Pin Multiplexing on Expansion Connector"** for details on GPIO options available from Expansion connector.*

2.13 Other Features

2.13.1 Fan Header

The i.MX 8 QM/QP Pico ITX SBC supports a Fan Header to connect cooling Fan if required. This Fan Header (J12) is physically located at the top of the board as shown below.

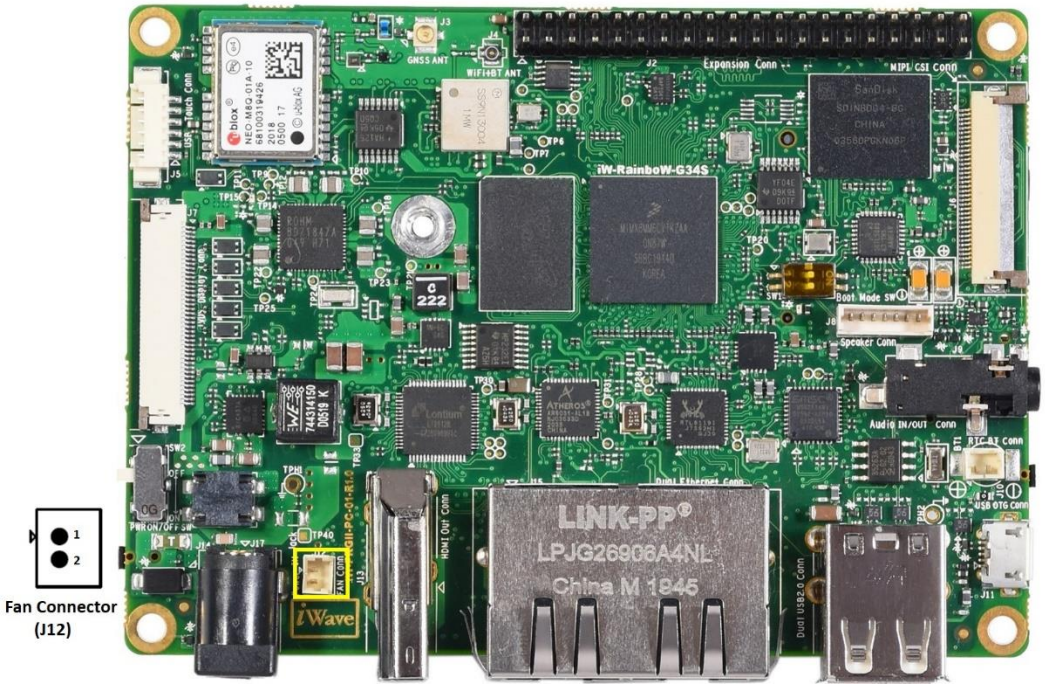

Figure 26: Fan Connector

Number of Pins : 2

Connector Part : 10114829-10102LF from Amphenol ICC (FCI)

Table 17: Fan Connector Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN. *Note: Optionally connected to 12V Power.*
2	GND	Power	Ground.

Note: Contact iWave support team if 12V Power Support is required for FAN Header support is required

2.13.2 RTC Controller with RTC Battery Header

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports external RTC Controller “PCF85263” for Real time clock support. This external RTC Controller IC (U27) is connected to i.MX 8M Mini SoC through I2C1 Interface and operates at 3.3V voltage level.

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports external RTC cell. The SBC supports 2pin connector for backup battery or coin cell connection. The 2pin RTC (J10) battery connector is physically located on top side of the SBC as shown below.

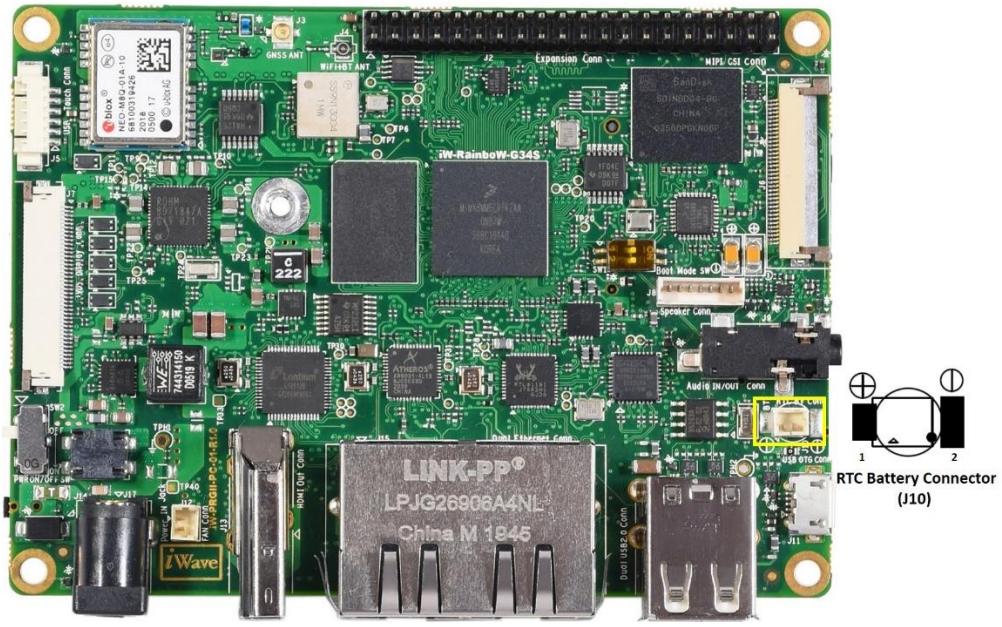

Figure 27: RTC Battery Connector

Number of Pins : 2

Connector Part : 10114829-10102LF from Amphenol ICC (FCI)

Table 18: RTC Battery Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VRTC_3V0	I, Power	+3V Power Input to RTC Controller
2	GND	Power	Ground.

Note: Contact iWave support team if External RTC Controller support is required.

2.13.3 JTAG Interface

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports JTAG interface for CPU debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security.

JTAG Header (J25) is physically located on bottom side of the board.

Number of Pins - 20

Connector Part - 62132021021 from Wruth Electronics.

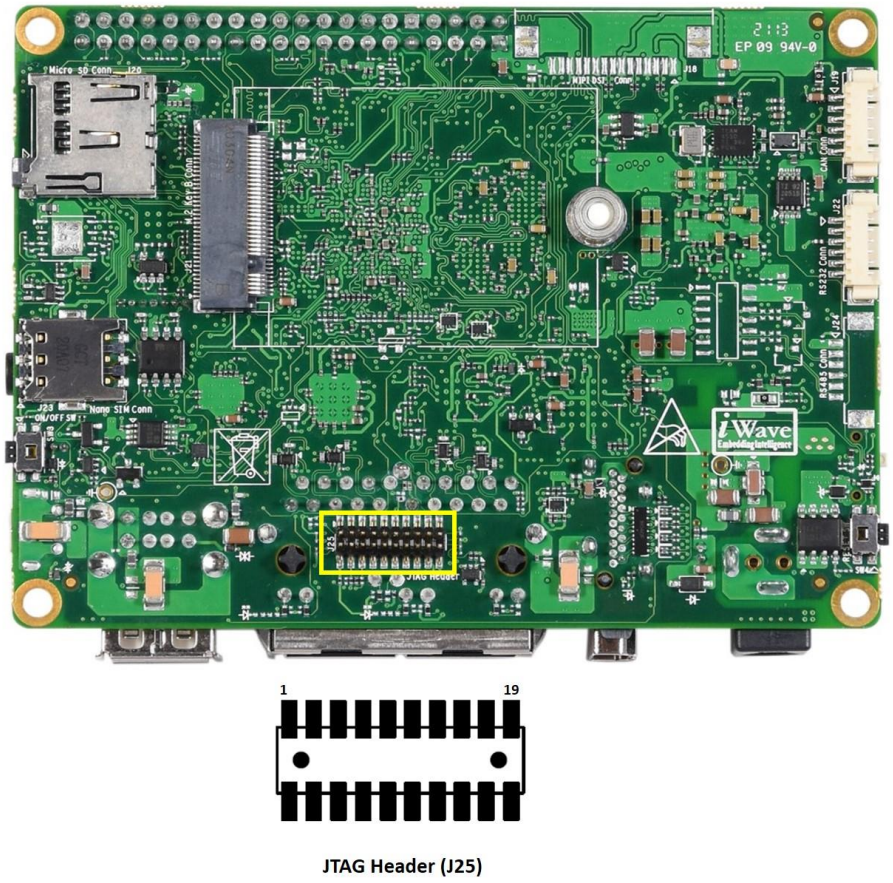

Figure 28: JTAG Header

Table 19: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	NVCC_3V3	O, 3.3V Power	VTREF Voltage Reference.
2	NVCC_3V3	O, 3.3V Power	Supply Voltage.
3	JTAG_TRSTB	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	Power	Ground. *Note: Optionally connected to UART3_TX_M4*
5	JTAG_TDI	I, 3.3V CMOS	JTAG test data input.
6	GND	Power	Ground. *Note: Optionally connected to SCU_UART0_RX*
7	JTAG_TMS	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
8	GND	Power	Ground.
9	JTAG_TCK	I, 3.3V CMOS/ 10K PD	JTAG test Clock.
10	GND	Power	Ground.
11	-	-	Only pull down is provided.

Pin No	Signal Name	Signal Type/ Termination	Description
12	GND	Power	Ground.
13	JTAG_TDO	O, 3.3V CMOS	JTAG test data output.
14	GND	Power	Ground.
15	JTAG_RESETB	I, 3.3V CMOS/ 10K PU	Reset input.
16	GND	Power	Ground.
17	-	-	Only pull up is provided.
18	GND	Power	Ground.
19	-	-	Only pull down is provided.
20	GND	Power	Ground.

2.13.4 Power ON/OFF Switch

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC has power ON/OFF switch (SW2) to control the Main power Input ON/OFF functionality. The Power ON/OFF switch is physically located at the top of the board as shown below.

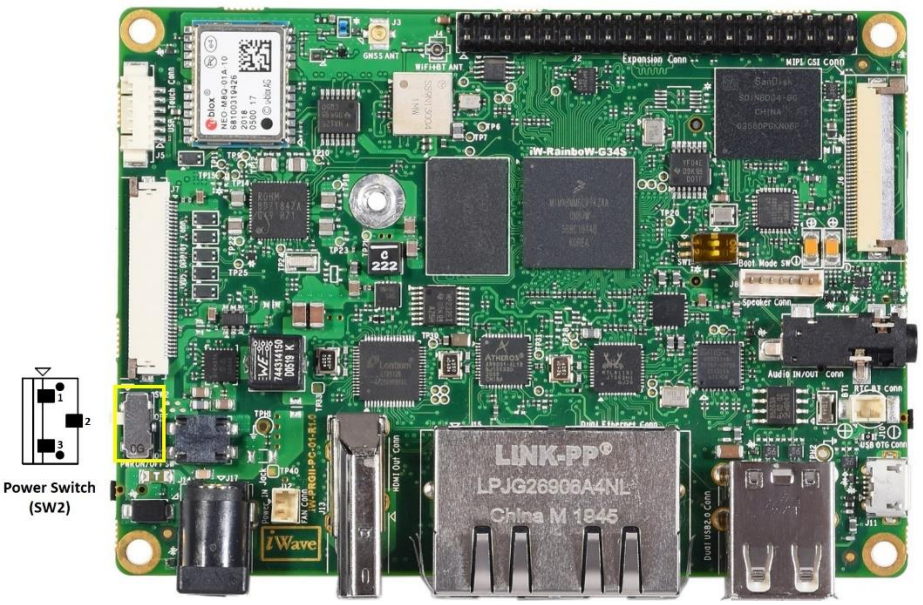

Figure 29: Power ON/OFF Switch

2.13.5 Reset Switch

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports Push button switch (SW4) to reset the i.MX 8M Mini or i.MX 8M Nano CPU. Reset signal is directly connected from Reset Push button switch. This Reset Push button switch (SW4) is physically located at the bottom of the board as shown below.

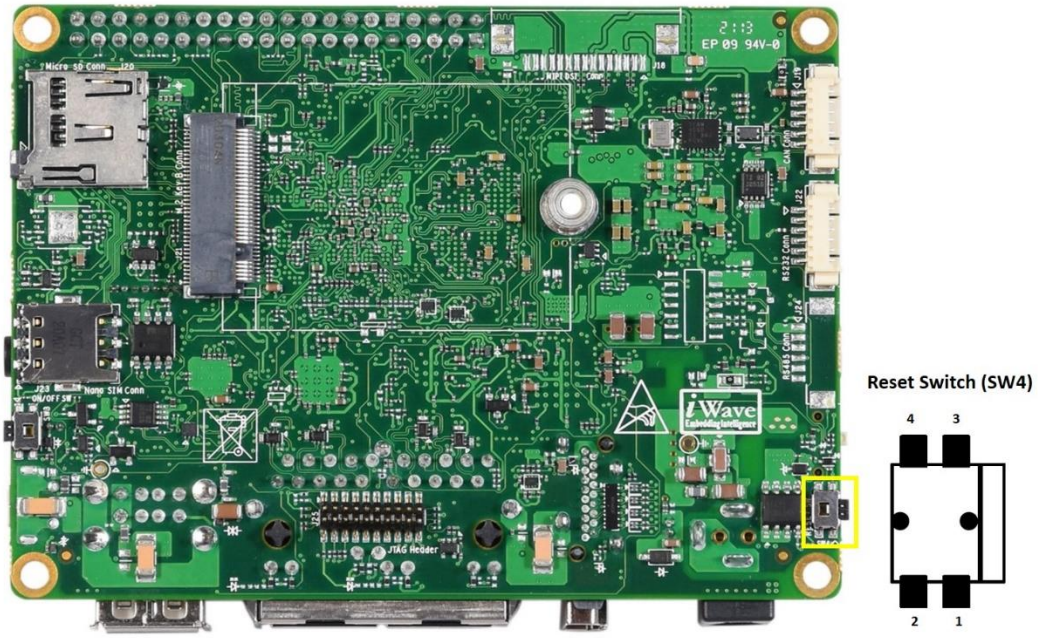

Figure 30: Reset Switch

2.13.6 CPU ON/OFF Switch

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports Push button switch (SW3) for ON OFF the i.MX 8M Mini or i.MX 8M Nano CPU. ON/OFF is directly connected from ON/OFF Push button switch. This ON/OFF Push button switch (SW3) is physically located at the bottom of the board as shown below.

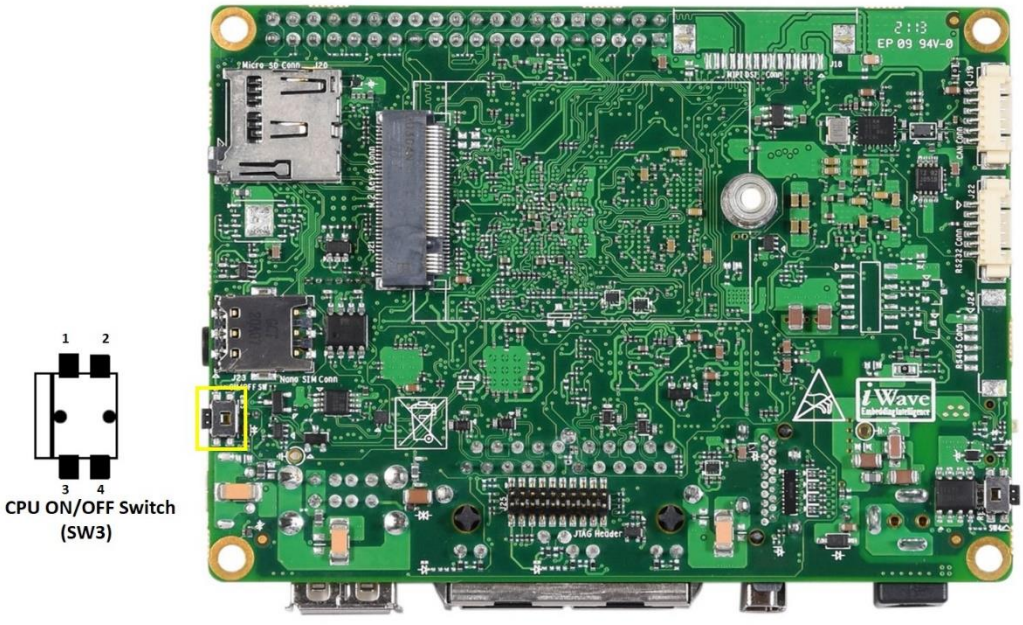

Figure 31: CPU ON/OFF Switch

2.14 i.MX 8M Mini Pin Multiplexing on Expansion Connector

The i.MX 8M Mini SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M Mini SOC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8M Mini SoC pin connections to the Expansion Connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M Mini Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in SBC for iWave's BSP reusability.

Table 20: i.MX 8M Mini CPU IOMUX for Expansion Connector interfaces

Interface/ Function	Exp. Conn. Pin Number	i.MX 8M Mini CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
ECSPI2	23	E6	ecspi2.SCLK	uart4.RX				gpio5.IO[10]		gpio5.IO[10]
	19	B8	ecspi2.MOSI	uart4.TX				gpio5.IO[11]		gpio5.IO[11]
	21	A8	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]		gpio5.IO[12]
	24	A6	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]		gpio5.IO[13]
PWM	32	D13	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]		gpio5.IO[20]
	33	E13	i2c4.SDA	pwm1.OUT				gpio5.IO[21]		gpio5.IO[21]
I2C2	28	D10	i2c2.SCL	enet1.1588_EVENT1_IN	usdhc3.CD_B			gpio5.IO[16]		gpio5.IO[16]
	27	D9	i2c2.SDA	enet1.1588_EVENT1_OUT	usdhc3.WP			gpio5.IO[17]		gpio5.IO[17]
I2C3	3	E10	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]		gpio5.IO[18]
	5	F10	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]		gpio5.IO[19]
UART3	16	D6	ecspi1.SCLK	uart3.RX				gpio5.IO[6]		gpio5.IO[6]
	18	B7	ecspi1.MOSI	uart3.TX				gpio5.IO[7]		gpio5.IO[7]
	36	B6	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]		gpio5.IO[9]
UART4	10	F19	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]		gpio5.IO[28]
	8	F18	uart4.TX	uart2.RTS_B				gpio5.IO[29]		gpio5.IO[29]
SAI1	38	AF22	sai1.TX_DATA[5]	sai6.RX_DATA[0]	sai6.TX_DATA[0]		coresight.TRACE[13]	gpio4.IO[17]		gpio4.IO[18]
	40	AG18	sai1.RX_DATA[4]	sai6.TX_BCLK	sai6.RX_BCLK		coresight.TRACE[4]	gpio4.IO[6]		gpio4.IO[16]
	35	AG23	sai1.TX_DATA[6]	sai6.RX_SYNC	sai6.TX_SYNC		coresight.TRACE[14]	gpio4.IO[18]	sai1.TX_DATA[6]	gpio4.IO[18]
	12	AG22	sai1.TX_DATA[4]	sai6.RX_BCLK	sai6.TX_BCLK		coresight.TRACE[12]	gpio4.IO[16]	sai1.TX_DATA[4]	gpio4.IO[16]
GPIOs	7	AF6	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]		gpio5.IO[1]
	11	AF13	gpio1.IO[3]	usdhc1.VSELECT				sdma1.EXT_EVENT[0]		gpio1.IO[3]

Interface/ Function	Exp. Conn. Pin Number	i.MX 8M Mini CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	13	AB15	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]	sai5.RX_SYNC	gpio3.IO[19]
	15	AG16	sai1.RX_SYNC	sai5.RX_SYNC			coresight.TRACE_CLK	gpio4.IO[0]	sai1.RX_SYNC	gpio4.IO[0]
	29	AG9	spdif1.IN	pwm2.OUT				gpio5.IO[4]	spdif1.IN	gpio5.IO[4]
	31	AF16	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio4.IO[1]	sai1.RX_BCLK	gpio4.IO[1]
	37	AB9	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT	ccmsrcgpcmix.CLKO2	gpio1.IO[15]

Important Note: The SAI1 signals which is having Boot configuration functionality in Funtion6 -BOOT_CFG[0:15] are also used for i.MX 8M Mini SoC boot media setting on SBC and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot media configurations.

2.15 i.MX 8M Nano Pin Multiplexing on Expansion Connector

The i.MX 8M Nano SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M Nano SOC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8M Nano SoC pin connections to the Expansion connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M Nano Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SBC for iWave's BSP reusability

Table 21: i.MX 8M Nano CPU IOMUX for Expansion Connector interfaces

Interface/ Function	Exp. Conn. Pin Number	i.MX8M Nano CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
ECSPI2	23	E6	ecspi2.SCLK	uart4.RX				gpio5.IO[10]		gpio5.IO[10]
	19	B8	ecspi2.MOSI	uart4.TX				gpio5.IO[11]		gpio5.IO[11]
	21	A8	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]		gpio5.IO[12]
	24	A6	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]		gpio5.IO[13]
PWM	32	D13	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]		gpio5.IO[20]
	33	E13	i2c4.SDA	pwm1.OUT				gpio5.IO[21]		gpio5.IO[21]
I2C2	28	D10	i2c2.SCL	enet1.1588_EVENT1_IN	usdhc3.CD_B			gpio5.IO[16]		gpio5.IO[16]
	27	D9	i2c2.SDA	enet1.1588_EVENT1_OUT	usdhc3.WP			gpio5.IO[17]		gpio5.IO[17]
I2C3	3	E10	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]		gpio5.IO[18]
	5	F10	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]		gpio5.IO[19]
UART3	16	D6	ecspi1.SCLK	uart3.RX				gpio5.IO[6]		gpio5.IO[6]
	18	B7	ecspi1.MOSI	uart3.TX				gpio5.IO[7]		gpio5.IO[7]
	36	B6	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]		gpio5.IO[9]
UART4	10	F19	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]		gpio5.IO[28]
	8	F18	uart4.TX	uart2.RTS_B				gpio5.IO[29]		gpio5.IO[29]
GPIOs	7	AF6	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]		gpio5.IO[1]
	11	AF13	gpio1.IO[3]	usdhc1.VSELECT				sdma1.EXT_EVENT[0]		gpio1.IO[3]
	13	AB15	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]	sai5.RX_SYNC	gpio3.IO[19]
	29	AG9	spdif1.IN	pwm2.OUT				gpio5.IO[4]	spdif1.IN	gpio5.IO[4]
	37	AB9	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT	ccmsrcgpcmix.CLKO2	gpio1.IO[15]

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports 6.9V to 24V external power and uses on board voltage regulators for internal power management. By default, it supports to work with 12V power input. 12V power input from an external power supply is connected to the i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC (J17). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. The Power Jack is physically placed at the top of the board as shown below.

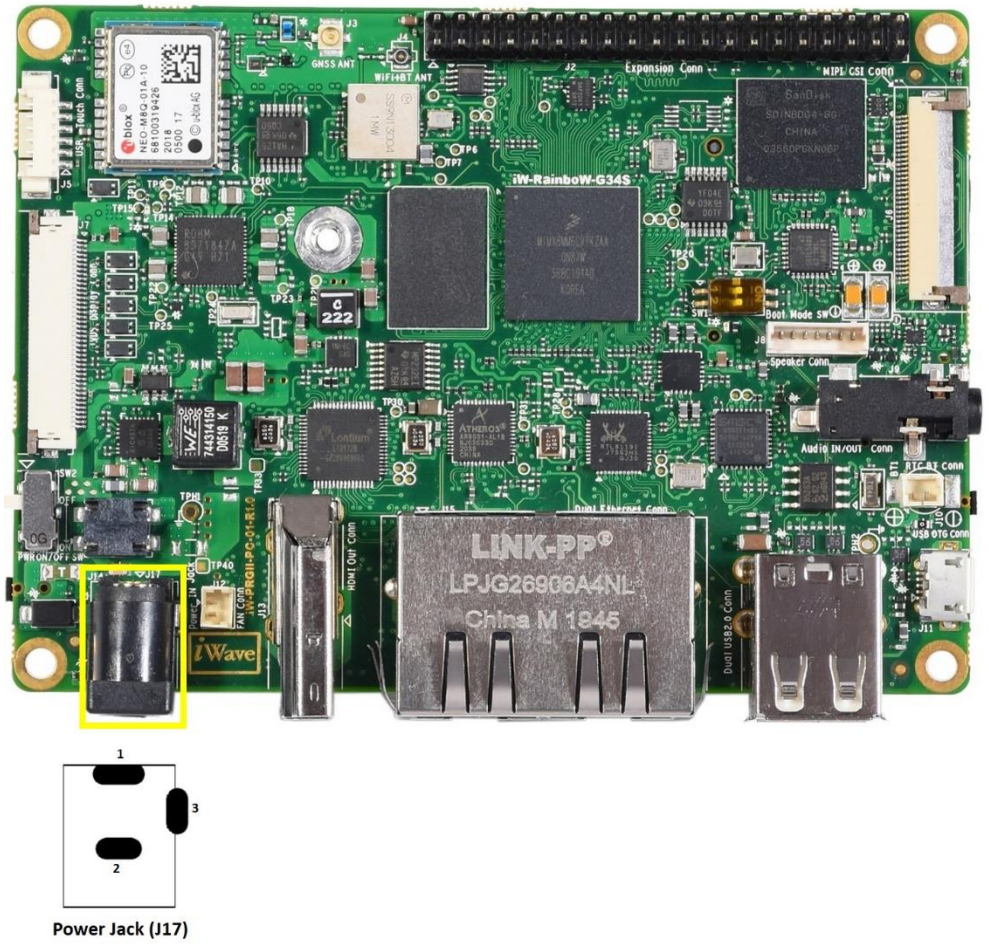

Figure 32: Power Input Jack

Table 22: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[1]	2.8V	3V	3.3V	±20mV

[1] The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC uses this voltage as backup power source to PMIC RTC controller when VCC is off.

3.2 Power Consumption

Table23: i.MX 8M Mini Pico ITX SBC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play 1080p Video run in HDMI display	VCC_ 12V	TBD
GPU Processor -Graphics 3D Test	VCC_ 12V	TBD
Play Audio	VCC_ 12V	TBD
Ping Bluetooth	VCC_ 12V	TBD
Ping Wi-Fi	VCC_ 12V	TBD
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_ 12V	TBD
Ping Ethernet (Eth0 & Eth1) at 100Mbps	VCC_ 12V	TBD
Ping Ethernet (Eth0 & Eth1) at 10Mbps	VCC_ 12V	TBD
eMMC to Micro SD file transfer	VCC_ 12V	TBD
eMMC to USB2.0 OTG file transfer	VCC_ 12V	TBD
eMMC to USB2.0 file transfer	VCC_ 12V	TBD
Bluetooth file transfer	VCC_ 12V	TBD
Wi-Fi file transfer	VCC_ 12V	TBD
Ethernet Streaming (Video Play)	VCC_ 12V	TBD
Dhrystone	VCC_ 12V	TBD
Maximum Power Test: • Run the below during Maximum Power Test, • Play Video run in MIPI display (Gplay) • Camera Streaming • Ethernet (eth0 & eth1) Run the ping (65500 packet size) • Wi-Fi- Run the ping testing in background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background • GPU Processor -Graphics 3D Test	VCC_ 12V	TBD
Low Power Mode Power Consumption		
System Idle Mode.	VCC_ 12V	TBD
Deep Sleep Mode.	VCC_ 12V	TBD
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	TBD

[1] Power consumption measurements have been done in iWave'si.MX 8M based Pico ITX SBC with iWave's iW-PRGII-SC-01-R1.0-REL1.0-Linux4.14.98 BSP.

Table24: i.MX 8M Nano Pico ITX SBC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play 1080p Video run in HDMI display	VCC_ 12V	TBD
GPU Processor -Graphics 3D Test	VCC_ 12V	TBD

Task/Status	Power Rail	Current Drawn/ Power Consumption
Play Audio	VCC_ 12V	TBD
Ping Bluetooth	VCC_ 12V	TBD
Ping Wi-Fi	VCC_ 12V	TBD
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_ 12V	TBD
Ping Ethernet (Eth0 & Eth1) at 100Mbps	VCC_ 12V	TBD
Ping Ethernet (Eth0 & Eth1) at 10Mbps	VCC_ 12V	TBD
eMMC to Micro SD file transfer	VCC_ 12V	TBD
eMMC to USB2.0 OTG file transfer	VCC_ 12V	TBD
eMMC to USB2.0 file transfer	VCC_ 12V	TBD
Bluetooth file transfer	VCC_ 12V	TBD
Wi-Fi file transfer	VCC_ 12V	TBD
Ethernet Streaming (Video Play)	VCC_ 12V	TBD
Dhrystone	VCC_ 12V	TBD
Maximum Power Test: • Run the below during Maximum Power Test, • Play Video run in MIPI display (Gplay) • Camera Streaming • Ethernet (eth0 & eth1) Run the ping (65500 packet size) • Wi-Fi- Run the ping testing in background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background • GPU Processor -Graphics 3D Test	VCC_ 12V	TBD
Low Power Mode Power Consumption		
System Idle Mode.	VCC_ 12V	TBD
Deep Sleep Mode.	VCC_ 12V	TBD
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	TBD

[1] Power consumption measurements have been done in iWave'si.MX 8M Nano SoC based Pico ITX SBC with iWave's iW-PRGII-SC-01-R1.0-REL1.0-Linux4.14.98 BSP.

3.3 EnvironmentalCharacteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC.

Table 25: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]The LBEE5HY1MW Wi-Fi & BT module supports operating temperature -30°C to 85°C with the default module's firmware. To set the module temperature to industrial grade in firmware, please contact iWave.

[3] For more information on Thermal solution & Heat sink refer the following section.

3.3.1 Heat Sink

For any highly integrated SBC, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink or Fan Sink must be used. Always need to remember that more effective thermal solution will give more performance out of the CPU.

Heat spreader acts as thermal coupling device between Module and external thermal solution. Heat spreader also provides thermal coupling to CPU via gap filler for better heat exchange. Heat spreader is not a complete thermal solution by itself. Heat spreader has to be used with application specific thermal solutions like heat sinks, Chassis, fans, Heat pipes etc.

Note: iWave supports Heat Sink Solution for i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC. For more information on Heat Sink& Fan Sink contact iWave support team. Do not Power On the i.MX 8 QM/QP Pico ITX SBC without a proper thermal solution.

iW-RainboW-G34S/G37S
i.MX 8M Mini/Nano Pico ITX SBC HEAT SINK
ORDERING PART NUMBER: iW-HSKALU-CLASLR-SB04

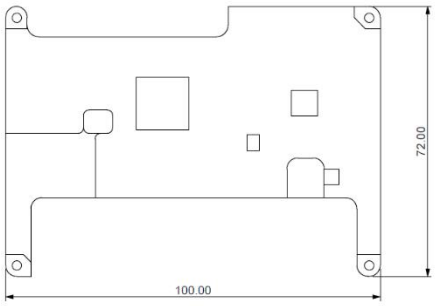

Fig 1.1

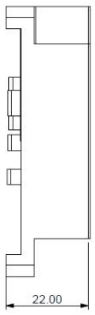

Fig 1.2

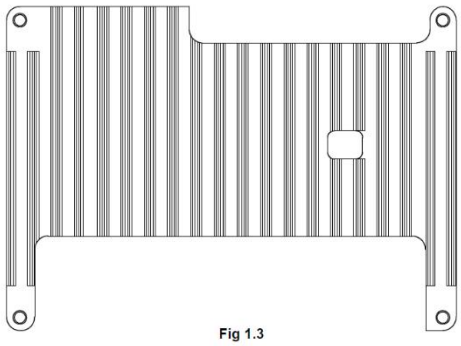
Fig 1.3

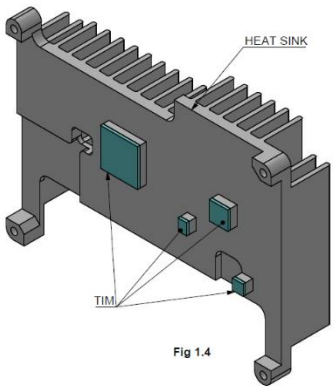

Fig 1.4

Fig 1.5

TABLE1.1: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
THERMAL CONDUCTIVITY	6.2 W/mK
FLAME RATING	UL 94 V-0
HARDNESS	50 Shore 00
WORKING TEMP.	-50~+150 °C
ROHS	YES

Figure 33: Mechanical dimension of Heat Sink

3.3.2 RoHS Compliance

iWave'si.MX 8M Mini or i.MX 8M Nano Pico ITX SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave'si.MX 8M Mini or i.MX 8M Nano Pico ITX SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Mechanical Dimensions

i.MX 8 Pico ITX SBCPCB size is 100mm x 72mm x 1.2mm. Pico ITX SBC mechanical dimension is shown below. (All dimensions are shown in mm)

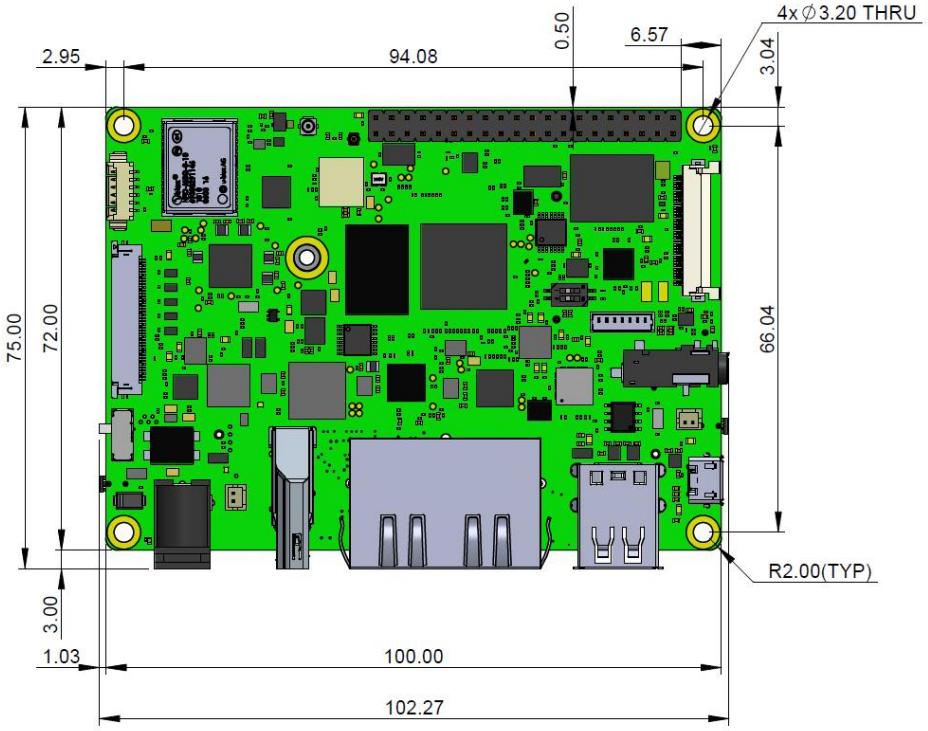

Figure 34: Mechanical Dimensions of 1.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Top View

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC PCB thickness is 1.2mm±0.15mm, top side maximum height component is 16.40mm (HDMI Connector), followed by Dual Ethernet Connector (16.40mm). In bottom side maximum height component is JTAG connector (5.91mm) followed by M.2 SMT spacer (3.99mm).

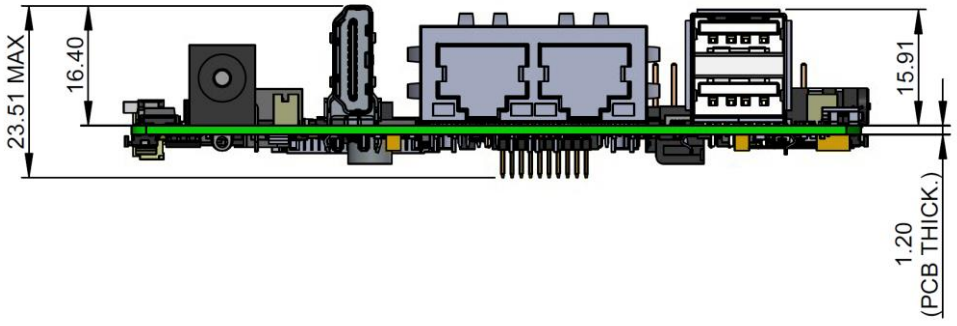

Figure 35: Mechanical Dimensions of 1.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Side View-1

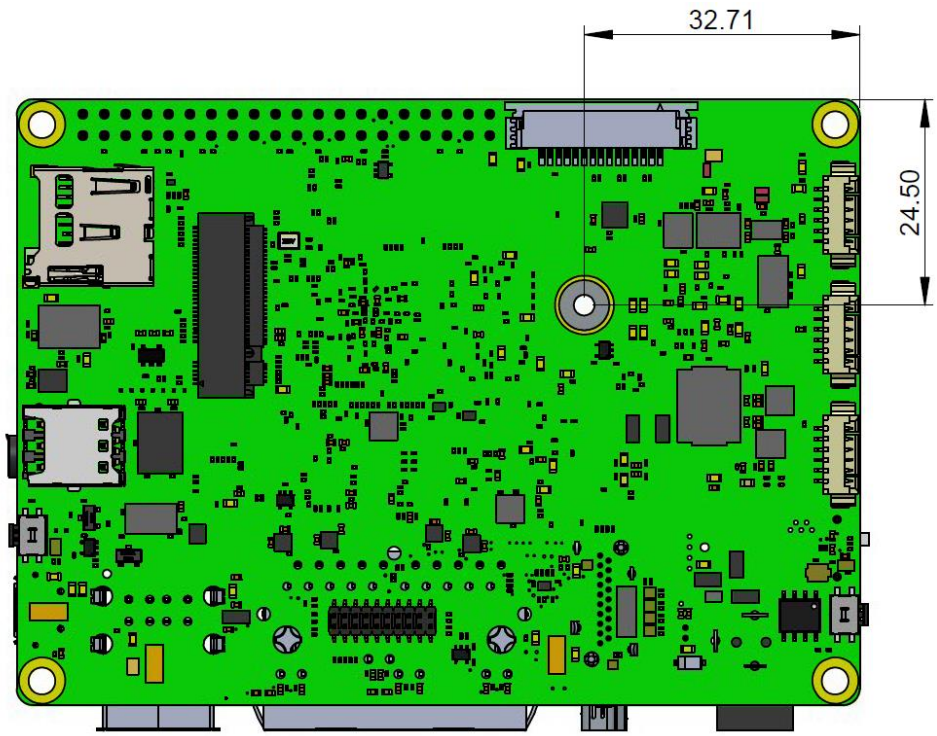

Figure 36: Mechanical Dimensions of 1.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Bottom View

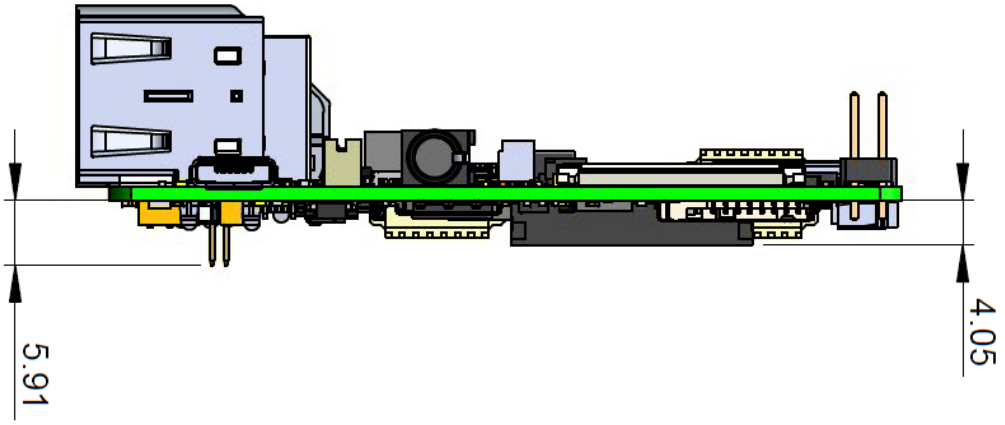

Figure 37: Mechanical Dimensions of 1.MX 8M Mini or i.MX 8M Nano Pico ITX SBC Side View-2

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 26: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G34S - i.MX 8M Mini Pico ITX SBC (Industrial grade) with 1GB LPDDR4, Wi-Fi & Ethernet		
TBD		
TBD		
TBD		
TBD		
TBD		
TBD		
iW-Rainbow G34S - i.MX 8M Mini Pico ITX SBC (Industrial grade) with 2GB LPDDR4, Wi-Fi & Ethernet		
TBD		
TBD		
TBD		
TBD		

Important Note: Some of the above-mentioned Part Numbers are subject to MOQ purchase. Please contact iWave for further details.

For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.


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