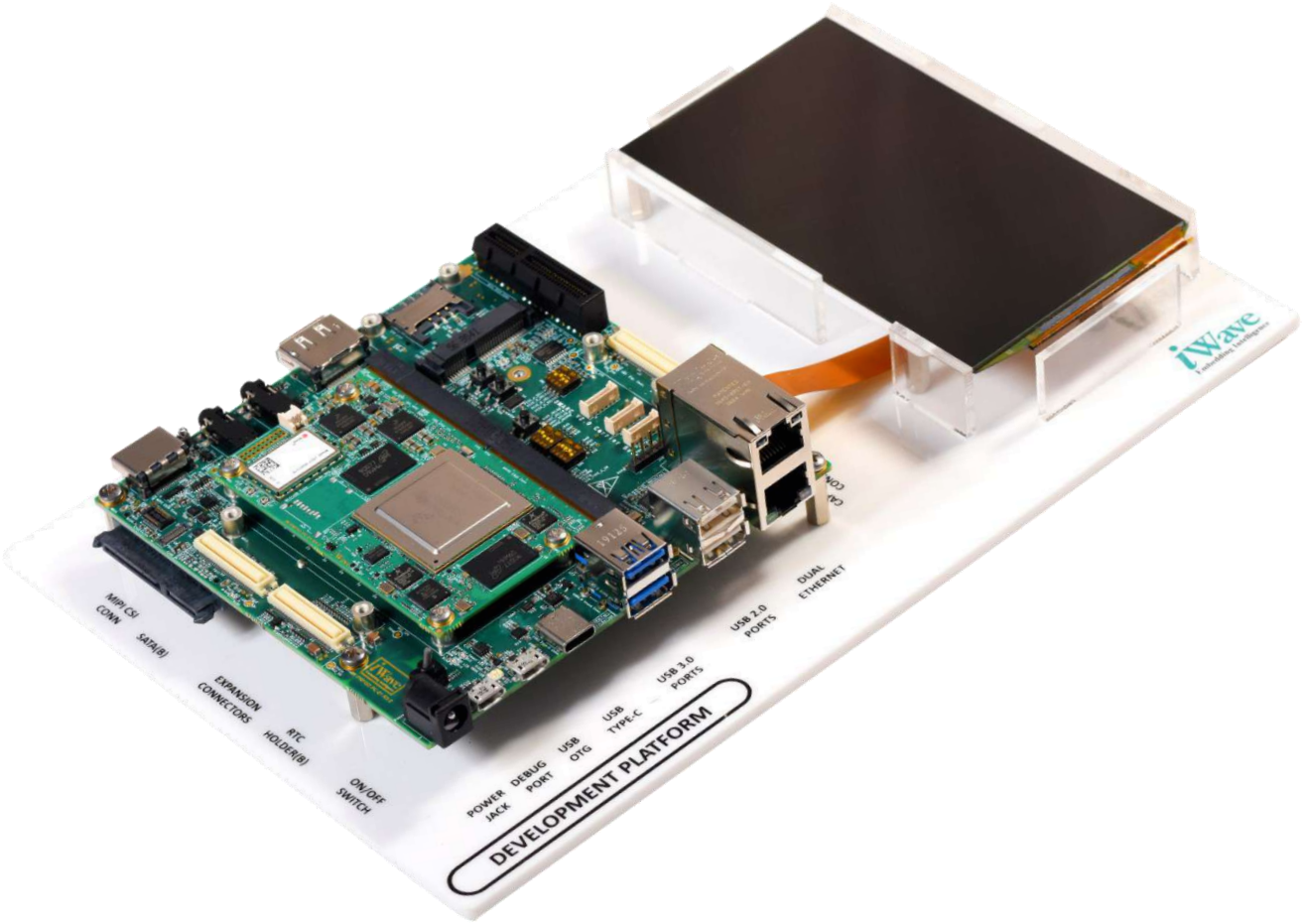
iW-RainboW-G27D
i.MX8 QuadMax/QuadPlus
SMARC Development Platform
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the i.MX8 QM/QP SMARC V2.0 Development platform "iW-RainboW-G27D" based on the NXP's i.MX8 Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX8 QM/QP based SMARC development platform from a Hardware Systems perspective. Complete information about the i.MX8 QM/QP SMARC SOM is explained in another document "iW-RainboW-G27M_i.MX8_SMARC_SOM-HardwareUserGuide".

1.2 Overview

The SMARC V2.0 ("Smart Mobility ARChitecture") is a versatile small form factor computer Module definition targeting application that require low power, low costs, and high performance. The Module power envelope is typically under 6W although designs up to about 15W are possible.

iW-RainboW-G27D Development Platform comes with SMARC V2.0 Generic Carrier, i.MX8 QM/QP based SMARC V2.1.1 SOM along with 5.5-inch Capacitive Touch Display. The development board can be used for quick prototyping of various applications targeted by the I.MX8 processor. With the 120mmx120mm Nano ITX size, SMARC carrier board is highly packed with all the necessary on-board connectors to validate the SMARC features of I.MX8 QM/QP SMARC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DP	Display Port
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia Interface
Hz	Hertz
I2C	Inter-Integrated Circuit

Acronyms	Abbreviations
I2S	Inter-IC Sound
IC	Integrated Circuit
LVDS	Low Voltage Differential Signalling
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
MXM	Mobile PCI Express Module
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SMARC	Smart Mobility ARChitecture
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface signals
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

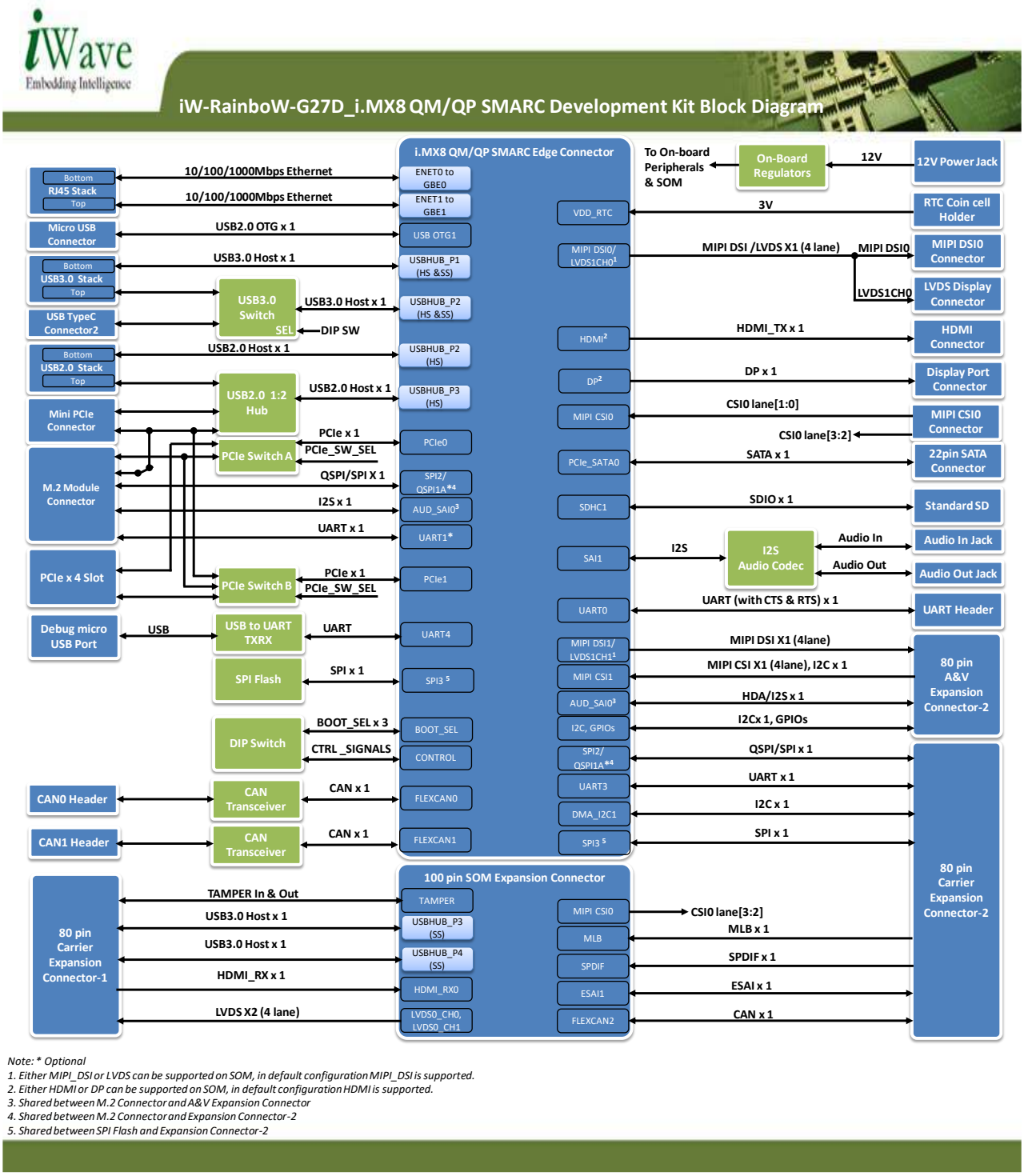
1.5 References

- IMX8QMAEC_Revx.pdf
- iMX8QM_RM_Rev_x.pdf
- SMARC Specification V2.0

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX8 QM/QP SMARC SOM features and Hardware architecture with high level block diagram.

2.1 i.MX8 QM/QP SMARC Development Platform Block Diagram



*Note: * Optional*
1. Either MIPI_DSI or LVDS can be supported on SOM, in default configuration MIPI_DSI is supported.
2. Either HDMI or DP can be supported on SOM, in default configuration HDMI is supported.
3. Shared between M.2 Connector and A&V Expansion Connector
4. Shared between M.2 Connector and Expansion Connector-2
5. Shared between SPI Flash and Expansion Connector-2

Figure 1: i.MX8 QM/QP SMARC Development Platform Block Diagram

2.2 i.MX8 QM/QP SMARC Development Platform Features

The NXP's i.MX8 QM/QP SMARC carrier board supports the following features to validate the NXP's i.MX8 QM/QP SMARC SOM Edge connector interface.

Serial Interface Features

- Debug UART through USB Micro AB Connector
- Data UART x 1 Port through Header

High Speed Interface Features

- PCIe x 1 Port through x4 connector or Mini-PCIe connector or M.2 connector [1,2]
- SATA x 1 Port through 22pin SATA Connector
- USB 3.0 Host x 2 Port through USB 3.0 Type A Connector[3]
- USB Type C x 1 Port[3]

Communication Features

- Dual 10/100/1000Mbps Ethernet through RJ45MagJack
- USB 2.0 Host x 2 Port through USB 2.0 Type A Connector
- USB 2.0 OTG x 1 Port through Micro AB Connector
- SDHC/SDIO (4bit) x 1 Port through Standard SD Connector
- CAN x 2 Port Through Header

Audio/Video Features

- HDMI X 1 Port through Type A Connector
- MIPI DSI 4lane Display Connector with Capacitive Touch
- MIPI CSI 2lane/4lane Camera Connector
- I2S Audio Codec with 3.5mm Audio IN and OUT jack
- LVDS Connector (Optional)
- Display Port (Optional)

Additional Features

- SPI Flash
- RTC Coin Cell holder

On Board Switches

- Power ON/OFF Switch
- Board Configuration Switch
- Reset Switch
- Force Boot Switch

A&V Expansion Connector

- MIPI CSI - 4 lanes x 1 Port
- MIPI DSI - 4 lanes x 1 Port
- I2S/HDA x 1 Port

Carrier board Expansion Connectors

- SPI x 1 Port (Optional - Shared with SPI Flash)
- QSPI/SPI x 1 Port (Shared with M.2 connector)
- HDMI Receiver x 1Port
- LVDS x 2 Channel
- CAN x 1 Port
- USB3.0 Host x 2 Ports (through On-SOM USB Hub)
- ESAI x 1 Port
- SPDIF x 1 Port
- MLB x 1 Port
- TAMPER In & Out
- GPIOs

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Temperature Supported : 0°C to +60°C
- Form Factor : 120mm X 120mm Nano ITX

1. PCIe Channel A can be connected to either Mini PCIe or M.2 Connector or PETp0 of PCIe X4 connector by using on Board Switches, whereas PCIe Channel B can be connected to either Mini PCIe or M.2 Connector or PETp1 of PCIe X4 connector by using on Board Switches.

2. At a time, do not set Both the PCIe Channel A & B neither to mini PCIe nor to M.2 connector.

3. Either USB Type C connector or USB 3.0 Type A TOP connector can be supported at a time. Anyone can be selected using on Board Switches.

2.3 SMARC MXM Connector

The i.MX8 QM/QP SMARC carrier board supports 314Pin SMARC MXM Edge mating connector for SMARC SOM attachment. This standard 314-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This SMARC MXM connector (J16) is physically located at the top of the board as shown below.

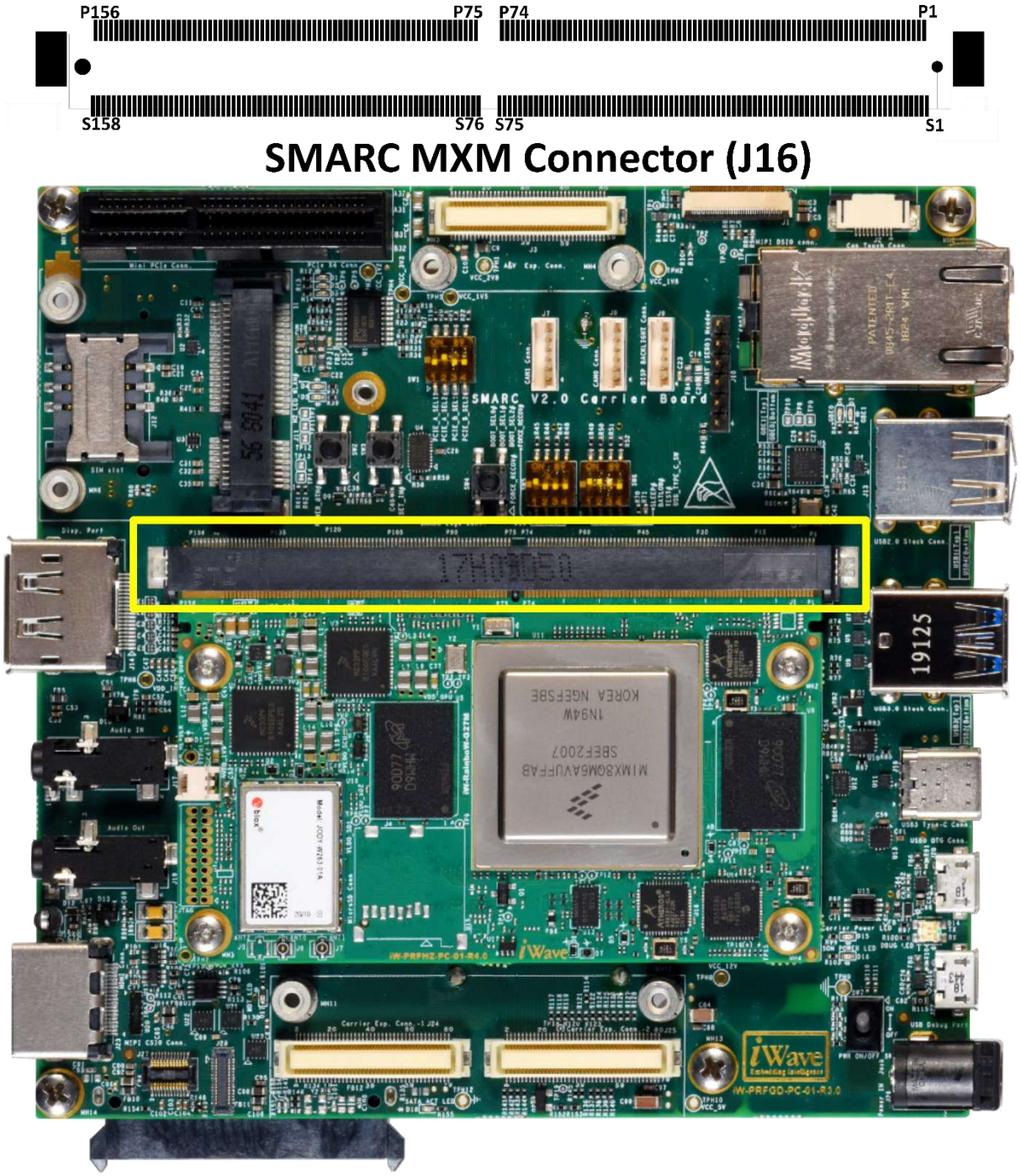


Figure 2: SMARC MXM Connector

2.3.1 SMARC PCB Edge Connector Pin Assignment

Table 3: SMARC PCB Edge Connector Pin Assignment

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
SMARC Primary Side					
P1	SMB_ALERT_1V8#	SMBUS_ALERT(GPIO 0_16)	GPT0_COMPARE/ AW53	O, 1.8V CMOS	SM Bus Alert# (interrupt) signal
P2	GND	GND	NA	Power	Ground.
P3	CSI1_CK+	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/ BJ17	O, MIPI	MIPI CSI1 differential clock positive.
P4	CSI1_CK-	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ BH16	O, MIPI	MIPI CSI1 differential clock negative.
P5	GBE1_SDP	NC	NA	NA	NC
P6	GBE0_SDP	NC	NA	NA	NC
P7	CSI1_RX0+	MIPI_CSI1_DATA0_P	MIPI_CSI1_DATA0_ P/BH18	O, MIPI	MIPI CSI1 differential data lane 0 positive.
P8	CSI1_RX0-	MIPI_CSI1_DATA0_N	MIPI_CSI1_DATA0_ N /BJ19	O, MIPI	MIPI CSI1 differential data lane 0 negative.
P9	GND	GND	NA	Power	Ground.
P10	CSI1_RX1+	MIPI_CSI1_DATA1_P	MIPI_CSI1_DATA1_ P/BJ15	O, MIPI	MIPI CSI1 differential data lane 1 positive.
P11	CSI1_RX1-	MIPI_CSI1_DATA1_N	MIPI_CSI1_DATA1_ N/BH14	O, MIPI	MIPI CSI1 differential data lane 1 negative.
P12	GND	GND	NA	Power	Ground.
P13	CSI1_RX2+	MIPI_CSI1_DATA2_P	MIPI_CSI1_DATA2_ P/BJ21	O, MIPI	MIPI CSI1 differential data lane 2 positive.
P14	CSI1_RX2-	MIPI_CSI1_DATA2_N	MIPI_CSI1_DATA2_ N/BH20	O, MIPI	MIPI CSI1 differential data lane 2 negative
P15	GND	GND	NA	Power	Ground.
P16	CSI1_RX3+	MIPI_CSI1_DATA3_P	MIPI_CSI1_DATA3_ P/BJ13	O, MIPI	MIPI CSI1 differential data lane 3 positive.
P17	CSI1_RX3-	MIPI_CSI1_DATA3_N	MIPI_CSI1_DATA3_ N/BH12	O, MIPI	MIPI CSI1 differential data lane 3 negative.
P18	GND	GND	NA	Power	Ground.
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
P21	GBE0_LINK100#	GBE0_LINK100#	NA	I, 3.3V CMOS	100Mbps Ethernet link status LED
P22	GBE0_LINK1000#	GBE0_LINK1000#	NA	I, 3.3V CMOS	Gigabit Ethernet link status LED

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
P25	GBE0_LINK_ACT#	GBE0_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet activity status
P26	GBE0_MDI1-	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.
P27	GBE0_MDI1+	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
P28	GBE0_CTREF	VPHY0_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector
P29	GBE0_MDI0-	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
P30	GBE0_MDI0+	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.
P31	SPI0_CS1#	SPI3_CS1	SPI3_CS1/ BD8	I, 1.8V CMOS	SPI0 Chip Select 1
P32	GND	GND	NA	Power	Ground.
P33	SDIO_WP	GPIO_SDC1_WP(GPIO1_22)	MIPI_DSI1_GPIO0_00/BM24	0, 3.3V CMOS	SD write Protect.
P34	SDIO_CMD	USDHC1_CMD	USDHC1_CMD/ G41	IO, 1.8/3.3V CMOS	SD command.
P35	SDIO_CD#	GPIO_SDC1_CD(GPIO1_23)	MIPI_DSI1_GPIO0_01/BK24	I, 3.3V/ CMOS	SD Card Detect.
P36	SDIO_CK	USDHC1_CLK	USDHC1_CLK/ J39	I, 1.8/3.3V CMOS	SD Clock.
P37	SDIO_PWR_EN	GPIO_SDC1_PWR_EN(GPIO1_19)	MIPI_DSI0_GPIO0_01/ BD28	I, 3.3V CMOS	SD Power enable.
P38	GND	GND	NA	Power	Ground.
P39	SDIO_D0	USDHC1_DATA0	USDHC1_DATA0/ E37	IO, 1.8/3.3V CMOS	SD data 0.
P40	SDIO_D1	USDHC1_DATA1	USDHC1_DATA1/ F38	IO, 1.8/3.3V CMOS	SD data 1
P41	SDIO_D2	USDHC1_DATA2	USDHC1_DATA2/ E39	IO, 1.8/3.3V CMOS	SD data 2
P42	SDIO_D3	USDHC1_DATA3	USDHC1_DATA3/ F40	IO, 1.8/3.3V CMOS	SD data 3
P43	SPI0_CS0#	SPI3_CS0	SPI3_CS0/ BG5	I, 1.8V CMOS	SPI0 Chip Select 0

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P44	SPI0_CK	SPI3_SCLK	SPI3_SCLK/ BF6	I, 1.8V CMOS	SPI0 Clock
P45	SPI0_DIN	SPI3_MISO/	SPI3_MISO/ BE5	I, 1.8V CMOS	SPI0 Master IN Slave OUT
P46	SPI0_DO	SPI3_MOSI	SPI3_MOSI/ BF2	O, 1.8V CMOS	SPI0 Master OUT Slave IN
P47	GND	GND	NA	Power	Ground.
P48	SATA_TX+	PCIE_SATA0_TX0_P	PCIE_SATA0_TX0_P / B16	I, DIFF	SATA Transmit Lane Positive
P49	SATA_TX-	PCIE_SATA0_TX0_N	PCIE_SATA0_TX0_ N/ C17	I, DIFF	SATA Transmit Lane Negative
P50	GND	GND	NA	Power	Ground.
P51	SATA_RX+	PCIE_SATA0_RX0_P	PCIE_SATA0_RX0_P / A19	O, DIFF	SATA Receive Lane Positive
P52	SATA_RX-	PCIE_SATA0_RX0_N	PCIE_SATA0_RX0_ N/ B20	O, DIFF	SATA Receive Lane Negative
P53	GND	GND	NA	Power	Ground.
P54	ESPI_CS0#	QSPI1A_SS0	SPI2_CS0/ AW1 or QSPI1A_SS0/ J11	I, 1.8V CMOS	SPI2 Chip Select 0. *Note: when used as QSPI, it will act as QSPI1A_ Chip Select 0*
P55	ESPI_CS1#	QSPI1A_SS1	QSPI1A_SS1/ G11	I, 1.8V CMOS	NC *Note: when used as QSPI, it will act as QSPI1A_ Chip Select 1*
P56	ESPI_CK	QSPI1A_SCLK	SPI2_SCK/ AW5 or QSPI1A_SCLK/ F10	I, 1.8V CMOS	SPI2 Clock *Note: when used as QSPI, it will act as QSPI1A_ Clock*
P57	ESPI_IO_0	QSPI1A_DATA0	SPI2_SDI/ AY4 or QSPI1A_DATA0/ D12	IO, 1.8V CMOS	SPI2 Master In Slave Out. *Note: when used as QSPI, it will act as QSPI1A_ DATA0*

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P58	ESPI_IO_1	QSPI1A_DATA1	SPI2_SDO/ BA1 or QSPI1A_DATA1/ D14	IO, 1.8V CMOS	SPI2 Master Out Slave In *Note: when used as QSPI, it will act as QSPI1A_ DATA1*
P59	GND	GND	NA	Power	Ground.
P60	USB0+	USB_OTG1_DP	USB_OTG1_DP / B40	IO, USB HS	USB Port0 Data Plus
P61	USB0-	USB_OTG1_DM	USB_OTG1_DM / C39	IO, USB HS	USB Port0 Data Minus
P62	USB0_EN_OC#	USB_OTG1_PWR(GPIO4_03)	USB_SS3_TC0/ J9	IO, 3.3V CMOS	USB Port0 Power Enable/ Over Current Indicator
P63	USB0_VBUS_DET	VBUS_OTG1	USB_OTG1_VBUS/ A39	5V, Power	USB host power detection, when this port is used as a device.
P64	USB0_OTG_ID	USB_OTG_ID	USB_OTG2_ID/ F30	O, 3.3V CMOS	USB0 OTG ID.
P65	USB1+	USB_HUB3OUT_DP	NA	IO, USB HS	USB Port1 Data Plus *Note: Connected to USB Hub*
P66	USB1-	USB_HUB3OUT_DM	NA	IO, USB HS	USB Port1 Data Minus *Note: Connected to USB Hub*
P67	USB1_EN_OC#	USB_HUB3_OC	NA	IO, 3.3V CMOS	USB Port1 Power Enable/ Over Current Indicator *Note: Connected to USB Hub*
P68	GND	GND	NA	Power	Ground.
P69	USB2+	USB_HUB1OUT_DP	NA	IO, USB HS	USB Port2 Data Plus *Note: Connected to USB Hub*
P70	USB2-	USB_HUB1OUT_DM	NA	IO, USB HS	USB Port2 Data Minus *Note: Connected to USB Hub*
P71	USB2_EN_OC#	USB_HUB1_OC	NA	IO, 3.3V CMOS	USB Port2 Power Enable/ Over Current Indicator *Note: Connected to USB Hub*
P72	RSVD4	NC	NA	NA	NA
P73	RSVD5	NC	NA	NA	NA
P74	USB3_EN_OC#	USB_HUB2_OC	NA	IO, 3.3V CMOS	USB Port3 Power Enable/ Over Current Indicator *Note: Connected to USB Hub*
KEY					
P75	PCIE_A_RST#	PCIE_A_RST_B(GPIO4_29)	PCIE_CTRL0_PERST_B/D20	I, 3.3V CMOS	PCIE_A Reset Out

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P76	USB4_EN_OC#	USB_HUB4_OC	NA	IO, 3.3V CMOS	USB Port4 Power Enable/ Over Current Indicator *Note: Connected to USB Hub*
P77	RSVD6	NC	NA	NA	NA
P78	RSVD7	NC	NA	NA	NA
P79	GND	GND	NA	Power	Ground.
P80	PCIE_C_REFCK+	NC	NA	NA	NA
P81	PCIE_C_REFCK-	NC	NA	NA	NA
P82	GND	GND	NA	Power	Ground.
P83	PCIE_A_REFCK+	PCIE_REFCLK_P	NA	I, PCIe	PCIe Channel-A Clock Positive
P84	PCIE_A_REFCK-	PCIE_REFCLK_N	NA	I, PCIe	PCIe Channel-A Clock Negative
P85	GND	GND	NA	Power	Ground.
P86	PCIE_A_RX+	PCIE0_A_RX0_P	PCIE0_RX0_P/ A29	O, PCIe	PCIe Channel-A Receive Positive
P87	PCIE_A_RX-	PCIE0_A_RX0_N	PCIE0_RX0_N/ B30	O, PCIe	PCIe Channel-A Receive Negative
P88	GND	GND	NA	Power	Ground.
P89	PCIE_A_TX+	PCIE0_A_TX0_P	PCIE0_TX0_P/ B26	I, PCIe	PCIe Channel-A Transmit Positive
P90	PCIE_A_TX-	PCIE0_A_TX0_N	PCIE0_TX0_N/ C27	I, PCIe	PCIe Channel-A Transmit Negative
P91	GND	GND	NA	Power	Ground.
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX0_DATA2_ P/EDP0_P	HDMI_TX0_DATA2 _EDP0_P/BL9	I, HDMI	HDMI Transceiver 2 Positive to HDMI Connector
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX0_DATA2_ N/EDP0_N	HDMI_TX0_DATA2 _EDP0_N/BM8	I, HDMI	HDMI Transceiver 2 Negative to HDMI Connector
P94	GND	GND	NA	Power	Ground.
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX0_DATA1_ P/EDP1_P	HDMI_TX0_DATA1 _EDP1_P/BL7	I, HDMI	HDMI Transceiver 1 Positive to HDMI Connector
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX0_DATA1_ N/EDP1_N	HDMI_TX0_DATA1 _EDP1_N/BM6	I, HDMI	HDMI Transceiver 1 Negative to HDMI Connector
P97	GND	GND	NA	Power	Ground.
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX0_DATA0_ P/EDP2_P	HDMI_TX0_DATA0 _EDP2_P/BL5	I, HDMI	HDMI Transceiver 0 Positive to HDMI Connector
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX0_DATA0_ N/EDP2_N	HDMI_TX0_DATA0 _EDP2_N/BM4	I, HDMI	HDMI Transceiver 0 Negative to HDMI Connector
P100	GND	GND	NA	Power	Ground.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TX0_CLK_P/EDP3_P	HDMI_TX0_CLK_EDP3_P/ BL3	I, HDMI	HDMI Transceiver CLK Positive to HDMI Connector
P102	HDMI_CK- / DP1_LANE3-	HDMI_TX0_CLK_N/EDP3_N	HDMI_TX0_CLK_EDP3_N/BK2	I, HDMI	HDMI Transceiver CLK Negative to HDMI Connector
P103	GND	GND	NA	Power	Ground.
P104	HDMI_HPD / DP1_HPD	HDMI_TX_HPD	HDMI_TX_HPD / BH8	O, 1.8V CMOS	HDMI Hot Plug Detect from HDMI Connector.
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_TX0_CTRL_CLK/_AUX_P	HDMI_TX0_DDC_SCL /BG1	I, 1.8V CMOS	HDMI DDC Clock to HDMI Connector through Voltage Level translator
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_TX0_CTRL_DAT/_AUX_N	HDMI_TX0_DDC_SDA /BN5	IO, 1.8V CMOS	HDMI DDC DATA to HDMI Connector through Voltage Level translator
P107	DP1_AUX_SEL	NC	NA	-	NC.
P108	GPIO0 / CAM0_PWR#	SMARC_GPIO_0(GPIO1_27)	MIPI_CSI0_GPIO0_00/BL23	IO, 1.8V CMOS	General Purpose Input/ Output 0. Connected to CAN0 Transceiver Power Down.
P109	GPIO1 / CAM1_PWR#	SMARC_GPIO_1(GPIO1_30)	MIPI_CSI1_GPIO0_00/BN15	IO, 1.8V CMOS	General Purpose Input/ Output 1. Connected to CAN1 Transceiver Power Down.
P110	GPIO2 / CAM0_RST#	SMARC_GPIO_2(GPIO1_28)	MIPI_CSI0_GPIO0_01/BM22	IO, 1.8V CMOS	General Purpose Input/ Output 2. Used for Camera RESET
P111	GPIO3 / CAM1_RST#	SMARC_GPIO_3(GPIO1_31)	MIPI_CSI1_GPIO0_01/BN13	IO, 1.8V CMOS	General Purpose Input/ Output 3. Connected to A&V Expansion connector
P112	GPIO4 / HDA_RST#	SMARC_GPIO_4(GPIO4_11)	USDHC2_WP / D8	IO, 1.8V CMOS	General Purpose Input/ Output 4.USB type C switching Port selection
P113	GPIO5 / PWM_OUT	SMARC_GPIO_5(GPIO0_19)	GPT1_COMPARE/ BA51	IO, 1.8V CMOS	General Purpose Input/ Output 5. Connected to HDMI_CEC#
P114	GPIO6 / TACHIN	SMARC_GPIO_6(GPIO0_00)	SIM0_CLK/ AL45	IO, 1.8V CMOS	General Purpose Input/ Output 6. Connected to USB Type C Controller Interrupt pin.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P115	GPIO7	SMARC_GPIO_7(GPIO0_01)	SIM0_RST/ AP48	IO, 1.8V CMOS	General Purpose Input/ Output 7. Connected to Touch interrupt
P116	GPIO8	SMARC_GPIO_8(GPIO0_02)	SIM0_IO/ AN45	IO, 1.8V CMOS	General Purpose Input/ Output 8. Connected to Headphone Detect
P117	GPIO9	SMARC_GPIO_9(GPIO0_03)	SIM0_PD/ AL43	IO, 1.8V CMOS	General Purpose Input/ Output 9. Connected to MIPI Display RESET
P118	GPIO10	SMARC_GPIO_10(GPIO0_04)	SIM0_POWER_EN/ AT48	IO, 1.8V CMOS	General Purpose Input/ Output 10. Connected to PCIe connector for Wireless disable (active low).
P119	GPIO11	SMARC_GPIO_11(GPIO0_05)	SIM0_GPIO0_00/ AP46	IO, 1.8V CMOS	General Purpose Input/ Output 11. Connected to MIC Detect.
P120	GND	GND	NA	Power	Ground.
P121	I2C_PM_CK	SM_PMIC_I2C_SCL	PMIC_I2C_SCL / AY46	I, 1.8V CMOS	NC
P122	I2C_PM_DAT	SM_PMIC_I2C_SDA	PMIC_I2C_SDA/ BG51	IO, 1.8V CMOS	NC
P123	BOOT_SEL0#	BOOT_SEL0#	NA	O, 1.8V CMOS	Boot Media Select bit 0 from 4bit DIP Switch (SW5).
P124	BOOT_SEL1#	BOOT_SEL1#	NA	O, 1.8V CMOS	Boot Media Select bit 1 from 4bit DIP Switch (SW5).
P125	BOOT_SEL2#	BOOT_SEL2#	NA	O, 1.8V CMOS	Boot Media Select bit 2 from 4bit DIP Switch (SW5).
P126	RESET_OUT#	GPIO_RESET_OUT(GPIO0_10)	M41_I2C0_SCL/ AR45	I, 1.8V CMOS	RESOUT from CPU to all other peripherals
P127	RESET_IN#	RESET_IN#	POR_B/ BE49	O, 1.8V CMOS	Hard RESET Input to SOM.
P128	POWER_BTN#	ON_OFF_BUTTON	ON_OFF_BUTTON/ BE47	O, 1.8V CMOS	Power ON /OFF Input to SOM.
P129	SER0_TX	UART0_TX	UART0_TX/ AV50	I, 1.8V CMOS	UART0 Transmitter
P130	SER0_RX	UART0_RX	UART0_RX/ AV48	O, 1.8V CMOS	UART0 Receiver
P131	SER0_RTS#	UART0_RTS_B	UART0_RTS_B/ AU45	I, 1.8V CMOS	UART0 Request to Send
P132	SER0_CTS#	UART0_CTS_B	UART0_CTS_B/ AW49	O, 1.8V CMOS	UART0 Clear to Send

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P133	GND	GND	NA	Power	Ground.
P134	SER1_TX	UART3_TX	UART3_TX/ AU47	I, 1.8V CMOS	UART3 Transmitter
P135	SER1_RX	UART3_RX	UART3_RX/ AP44	O, 1.8V CMOS	UART3 Receiver
P136	SER2_TX	UART1_TX	UART1_TX/ AY48	I, 1.8V CMOS	NC. *Note: In default configuration UART1_TX used for on SOM Bluetooth support.*
P137	SER2_RX	UART1_RX	UART1_RX/ AT44	O, 1.8V CMOS	NC. *Note: In default configuration UART1_RX used for on SOM Bluetooth support.*
P138	SER2_RTS#	UART1_RTS_B	UART1_RTS_B/ AR43	I, 1.8V CMOS	NC. *Note: In default configuration UART1_RTS_B used for on SOM Bluetooth support.*
P139	SER2_CTS#	UART1_CTS_B	UART1_CTS_B/ AV46	O, 1.8V CMOS	NC. *Note: In default configuration UART1_CTS_B used for on SOM Bluetooth support.*
P140	SER3_TX	UART4_TX	UART4_TX/ AU53	I, 1.8V CMOS	Debug UART Transmitter
P141	SER3_RX	UART4_RX	UART4_RX/ AR47	O, 1.8V CMOS	Debug UART Receiver.
P142	GND	GND	NA	Power	Ground.
P143	CAN0_TX	FLEXCAN0_TX	FLEXCAN0_TX/ H6	I, 1.8V CMOS	CAN 0 Transmitter
P144	CAN0_RX	FLEXCAN0_RX	FLEXCAN0_RX/ C5	O, 1.8V CMOS	CAN 0 Receiver
P145	CAN1_TX	FLEXCAN1_TX	FLEXCAN1_TX/ G7	I, 1.8V CMOS	CAN 1 Transmitter
P146	CAN1_RX	FLEXCAN1_RX	FLEXCAN1_RX/ E5	O, 1.8V CMOS	CAN 1 Receiver
P147	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P148	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P149	VDD_IN	VDD_IN	NA	0, 5V Power	Supply Voltage

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P150	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P151	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P152	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P153	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P154	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P155	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
P156	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage
SMARC Secondary Side					
S1	CSI1_TX+ / I2C_CAM1_CK	MIPI_CSI1_I2C0_SCL	MIPI_CSI1_I2C0_SCL/BN17	I, 1.8V CMOS	MIPI CSI1 I2C Clock
S2	CSI1_TX- / I2C_CAM1_DAT	MIPI_CSI1_I2C0_SDA	MIPI_CSI1_I2C0_SDA/BE15	IO, 1.8V CMOS	MIPI CSI1 I2C Data
S3	GND	GND	NA	Power	Ground.
S4	RSVD1	NC	NA	NA	NA
S5	CSI0_TX- / I2C_CAM0_CK	MIPI_CSI0_I2C0_SCL	MIPI_CSI0_I2C0_SCL/BH24	I, 1.8V CMOS	MIPI CSI0 I2C Clock
S6	CAM_MCK	MIPI_CSI0_MCLK_OUT	MIPI_CSI0_MCLK_OUT /BJ23	I, 1.8V CMOS	Master Clock for Camera
S7	CSI0_TX+ / I2C_CAM0_DAT	MIPI_CSI0_I2C0_SDA	MIPI_CSI0_I2C0_SDA /BN19	IO, 1.8V CMOS	MIPI CSI0 I2C Data
S8	CSI0_CK+	MIPI_CSI0_CLK_P	MIPI_CSI0_CLK_P / BF20	O, MIPI	MIPI CSI0 differential Clock positive
S9	CSI0_CK-	MIPI_CSI0_CLK_N	MIPI_CSI0_CLK_N / BE21	O, MIPI	MIPI CSI0 differential Clock negative
S10	GND	GND	NA	Power	Ground.
S11	CSI0_RX0+	MIPI_CSI0_DATA0_P	MIPI_CSI0_DATA0_P/BF22	O, MIPI	MIPI CSI0 differential data lane 0 positive
S12	CSI0_RX0-	MIPI_CSI0_DATA0_N	MIPI_CSI0_DATA0_N/BE23	O, MIPI	MIPI CSI0 differential data lane 0 negative
S13	GND	GND	NA	Power	Ground.
S14	CSI0_RX1+	MIPI_CSI0_DATA1_P	MIPI_CSI0_DATA1_P/BE19	O, MIPI	MIPI CSI0 differential data lane 1 positive
S15	CSI0_RX1-	MIPI_CSI0_DATA1_N	MIPI_CSI0_DATA1_N/BF18	O, MIPI	MIPI CSI0 differential data lane 1 negative
S16	GND	GND	NA	Power	Ground.
S17	GBE1_MDI0+	GBE1_MDI0+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 positive.
S18	GBE1_MDI0-	GBE1_MDI0-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 negative.
S19	GBE1_LINK100#	GBE1_LINK100#	NA	I, 3.3V CMOS	100Mbps Ethernet link status LED

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S20	GBE1_MDI1+	GBE1_MDI1+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 positive.
S21	GBE1_MDI1-	GBE1_MDI1-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 negative.
S22	GBE1_LINK1000#	GBE1_LINK1000#	NA	I, 3.3V CMOS	1000Mbps Ethernet link status LED
S23	GBE1_MDI2+	GBE1_MDI2+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 positive.
S24	GBE1_MDI2-	GBE1_MDI2-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair2 negative.
S25	GND	GND	NA	NA	Power
S26	GBE1_MDI3+	GBE1_MDI3+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 positive.
S27	GBE1_MDI3-	GBE1_MDI3-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 negative.
S28	GBE1_CTREF	VPHY1_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector
S29	PCIE_D_TX+	NC	NA	NA	NA
S30	PCIE_D_TX-	NC	NA	NA	NA
S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#	NA	I, 3.3V CMOS	Ethernet Activity status LED
S32	PCIE_D_RX+	NC	NA	NA	NA
S33	PCIE_D_RX-	NC	NA	NA	NA
S34	GND	GND	NA	Power	Ground.
S35	USB4+	USB_HUB4OUT_DP	NA	IO, USB HS	USB Port4 Data Plus Note: Connected to USB Hub
S36	USB4-	USB_HUB4OUT_DM	NA	IO, USB HS	USB Port4 Data Minus Note: Connected to USB Hub
S37	USB3_VBUS_DET	NC	NA	NA	NA
S38	AUDIO_MCK	MCLK_OUT0	MCLK_OUT0/ BD4	I, 1.8V CMOS	Master Clock for Audio codec
S39	I2S0_LRCK	SAI1_TXFS	SAI1_TXFS/ AV2	I, 1.8V CMOS	Serial Audio Interface Channel1 Frame Sync /Left Right Clock
S40	I2S0_SDOUT	SAI1_TXD	SAI1_TXD/ AU1	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Output
S41	I2S0_SDIN	SAI1_RXD	SAI1_RXD/ AV4	O, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
S42	I2S0_CK	SAI1_TXC	SAI1_TXC/ AU5	I, 1.8V CMOS	Serial Audio Interface Channel1 Clock
S43	ESPI_ALERT0#	NC	NA	NA	NA
S44	ESPI_ALERT1#	NC	NA	NA	NA

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S45	RSVD2	NC	NA	NA	NA
S46	RSVD3	NC	NA	NA	NA
S47	GND	GND	NA	Power	Ground.
S48	I2C_GP_CK	DMA_I2C1_SCL	GPT0_CLK / AY52	I, 1.8V CMOS	General Purpose I2C Clock
S49	I2C_GP_DAT	DMA_I2C1_SDA	GPT0_CAPTURE / AV52	IO, 1.8V CMOS	General Purpose I2C Data
S50	HDA_SYNC / I2S2_LRCK	AUD_SAI0_TXFS(SPI 2_CS1)	SPI2_CS1/ AY2	I, 1.8V CMOS	Serial Audio Interface Channel0 Left Right Clock
S51	HDA_SDO / I2S2_SDOUT	AUD_SAI0_TXD	SPI0_SDO / AY6	I, 1.8V CMOS	Serial Audio Interface Channel0 Data Output
S52	HDA_SDI / I2S2_SDIN	AUD_SAI0_RXD	SPI0_SDI / BA5	O, 1.8V CMOS	Serial Audio Interface Channel0 Data Input
S53	HDA_CK / I2S2_CK	AUD_SAI0_TXC	SPI0_CS1 / BA3	I, 1.8V CMOS	Serial Audio Interface Channel0 Clock
S54	SATA_ACT#	GPIO_SATA_ACT#(G PIO1_18)	MIPI_DSI0_GPIO0_ 00/BD30	I, 3.3V CMOS	SATA Activity indication
S55	USB5_EN_OC#	NC	NA	NA	NA
S56	ESPI_IO_2	QSPI1A_DATA2	QSPI1A_DATA2/ E13	IO, 1.8V CMOS	NC. *Note: when used as QSPI, it will act as QSPI1A_ DATA2*
S57	ESPI_IO_3	QSPI1A_DATA3	QSPI1A_DATA3/ E11	IO, 1.8V CMOS	NC *Note: when used as QSPI, it will act as QSPI1A_ DATA3*
S58	ESPI_RESET#	QSPI1A_RESET(GPIO 4_22)	QSPI1A_DQS/ H12	I, 1.8V CMOS	NC *Note: when used as QSPI, it will act as QSPI1A_ RESET*
S59	USB5+	NC	NA	NA	NA
S60	USB5-	NC	NA	NA	NA
S61	GND	GND	NA	Power	Ground.
S62	USB3_SSTX+	USB3_HUB2_TXP	NA	I, USB SS	USB3.0 Port3 Transmit Plus *Note: Connected to USB Hub*
S63	USB3_SSTX-	USB3_HUB2_TXM	NA	I, USB SS	USB3.0 Port3 Transmit Minus *Note: Connected to USB Hub*
S64	GND	GND	NA	Power	Ground.
S65	USB3_SSRX+	USB3_HUB2_RXP	NA	O, USB SS	USB3.0 Port3 Receive Plus *Note: Connected to USB Hub*
S66	USB3_SSRX-	USB3_HUB2_RXM	NA	O, USB SS	USB3.0 Port3 Receive Minus *Note: Connected to USB Hub*
S67	GND	GND	NA	Power	Ground.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S68	USB3+	USB_HUB2OUT_DP	NA	IO, USB HS	USB Port3 Data Plus *Note: Connected to USB Hub*
S69	USB3-	USB_HUB2OUT_DM	NA	IO, USB HS	USB Port3 Data Minus *Note: Connected to USB Hub*
S70	GND	GND	NA	Power	Ground.
S71	USB2_SSTX+	USB3_HUB1_TXP	NA	I, USB SS	USB3.0 Port2 Transmit Plus *Note: Connected to USB Hub*
S72	USB2_SSTX-	USB3_HUB1_TXM	NA	I, USB SS	USB3.0 Port2 Transmit Minus *Note: Connected to USB Hub*
S73	GND	GND	NA	Power	Ground.
S74	USB2_SSRX+	USB3_HUB1_RXP	NA	O, USB SS	USB3.0 Port2 Receive Plus *Note: Connected to USB Hub*
S75	USB2_SSRX-	USB3_HUB1_RXM	NA	O, USB SS	USB3.0 Port2 Receive Minus *Note: Connected to USB Hub*
KEY					
S76	PCIE_B_RST#	PCIE_B_RST_B(GPIO5_00)	PCIE_CTRL1_PERST_B/G25	I, 3.3V CMOS	PCIe 1 RESET OUT
S77	PCIE_C_RST#	NC	NA	NA	NC
S78	PCIE_C_RX+	NC	NA	NA	NC
S79	PCIE_C_RX-	NC	NA	NA	NC
S80	GND	GND	NA	Power	Ground.
S81	PCIE_C_TX+	NC	NA	NA	NC
S82	PCIE_C_TX-	NC	NA	NA	NC
S83	GND	GND	NA	Power	Ground.
S84	PCIE_B_REFCK+	PCIE_B_REFCLK_P	NA	I, PCIe	PCIe1 Clock Positive
S85	PCIE_B_REFCK-	PCIE_B_REFCLK_N	NA	I, PCIe	PCIe1 Clock Negative
S86	GND	GND	NA	Power	Ground.
S87	PCIE_B_RX+	PCIE1_B_RX0_P	PCIE1_RX0_P/A21	O, PCIe	PCIE1 Receiver Positive
S88	PCIE_B_RX-	PCIE1_B_RX0_N	PCIE1_RX0_N/B22	O, PCIe	PCIE1 Receiver Negative
S89	GND	GND	NA	Power	Ground.
S90	PCIE_B_TX+	PCIE1_B_TX0_P	PCIE1_TX0_P/B24	I, PCIe	PCIE1 Transmitter Positive
S91	PCIE_B_TX-	PCIE1_B_TX0_N	PCIE1_TX0_N/C25	I, PCIe	PCIE1 Transmitter Negative
S92	GND	GND	NA	Power	Ground.
S93	DP0_LANE0+	HDMI_TX0_DATA2_P/EDP0_P	HDMI_TX0_DATA2_EDP0_P/BL9	I, DP	NC. *Note: Optionally connected to Display Port Lane 0 Positive*
S94	DP0_LANE0-	HDMI_TX0_DATA2_N/EDP0_N	HDMI_TX0_DATA2_EDP0_N/BM8	I, DP	NC.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: Optionally connected to Display Port Lane 0 Negative
S95	DP0_AUX_SEL	GPIO3_23	ADC_IN5/ AR7	IO, 1.8V CMOS	GPIO3_23 is connected.
S96	DP0_LANE1+	HDMI_TX0_DATA1_P/EDP1_P	HDMI_TX0_DATA1_EDP1_P/BL7	I, DP	NC. *Note: Optionally connected to Display Port Lane 1 Positive*
S97	DP0_LANE1-	HDMI_TX0_DATA1_N/EDP1_N	HDMI_TX0_DATA1_EDP1_N/BM6	I, DP	NC. *Note: Optionally connected to Display Port Lane 1 Negative*
S98	DP0_HPD	GPIO3_22	ADC_IN4/ AN9 or HDMI_TX0_HPD/ BH8	IO, 1.8V CMOS	Default GPIO3_22 is connected. *Note: If Display port is used SMARC Pin S98 must be connected to HDMI_TX0_HPD Pin*
S99	DP0_LANE2+	HDMI_TX0_DATA0_P/EDP2_P	HDMI_TX0_DATA0_EDP2_P/BL5	I, DP	NC. *Note: Optionally connected to Display Port Lane 2 Positive*
S100	DP0_LANE2-	HDMI_TX0_DATA0_N/EDP2_N	HDMI_TX0_DATA0_EDP2_N/BM4	I, DP	NC. *Note: Optionally connected to Display Port Lane 2 Negative*
S101	GND	GND	NA	Power	Ground.
S102	DP0_LANE3+	HDMI_TX0_CLK_P/EDP3_P	HDMI_TX0_CLK_EDP3_P/BL3	I, DP	NC. *Note: Optionally connected to Display Port Lane 3 Positive*
S103	DP0_LANE3-	HDMI_TX0_CLK_N/EDP3_N	HDMI_TX0_CLK_EDP3_N/BK2	I, DP	NC. *Note: Optionally connected to Display Port Lane 3 Negative*
S104	USB3_OTG_ID	USB_OTG1_ID	NA	-	NC.
S105	DP0_AUX+	HDMI_TX0_CTRL_CLK/_AUX_P	HDMI_TX0_AUX_P/ BH2	I, DP	NC. *Note: Optionally connected to Display Port AUX Positive*

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S106	DP0_AUX-	HDMI_TX0_CTRL_DAT/_AUX_N	HDMI_TX0_AUX_N /BG3	I, DP	NC. *Note: Optionally connected to Display Port AUX Negative*
S107	LCD1_BKLT_EN	LCD1_BKLT_EN(GPIO1_15)	LVDS1_I2C1_SDA/ BN35	I, 1.8V CMOS	LCD1 Backlight Enable
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS0/DSI1_CH1_CLK_P	MIPI_DSI1_CLK_P / BG31 or LVDS1_CH1_CLK_P / BH46	I, DIFF	MIPI DSI1 differential Clock positive *Note: Optionally connected to LVDS0_CH1 differential Clock positive*
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS0/DSI1_CH1_CLK_N	MIPI_DSI1_CLK_N / BH30 or LVDS1_CH1_CLK_N / BG45	I, DIFF	MIPI DSI1 differential Clock negative *Note: Optionally connected to LVDS0_CH1 differential Clock negative*
S110	GND	GND	NA	Power	Ground.
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS0/DSI1_CH1_TX0_P	MIPI_DSI1_DATA0_P /BG33 or LVDS0_CH1_TX0_P / BH44	I, DIFF	MIPI DSI1 differential data lane 0 positive *Note: Optionally connected to LVDS0_CH1 differential data lane 0 positive*
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS0/DSI1_CH1_TX0_N	MIPI_DSI1_DATA0_N/ BH32 or LVDS0_CH1_TX1_N / BG43	I, DIFF	MIPI DSI1 differential data Lane 0 negative *Note: Optionally connected to LVDS0_CH1 differential data Lane 0 negative*
S113	eDP1_HPD	GPIO3_24	ADC_IN6/ AL9	IO, 1.8V CMOS	GPIO3_24 is connected.
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS0/DSI1_CH1_TX1_P	MIPI_DSI1_DATA1_P /BG29 or LVDS0_CH1_TX1_P / BH42	I, DIFF	MIPI DSI1 differential data lane 1 positive *Note: Optionally connected to LVDS0_CH1 differential data lane 1 positive*
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS0/DSI1_CH1_TX1_N	MIPI_DSI1_DATA1_N/BH28 or LVDS0_CH1_TX1_N / BG41	I, DIFF	MIPI DSI1 differential data lane 1 negative *Note: Optionally connected to LVDS0_CH1 differential data lane 1 negative*
S116	LCD1_VDD_EN	LCD1_VDD_EN(GPIO1_14)	LVDS1_I2C1_SCL/ BD32	I, 1.8V CMOS	LCD1Power Enable

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS0/DSI1_CH1_TX2_P	MIPI_DSI1_DATA2_P /BG35 or LVDS0_CH1_TX2_P / BH40	I, DIFF	MIPI DSI1 differential data lane 2 positive *Note: Optionally connected to LVDS0_CH1 differential data lane 2 positive*
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS0/DSI1_CH1_TX2_N	MIPI_DSI1_DATA2_N/BH34 or LVDS0_CH1_TX2_N / BG39	I, DIFF	MIPI DSI1 differential data lane 2 negative *Note: Optionally connected to LVDS0_CH1 differential data lane 2 negative*
S119	GND	GND	NA	Power	Ground.
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS0/DSI1_CH1_TX3_P	MIPI_DSI1_DATA3_P /BG27 or LVDS0_CH1_TX3_P / BH38	I, DIFF	MIPI DSI1 differential data lane 3 positive *Note: Optionally connected to LVDS0_CH1 differential data lane 3 positive*
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS0/DSI1_CH1_TX3_N	MIPI_DSI1_DATA3_N/ BH26 or LVDS0_CH1_TX3_N / BG37	I, DIFF	MIPI DSI1 differential data lane 3 negative *Note: Optionally connected to LVDS0_CH1 differential data lane 3 negative*
S122	LCD1_BKLT_PWM	LCD1_BL_PWM(GPIO1_10)	LVDS1_GPIO00/ BD34	I, 1.8V CMOS	LCD0 Back Light Brightness control PWM
S123	RSVD8	NC	NA	NA	NA
S124	GND	GND	NA	Power	Ground.
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0/DSI0_CH0_TX0_P	MIPI_DSI0_DATA0_P /BK28 or LVDS0_CH0_TX0_P / BM42	I, DIFF	MIPI DSI0 differential data lane 0 positive *Note: Optionally connected to LVDS0_CH0 differential data lane 0 positive*
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0/DSI0_CH0_TX0_N	MIPI_DSI0_DATA0_N/ BM28 or LVDS0_CH0_TX0_N / BK42	I, DIFF	MIPI DSI0 differential data lane 0 negatives *Note: Optionally connected to LVDS0_CH0 differential data lane 0 negative*
S127	LCD0_BKLT_EN	LCD0_1_EN(GPIO1_08)	LVDS0_I2C1_SCL/ BE37	I, 1.8V CMOS	LCD0 Backlight Enable
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0/DSI0_CH0_TX1_P	MIPI_DSI0_DATA1_P /BK26 or	I, DIFF	MIPI DSI0 differential data lane 1 positive

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
			LVDS0_CH0_TX1_P / BN43		*Note: Optionally connected to LVDS0_CH0 differential data lane 1 positive*
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0/DSI0_CH0_TX1_N	MIPI_DSI0_DATA1_N/ BM26 or LVDS0_CH0_TX1_N / BL43	I, DIFF	MIPI DSI0 differential data lane 1 negative *Note: Optionally connected to LVDS0_CH0 differential data lane 1 negative*
S130	GND	GND	NA	Power	Ground.
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0/DSI0_CH0_TX2_P	MIPI_DSI0_DATA2_P /BL29 or LVDS0_CH0_TX2_P / BM44	I, DIFF	MIPI DSI0 differential data lane 2 positive *Note: Optionally connected to LVDS0_CH0 differential data lane 2 positive*
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0/DSI0_CH0_TX2_N	MIPI_DSI0_DATA2_N/ BN29 or LVDS0_CH0_TX2_N / BK44	I, DIFF	MIPI DSI0 differential data lane 2 negatives *Note: Optionally connected to LVDS0_CH0 differential data lane 2 negative*
S133	LCD0_VDD_EN	LCD0_VDD_EN(GPIO1_09)	LVDS0_I2C1_SDA/ BE35	I, 1.8V CMOS	LCD0 Power Enable
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0/DSI0_CH0_CLK_P	MIPI_DSI0_CLK_P / BL27 or LVDS0_CH0_CLK_P / BN41	I, DIFF	MIPI DSI0 differential Clock positive *Note: Optionally connected to LVDS0_CH0 differential Clock positive*
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0/DSI0_CH0_CLK_N	MIPI_DSI0_CLK_N / BN27 or LVDS0_CH0_CLK_N / BL41	I, DIFF	MIPI DSI0 differential Clock negative *Note: Optionally connected to LVDS0_CH0 differential Clock negative*
S136	GND	GND	NA	Power	Ground.
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0/DSI0_CH0_TX3_P	MIPI_DSI0_DATA3_P /BL25 or LVDS0_CH0_TX3_P / BN45	I, DIFF	MIPI DSI0 differential data lane 3 positive *Note: Optionally connected to LVDS0_CH0 differential data lane 3 positive*
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0/DSI0_CH0_TX3_N	MIPI_DSI0_DATA3_N/BN25 or	I, DIFF	MIPI DSI0 differential data lane 3 negative

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
			LVDS0_CH0_TX3_N / BL45		*Note: Optionally connected to LVDS0_CH0 differential data lane 3 negative*
S139	I2C_LCD_CK	LVDS_I2C_SCL	LVDS0_I2C0_SCL/ BD38	I, 1.8V CMOS	I2C CLK for Display and Touch
S140	I2C_LCD_DAT	LVDS_I2C_SDA	LVDS_I2C_SDA/ BD36	IO, 1.8V CMOS	I2C DATA for Display and Touch
S141	LCD0_BKLT_PWM	LCD0_BL_PWM(GPIO1_04)	LVDS0_GPIO00/ BE39	I, 1.8V CMOS	LCD0 Back Light Brightness control PWM
S142	RSVD9	NC	NA	NA	NA
S143	GND	GND	NA	Power	Ground.
S144	eDP0_HPD	GPIO3_25	ADC_IN7/ AP6	IO, 1.8V CMOS	GPIO3_25 is connected.
S145	WDT_TIME_OUT#	SCU_WDOG_OUT	SCU_WDOG_OUT / BB50	I, 1.8V CMOS	NC.
S146	PCIE_WAKE#	PCIE_A_WAKE_B(GPIO4_28)	PCIE_CTRL0_WAKE_B/A15	O, 3.3V CMOS	PCIe wake up interrupt to host
S147	VDD_RTC	VDD_RTC	NA	O, 3V Power	RTC backup power. Connected to RTC battery holder.
S148	LID#	NC	NA	-	NC.
S149	SLEEP#	NC	NA	-	NC.
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	O, 5V CMOS 10K PU	Power bad indication from Carrier board. Module and Carrier power supplies shall not be enabled while this signal is held low by the Carrier.
S151	CHARGING#	NC	NA	-	NC.
S152	CHARGER_PRSNT#	NC	NA	-	NC.
S153	CARRIER_STBY#	CARRIER_STBY#	NA	I, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_STBY# goes High.
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	NA	I, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_PWR_ON is High
S155	FORCE_RECOV#	FORCE_RECOV#	NA	O, 1.8V CMOS 10K PU	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked.
S156	BATLOW#	NC	NA	-	NC.
S157	TEST#	TEST_MODE_SELECT	TEST_MODE_SELECT/BC49	O, 1.8V CMOS 2.2K PD	Only for Module vendor specific use. Connected to 4bit DIP switch (SW6).
S158	GND	GND	NA	Power	Ground.

2.4 Serial Interface Features

2.4.1 Debug UART Interface

The i.MX8 QM/QP SMARC development board supports debug interface through i.MX8 CPU's UART4 interface. This UART4 signals from SMARC MXM connector is connected to UART to USB Convertor "FT232RQ" via 1.8V to 3.3V level Translator and FT232RQ is connected to USB Micro AB Connector (J22). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

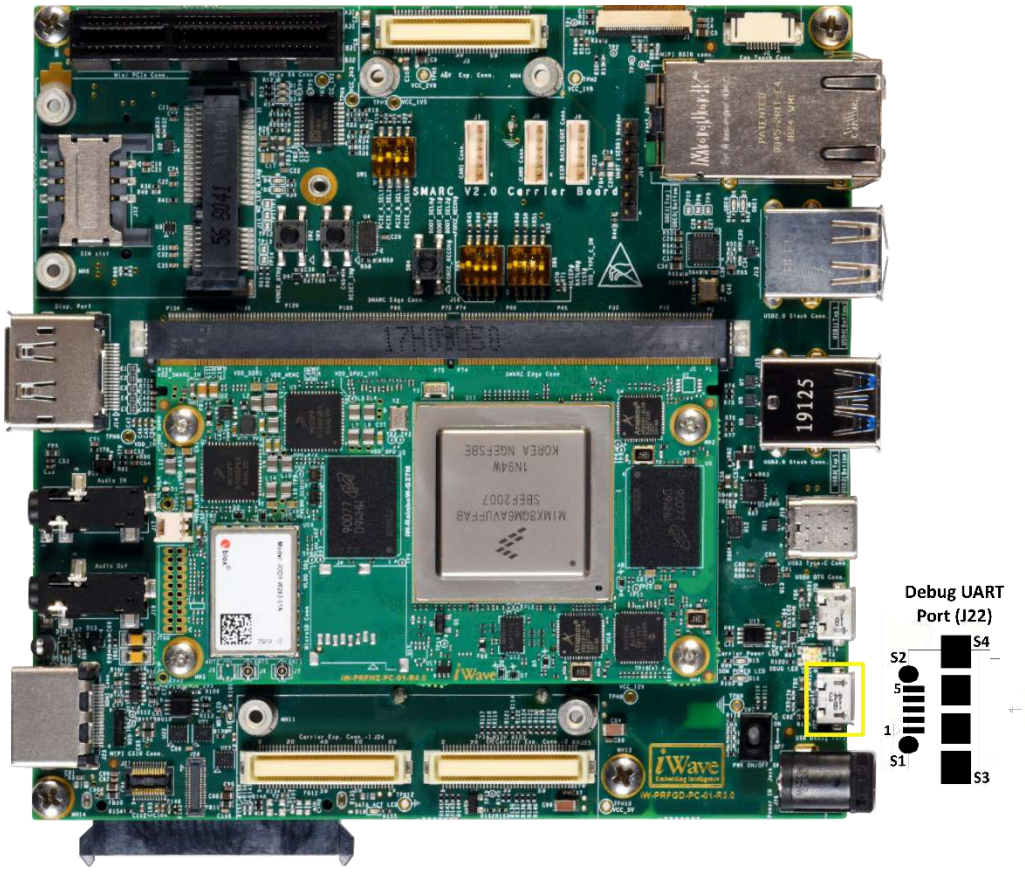


Figure 3: Debug UART Port

2.4.2 Data UART Interface

The i.MX8 QM/QP SMARC carrier board supports full functional Data UART interface through i.MX8 CPU's UART0 interface. This UART0 signals from SMARC MXM connector is connected to 6pin Header (J10) via 1.8 to 3.3V volatge level translator for easy accessibilty. This Data UART header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

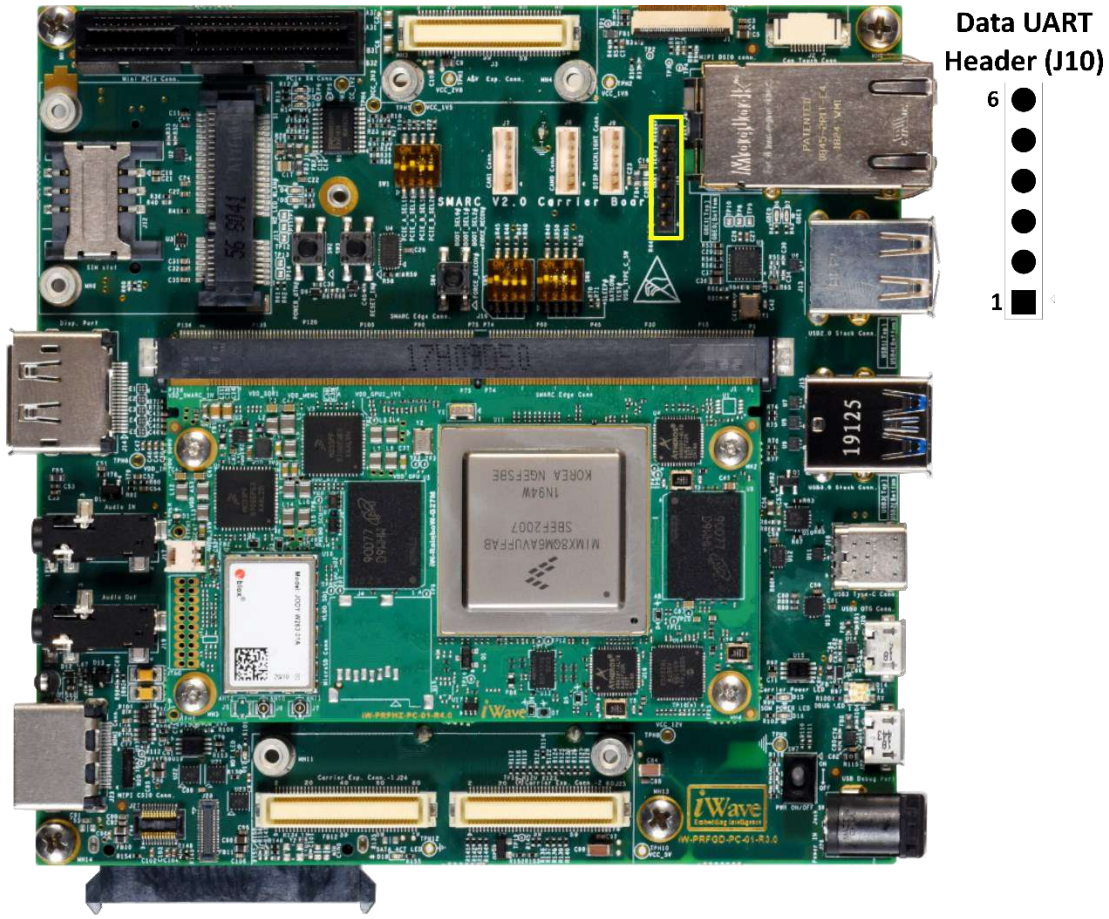


Figure 4: Data UART Header

Table 4: Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	UART_CTS#	UART0_CTS_B	I, 3.3V CMOS	UART0 interface Clear to Send signal.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART_RXD	UART0_RX	I, 3.3V CMOS	UART0 interface Receive signal.
5	UART_TXD	UART0_TX	O, 3.3V CMOS	UART0 interface Transmit signal.
6	UART_RTS#	UART0_RTS_B	O, 3.3V CMOS	UART0 interface Ready to Send signal.

2.5 High Speed Interface Features

2.5.1 PCIe Interface

The i.MX8 QM/QP SMARC Development platform by default supports two PCIe Lanes PCIe_A and PCIe_B. PCIe_A lane supported through i.MX8 CPU's PCIe0 Interface and other PCIe_B lane supported through i.MX8 CPU's PCIe1 Interface

Both PCIe A & B signals of SMARC MXM connector are connected to separate 1:3 Multiplexer/Demultiplexer switch and the output of both the Multiplexer/Demultiplexer switch are connected to PCIex4 connector, Mini PCIe connector and M.2 connector. The selection between the connector can be done by setting the 4th bit of Board configuration switch (SW1) to appropriate position. PCIe A reference clock from SMARC MXM connector is connected to 1:2 output clock buffer and then connected to PCIex4 connector and Mini PCIe connector for clock reference. Whereas PCIe B reference clock is directly connected to M.2 Connector.

Refer Dip Switch (SW1) Settings in "Table 14: Board Configuration Switch" for more details on selecting PCIe connector.

PCIex4 Connector: PCIeX4 connector (J4) is physically located at the top of the board as shown below

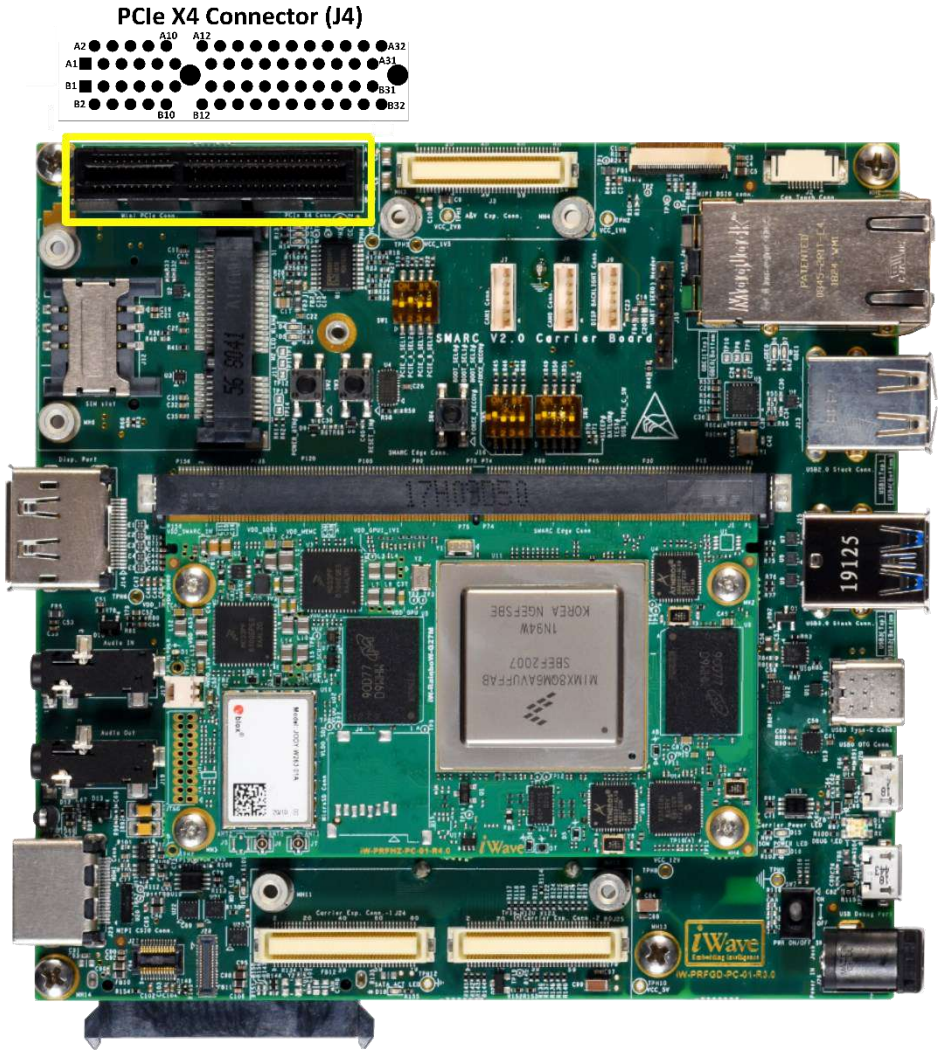


Figure 5: PCIex4 Connector

Table 5: PCIex4 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	PRSNT1#	PRSNT1#	O, 3.3V CMOS	Default Grounded.
B1	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B3	RSVD1	NC	-	NC, Reserved Pin.
A4	GND	GND	Power	Ground.
B4	GND	GND	Power	Ground.
A5	TCK	NC	-	NC.
B5	SMCLK	DMA_I2C1_SCL	O, 3.3V CMOS	SMB Clock.
A6	TDI	NC	-	NC.
B6	SMDAT	DMA_I2C1_SDA	IO, 3.3V CMOS	SMB Data.
A7	TDO	NC	-	NC.
B7	GND	GND	Power	Ground.
A8	TMS	NC	-	NC.
B8	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
A9	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NC	-	NC.
A10	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
B10	3V3AUX	VAUX_3V3	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	PCIE_A_RST_B(GPIO4_29	O, 3.3V CMOS	PCIe PERST#.
B11	WAKE#	PCIE_A_WAKE_B(GPIO4_28)	O, 3.3V CMOS	PCIe WAKE#.
A12	GND	GND	Power	Ground.
B12	RSVD2	NC	-	NC, Reserved Pin.
A13	PCIe0_CLK+	PCIe0_CLK+	O, PCIe	PCIe Clock positive.
B13	GND	GND	Power	Ground.
A14	PCIe0_CLK-	PCIe0_CLK-	O, PCIe	PCIe Clock negative.
B14	PCIE0_TX+	PCIEA_TX+	O, PCIe	PCIe Port 0 Transmit pair positive. *Note: Refer SW1 setting from Table 14 to support PCIE0_TX.*
A15	GND	GND	Power	Ground.
B15	PCIE0_TX-	PCIEA_TX-	O, PCIe	PCIe Port 0 Transmit pair negative. *Note: Refer SW1 setting from Table 14 to support PCIE0_TX.*
A16	PCIE0_RX+	PCIEA_RX+	I, PCIe	PCIe Port 0 Receive pair positive. *Note: Refer SW1 setting from Table 14 to support PCIE0_RX.*
B16	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A17	PCIE0_RX-	PCIEA_RX-	I, PCIe	PCIe Port 0 Receive pair negative. *Note: Refer SW1 setting from table to support PCIE0_RX.*
B17	PRSNT2#	NC	-	NC.
A18	GND	GND	Power	Ground.
B18	GND	GND	Power	Ground.
A19	RSVD	NC	-	NC, Reserved Pin.
B19	PCIE1_TX+	PCIEB_TX+	O, PCIe	PCIe Port 1 Transmit pair positive. *Note: Refer SW1 setting from Table 14 for support PCIE1_TX.*
A20	GND	GND	Power	Ground.
B20	PCIE1_TX-	PCIEB_TX-	O, PCIe	PCIe Port 1 Transmit pair negative. *Note: Refer SW1 setting from Table 14 for support PCIE1_TX.*
A21	PCIE1_RX+	PCIEB_RX+	I, PCIe	PCIe Port 1 Receive pair positive. *Note: Refer SW1 setting from Table 14 for support PCIE1_RX.*
B21	GND	GND	Power	Ground.
A22	PCIE1_RX-	PCIEB_RX-	I, PCIe	PCIe Port 1 Receive pair negative. *Note: Refer SW1 setting from Table 14 for support PCIE1_RX.*
B22	GND	GND	Power	Ground.
A23	GND	GND	Power	Ground.
B23	PCIE2_TX+	NC	-	NC, PCIe Port 2 Transmit pair positive.
A24	GND	GND	Power	Ground.
B24	PCIE2_TX-	NC	-	NC, PCIe Port 2 Transmit pair negative.
A25	PCIE2_RX+	NC	-	NC, PCIe Port 2 Receive pair positive.
B25	GND	GND	Power	Ground.
A26	PCIE2_RX-	NC	-	NC, PCIe Port 2 Receive pair negative.
B26	GND	GND	Power	Ground.
A27	GND	GND	Power	Ground.
B27	PCIE3_TX+	NC	-	NC, PCIe Port 3 Transmit pair positive.
A28	GND	GND	Power	Ground.
B28	PCIE3_TX-	NC	-	NC, PCIe Port 3 Transmit pair negative.
A29	PCIE3_RX+	NC	-	NC, PCIe Port 3 Receive pair positive.
B29	GND	GND	Power	Ground.
A30	PCIE3_RX-	NC	-	NC, PCIe Port 3 Receive pair negative.
B30	RSVD	NC	-	NC, Reserved Pin.
A31	GND	GND	Power	Ground.
B31	PRSNT3#	NC	-	NC.
A32	RSVD	NC	-	NC, Reserved Pin.
B32	GND	GND	Power	Ground.

Mini PCIe Connector: Mini PCIe connector (J11) is physically located at the top of the board as shown below.

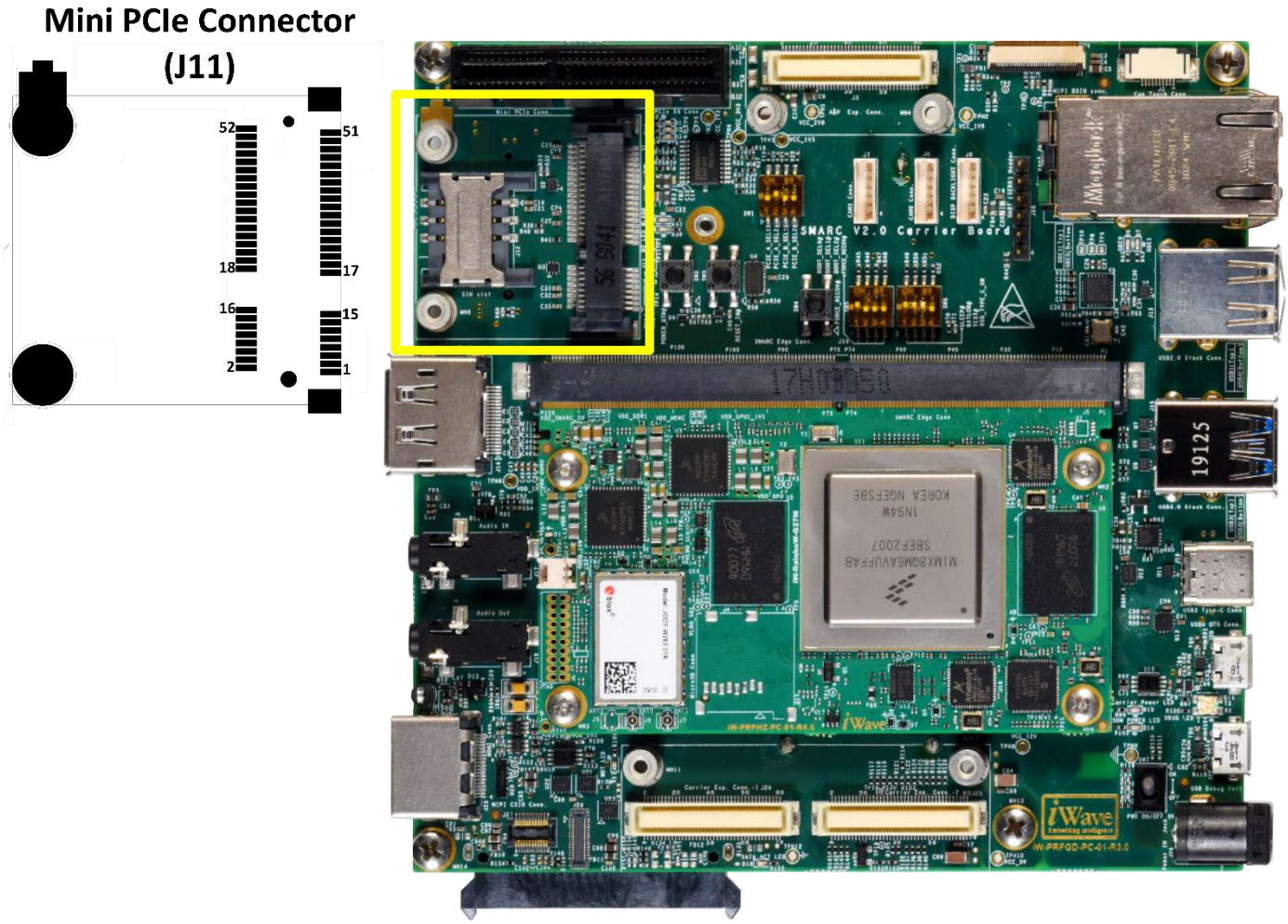


Figure 6: Mini PCIe Connector

Table 6: Mini-PCIe Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	PCIe_WAKE	PCIE_A_WAKE_B(GPIO4_28)	O, 3.3V CMOS	PCIe WAKE#.
2	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	COEX1	NC.	-	NC.
4	GND	GND	Power	Ground.
5	COEX2	NC.	-	NC.
6	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
7	CLK_REQ#	CLK_REQ#	O, 3.3V CMOS	Used to enable Clock.
8	UIM_PWR	NC.	-	NC.
9	GND	GND	Power	Ground.
10	UIM_DATA	NC.	-	NC.
11	REFCLK-	PCIe_REFCLK_DM	O, DIFF	PCIe Clock negative.
12	UIM_CLK	NC.	-	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
13	REFCLK+	PCIe_REFCLK_DP	O, DIFF	PCIe Clock positive.
14	UIM_RESET	NC.	-	NC.
15	GND	GND	Power	Ground.
16	UIM_VPP	NC.	-	NC.
17	RESERVED	NC.	-	NC.
18	GND	GND	Power	Ground.
19	RESERVED	NC.	-	NC.
20	W_DISABLEG	SMARC_GPIO_10(GPIO0_04)	O, 3.3V CMOS	Wireless Disable.
21	GND	GND	Power	Ground.
22	PERST#	PCIE_A_RST_B(GPIO4_29	O, 3.3V CMOS	PCIe Reset.
23	PCIE0_RX-	PCIE0_RX-	I, DIFF	PCIe Port0/1 Receive pair negative. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_RX.*
24	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
25	PCIE0_RX+	PCIE0_RX+	I, DIFF	PCIe Port0/1 Receive pair positive. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_RX*
26	GND	GND	Power	Ground.
27	GND	GND	Power	Ground.
28	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
29	GND	GND	Power	Ground.
30	SMB_CLK	DMA_I2C1_SCL	O, 3.3V CMOS	SMB Clock.
31	PCIE0_TX-	PCIE0_TX-	O, DIFF	PCIe Port0/1 Transmit pair negative. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_TX*
32	SMB_DATA	DMA_I2C1_SDA	IO, 3.3V CMOS	SMB DATA.
33	PCIE0_TX+	PCIE0_TX+	O, DIFF	PCIe Port0/1 Transmit pair positive. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_TX*
34	GND	GND	Power	Ground.
35	GND	GND	Power	Ground.
36	USB_D-	USB_HUBOUT2_DM	IO, DIFF	USB Data negative
37	GND	GND	Power	Ground.
38	USB_D+	USB_HUBOUT2_DP.	IO, DIFF	USB Data Positive
39	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
40	GND	GND	Power	Ground.
41	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
42	LED_WWAN#	LED_WWAN#	O, 3.3V CMOS	Connected to D3 Green LED cathode.
43	GND	GND	Power	Ground.
44	LED_WLAN#	LED_WLAN#	O, 3.3V CMOS	Connected to D2 Green LED cathode.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
45	RESERVED	NC.	-	NC.
46	LED_WPAN#	LED_WPAN#	O, 3.3V CMOS	Connected to D1 Green LED cathode.
47	RESERVED	NC.	-	NC.
48	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
49	RESERVED	NC.	-	NC.
50	GND	GND	Power	Ground.
51	RESERVED	NC.	-	NC.
52	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.

M.2 Connector: The i.MX8 SMARC carrier board supports M.2 Key-E Connector (J31) and is placed at the bottom side of the board. SPI, SDIO, PCIe, I2S, I2C, and UART interface are optionally supported over M.2 Connector.

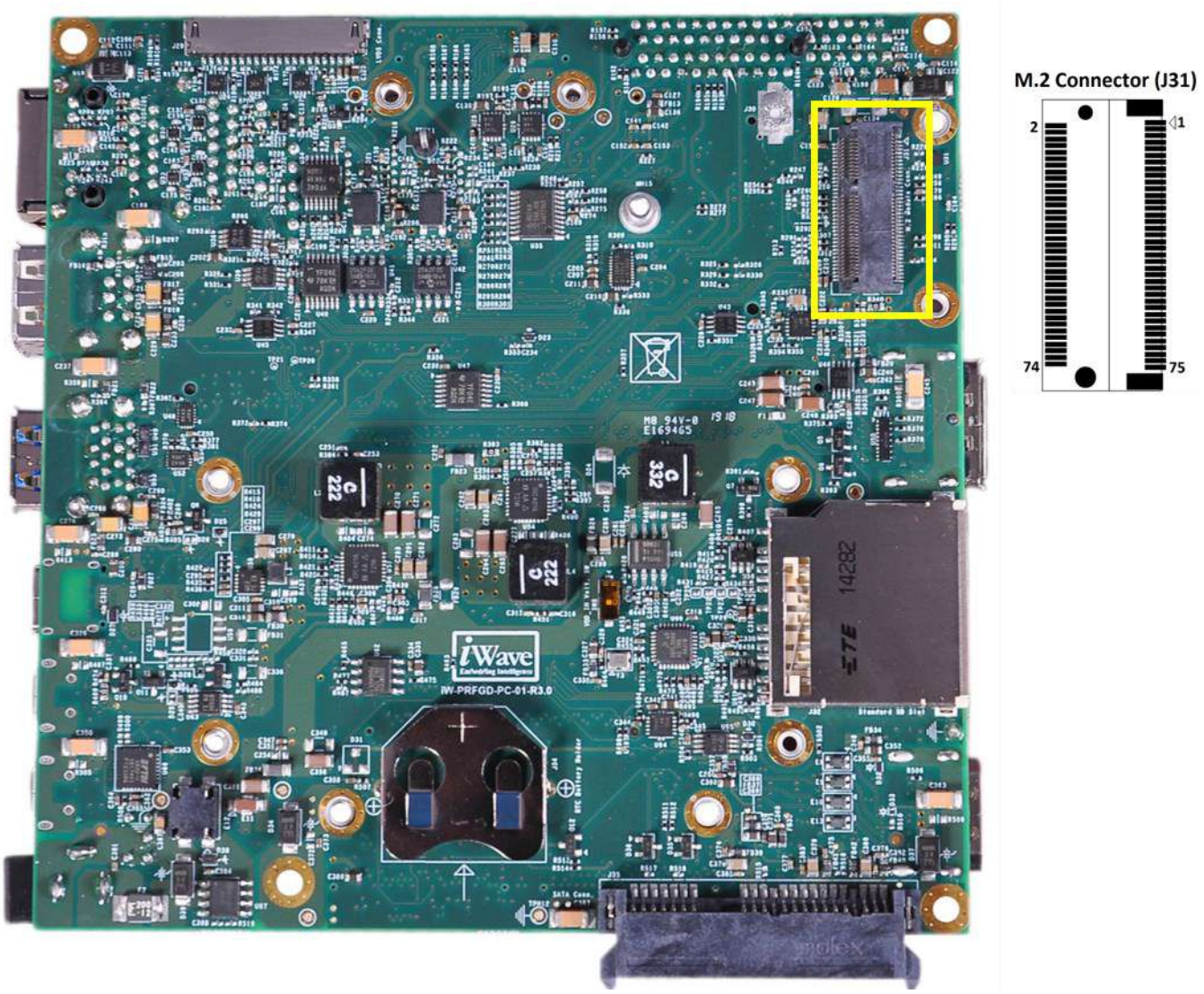


Figure 7: M.2 Connector

Refer below table for M.2 connector pinout details.

Table 7: M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	USB_DP	NC	NA	NC. *Note: To support USB2.0 refer* ***Note-1***
4	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	USB_DM	NC	NA	NC. *Note: To support USB2.0 refer* ***Note-1***
6	LED_WLAN#	M2_LED_WLAN#	O, 3.3V CMOS	Connected to D5 Green LED cathode.
7	GND	GND	Power	Ground.
8	I2S SCK	M2_I2S_2_SCK	O, 1.8V CMOS	M.2 Module I2S Clock *Note: This pin is connected from SMARC Edge connector S53rd pin for I2S2_CK. This pin is also connected to A&V Expansion Conn connector (J3) 30th pin through R165 resistor.*
9	SDIO CLK	NC	NA	NC. *Note: To support SD interface refer* ***Note-2***
10	I2S WS	M2_MI2S_2_WS	O, 1.8V CMOS	M.2 Module I2S Word Select. *Note: This pin is connected from SMARC Edge connector S50th pin for I2S2_LRCK. This pin is also connected to A&V Expansion Conn connector (J3) 36th pin through R168 resistor.*
11	SDIO CMD	NC	NA	NC. *Note: To support SD interface refer* ***Note-2***
12	I2S SD_IN	M2_MI2S_2_D0	IO, 1.8V CMOS	M.2 Module I2S SD_IN *Note: This pin is connected from SMARC Edge connector S51st pin for I2S2_SDOUT. This pin is also connected to A&V Expansion Conn connector (J3) 32nd pin through R166 resistor.*
13	SDIO DATA0	NC	NA	NC. *Note: To support SD interface refer* ***Note-2***
14	I2S SD_OUT	M2_MI2S_2_D1	IO, 1.8V CMOS	M.2 Module I2S SD_OUT *Note: This pin is connected from SMARC Edge connector S52nd pin for I2S2_SDIN.*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				This pin is also connected to A&V Expansion Conn connector (J3) 34th pin through R167 resistor.
15	SDIO DATA1	NC	NA	NC. *Note: To support SD interface refer* ***Note-2***
16	LED_BT#	M2_LED_BT#	O, 3.3V CMOS	Connected to D4 Green LED cathode.
17	SDIO DATA2	NC	NA	NC. *Note: To support SD interface refer* ***Note-2****.*
18	GND	GND	Power	Ground.
19	SDIO DATA3	NC	NA	NC. *Note: To support SD interface refer* ***Note-2***
20	CB_PWR_ON	NC	NA	NC
21	SDIO WAKE#	NC	NA	NC. *Note: To support SD interface refer* ***Note-2***
22	UART0 RXD	SER2_RX	I, 1.8V CMOS	NC. *Note: M.2 UART Receive Signal. This signal is Connected to SMARC Edge P137th pin for SER2_RX. SER2 is optional in default SOM Configuration.*
23	SDIO RESET#	SDIO_RST#	NA	NC. *Note: Optionally connected to SMARC Edge P113th pin.*
24	NC1	NA	NA	NC.
25	NC2	NA	NA	NC.
26	NC3	NA	NA	NC.
27	NC4	NA	NA	NC.
28	NC5	NA	NA	NC.
29	NC6	NA	NA	NC.
30	NC7	NA	NA	NC.
31	NC8	NA	NA	NC.
32	UART0 TXD	SER2_TX	O, 1.8V CMOS	NC. *Note: M.2 UART Transmit Signal. This signal is Connected to SMARC Edge P136th pin for SER2_TX. SER2 is optional in default SOM Configuration.*
33	GND	GND	Power	Ground.
34	UART0 CTS	SER2_CTS#	I, 1.8V CMOS	NC. *Note: M.2 UART Clear to Send signal. This signal is Connected to SMARC Edge P139th pin for SER2_CTS#. SER2 is*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				optional in default SOM Configuration.
35	PETp0	PCIe_TX+	O, PCIe	PCIe Port 0/1 Transmit pair positive. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_TX*
36	UART0 RTS	SER2_RTS#	O, 1.8V CMOS	NC. *Note: M.2 UART Ready to Send signal. This signal is Connected to SMARC Edge P138th pin for SER2_RTS#. SER2 is optional in default SOM Configuration.*
37	PETn0	PCIe_TX-	O, PCIe	PCIe Port 0/1 Transmit pair negative. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_TX*
38	GPIO0	NA	IO, 3.3V CMOS	NC.
39	GND	GND	Power	Ground.
40	GPIO1	NA	IO, 3.3V CMOS	NC.
41	PERp0	PCIe_RX+	I, PCIe	PCIe Port 0/1 Receive pair positive. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_RX*
42	GPIO2	NA	IO, 3.3V CMOS	NC.
43	PERn0	PCIe_RX-	I, PCIe	PCIe Port 0/1 Receive pair negative. *Note: Refer SW1 setting from Table 14 for support PCIE0/1_RX*
44	COEX3(LTE_ACTIVE)	TP7	NA	Connected to Test Point.
45	GND	GND	Power	Ground.
46	COEX2(LTE_PRI)	TP12	NA	Connected to Test Point.
47	REFCLK+	REFCLK+	I, DIFF	100MHz Reference Clock for PCIe.
48	COEX2(LTEE_SYNC)	TP11	NA	Connected to Test Point
49	REFCLK-	REFCLK-	I DIFF	100MHz Reference Clock for PCIe.
50	SUSCLK(32KHz)	NA	NA	NC
51	GND	GND	Power	Ground.
52	PERST#	PCIe_A_RST#	O, 3.3V CMOS	M.2 PCIe Reset. *Note: This pin is optionally connected to SMARC Edge P75th pin for PCIe_A_RST#*
53	CLKREQ#	CLKREQ#	O, 3.3V CMOS	PCIe Reference Clock Request *Note: This pin should have Pull Down on Module to enable to CLK.*
54	BT_DISABLE#	SMARC_GPIO_10(GPIO0_04)	O, 3.3V CMOS	BT_DISABLE# *Note: This Pin is Connected to SMARC Edge P118th pin* SMARC_GPIO_10. *Also shared with W_DISABLE#*
55	PEWAKE#	PEWAKE#	O, 3.3V CMOS	NC Note: by default, connected to Mini PCIe connector

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
56	W_DISABLE#	SMARC_GPIO_10(GPIO0_04)	O, 3.3V CMOS	W_DISABLE. *This Pin is Connected to SMARC Edge P118th pin* SMARC_GPIO_10. *Also shared with* BT_DISABLE#
57	GND	GND	Power	Ground.
58	I2C_DATA	I2C_GP_CK_3V3	IO, 3.3V CMOS	I2C Data Signal. *Note: This Pin is Connected to SMARC Edge S49th pin I2C_GP_DAT via voltage level Translator.*
59	ADC4/ GPIO14	NA	NA	NC
60	I2C_CLK	I2C_GP_DAT_3V3	O, 3.3V CMOS	I2C Clock Signal. *Note: This Pin is Connected to SMARC Edge S48th pin I2C_GP_CK via voltage level Translator.*
61	ADC5 / GPIO15	NA	NA	NC.
62	SPI0_MOSI	ESPI_IO_0_3V3	O, 3.3V CMOS	SPI Master Out Slave In. *Note: This Pin is Connected to SMARC Edge P58th pin ESPI_IO_0 via voltage level Translator.*
63	GND	GND	Power	Ground.
64	SPI0_MISO	ESPI_IO_1_3V3	I, 3.3V CMOS	SPI Master in Slave Out. *Note: This Pin is Connected to SMARC Edge P57th pin ESPI_IO_1 via voltage level Translator.*
65	VBAT	NC	O, 3.3V Power	NC. *Note: Optionally connected to VDD_RTC*
66	SPI0_CLK	ESPI_CK_3V3	I, 3.3V CMOS	SPI Clock. *Note: This Pin is Connected to SMARC Edge P56th pin ESPI_CK via voltage level Translator*
67	Backup#	NC	I, 3.3V CMOS	NC
68	SPI0_CS0#	ESPI_CS0_N_3V3	O, 3.3V CMOS	SPI Chip Select0. *Note: This Pin is Connected to SMARC Edge P54th pin ESPI_CS0# via voltage level Translator*
69	GND	GND	Power	Ground.
70	SPI0_CS1#	ESPI_CS1_N_3V3	O, 3.3V CMOS	SPI Chip Select1. *Note: This Pin is Connected to SMARC Edge P55th pin ESPI_CS1# via voltage level Translator*
71	RESET_IN#	PCIe_A_RST#	I, 3.3V CMOS	Reset Input. *Note: This pin is connected to SMARC Edge P75th pin for PCIe_A_RST#*
72	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	Wake#	NA	NA	NC

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
74	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	GND	GND	Power	Ground.

Note-1: *USB signals are sharing between mini-PCIe and M.2 Connector. To support USB at M.2 connector contact iWave support Team.*

Note-2: *SMARC SDIO interface is directly connected to Standard SD and optionally connected to M.2 Connector. To Support SDIO interface at M.2 connector contact iWave Support team.*

2.5.2 SATA Interface

The i.MX8 QM/QP SMARC carrier board supports SATA interface from PCIE_SATA0 of i.MX8 QM/QP processor using 22 pins SATA connector (J35). The SMARC carrier board also supports SATA activity LED (D18) on Top side of the board for SATA activity indication. This 22 Pins SATA connector is physically located at the bottom of the board.

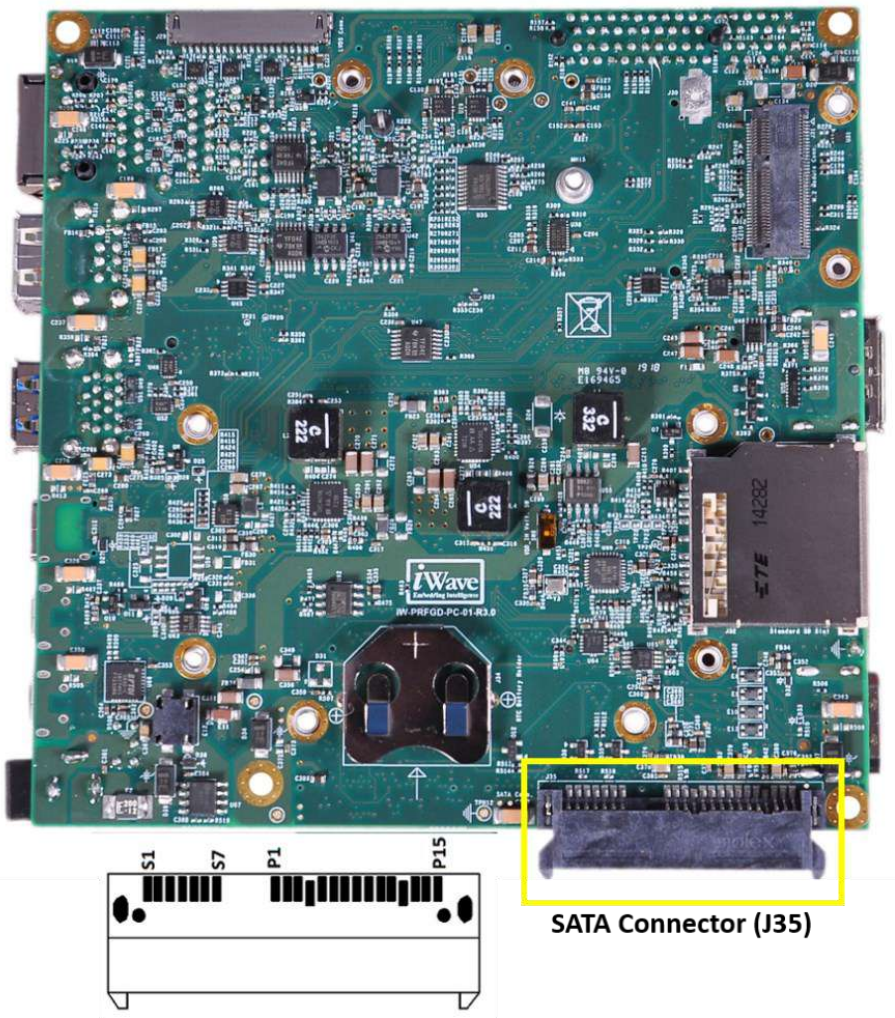


Figure 8: SATA Connector

Refer below table for the pinout is listed of SATA connector.

Table 8: 22 pins SATA Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
S1	GND	GND	Power	Ground.
S2	SATA1_TXP	PCIE_SATA0_TX0_P	O, DIFF 0.022uF AC Coupled	SATA Transmit Differential pair positive.
S3	SATA1_TXN	PCIE_SATA0_TX0_N	O, DIFF 0.022uF AC Coupled	SATA Transmit Differential pair negative.
S4	GND	GND	Power	Ground.
S5	SATA1_RXN	PCIE_SATA0_RX0_N	I, DIFF 0.022uF AC Coupled	SATA Receive Differential pair negative.
S6	SATA1_RXP	PCIE_SATA0_RX0_P	I, DIFF 0.022uF AC Coupled	SATA Receive Differential pair positive.
S7	GND	GND	Power	Ground.
P1	V33	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
P2	V33	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
P3	V33	VCC_3V3	-	NC.
P4	GND	GND	Power	Ground.
P5	GND	GND	Power	Ground.
P6	GND	GND	Power	Ground.
P7	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P8	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P9	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P10	GND	GND	Power	Ground.
P11	DAS_DSS	NC	-	NC.
P12	GND	GND	Power	Ground.
P13	V12	VCC_12V	O, 12V Power	12V Supply Voltage.
P14	V12	VCC_12V	O, 12V Power	12V Supply Voltage.
P15	V12	VCC_12V	O, 12V Power	12V Supply Voltage.

2.5.3 USB3.0 Host Interface

The i.MX8 QM/QP SMARC development board supports Super Speed USB3.0 Host interface through on SOM USB3.0 Hub. This USB3.0 signals of SMARC USB2 and USB3 port from MXM connector is directly connected to bottom and top port of dual stack USB3.0 Type-A connector (J15) respectively. Also, USB2.0 signals of USB2 and USB3 Port of SMARC signals are connected to respective connector from 3.0 USB Hub used on SOM. The top port of J15 connector is shared with USB Type-C connector (J18).

The selection between USB Type C connector and top port of dual stack USB3.0 TypeA connector can be done by setting the 4th bit of Board configuration switch (SW6) to appropriate position. If the 4th bit of Board configuration switch (SW6) is set to OFF position, then USB3 port of SMARC MXM connector is connected to USB Type C connector. If the 4th bit of Board configuration switch (SW6) is set to ON position, then USB3 port of SMARC MXM connector is connected to top port of dual stack USB3.0 TypeA connector. Also USB2.0 signals of USB3 Port of SMARC MXM connector is connected to both these connectors.

To support double-way plug in on USB TypeC connector, USB3 signals are connected to FUSB340TMX USB3.0 switch and then connected to USB Type C connector. This USB3.0 switch port connection to Type C connector top or bottom is controlled through GPIO4 (P112nd pin) of the SMARC MXM connector.

The VBUS power of this USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of SMARC MXM connector USB2 and USB3 ports. This USB3.0 connector is physically located at the top of the board as shown below.

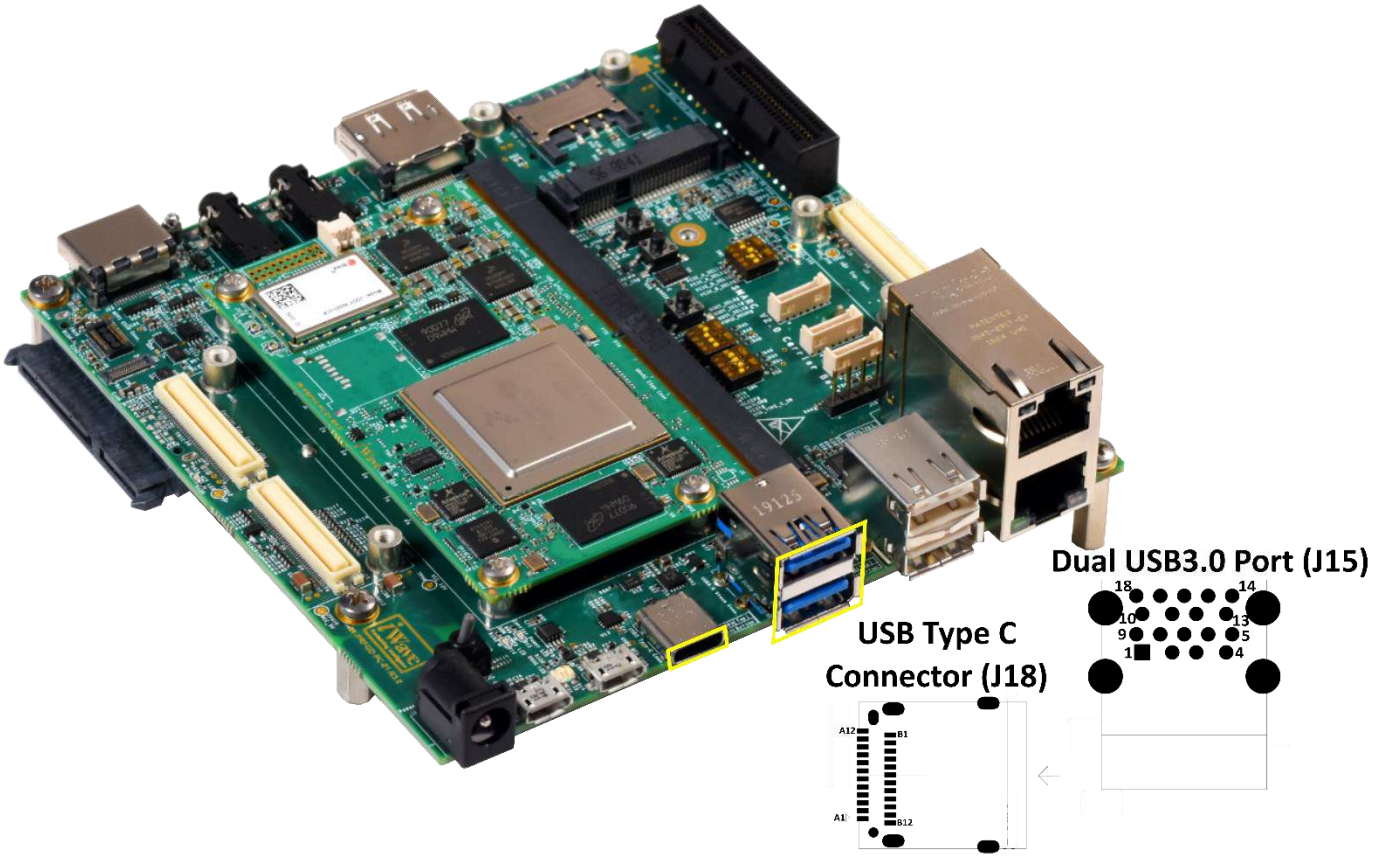


Figure 9: USB3.0 Host

2.6 Communication Interface Features

2.6.1 Gigabit Ethernet Interface

The i.MX8 QM/QP SMARC development board supports Dual Ethernet Port interface through on SOM Ethernet PHY which supports 10/100/1000Mbps Ethernet. The Ethernet PHY output signals from SMARC MXM connector GBE0 and GBE1 are directly connected to RJ45 Magjack (J6), Bottom & Top connector respectively. Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

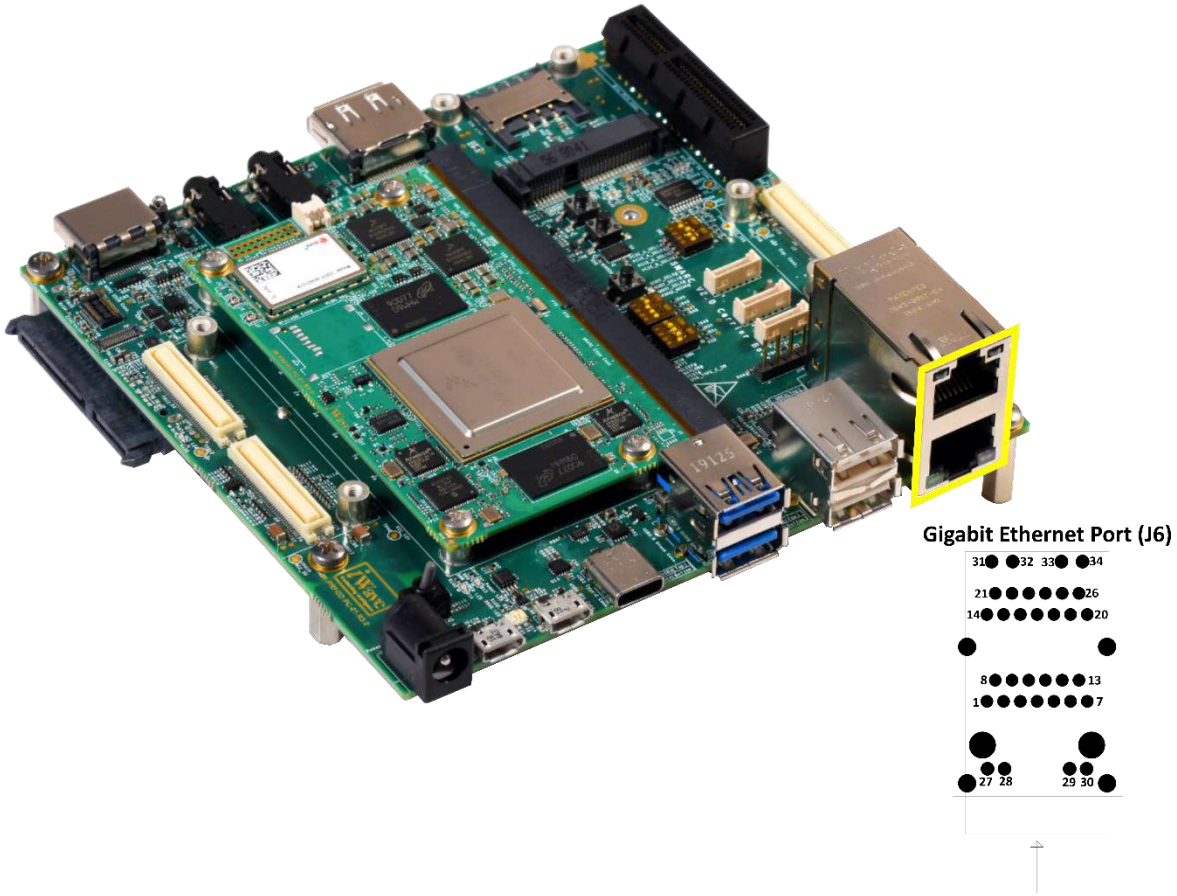


Figure 10: RJ45 Magjack

2.6.2 USB2.0 Host Interface

The i.MX8 QM/QP SMARC carrier board supports additional two USB2.0 Host interface through on SOM USB3.0 Hub via SMARC USB1 and USB4 ports. USB1 signals from the edge connector is connected to on board 1:2 USB hub. The primary port is directly connected to J13 TOP and secondary port is connected to mini-PCIe connector. Whereas USB4 port from the SMARC edge connector is directly connected to BOTTOM side of J13 connector.

The VBUS power of this USB2.0 connector is connected through current limit power switch and limit is set as 500mA. If connected USB2.0 device takes more than 500mA current, this power switch limits the current to constant mode

and sends the over current indication signal to the over current indicator pin of SMARC MXM connector USB1 and USB4 ports. This USB2.0 connector is physically located at the top of the board as shown below.

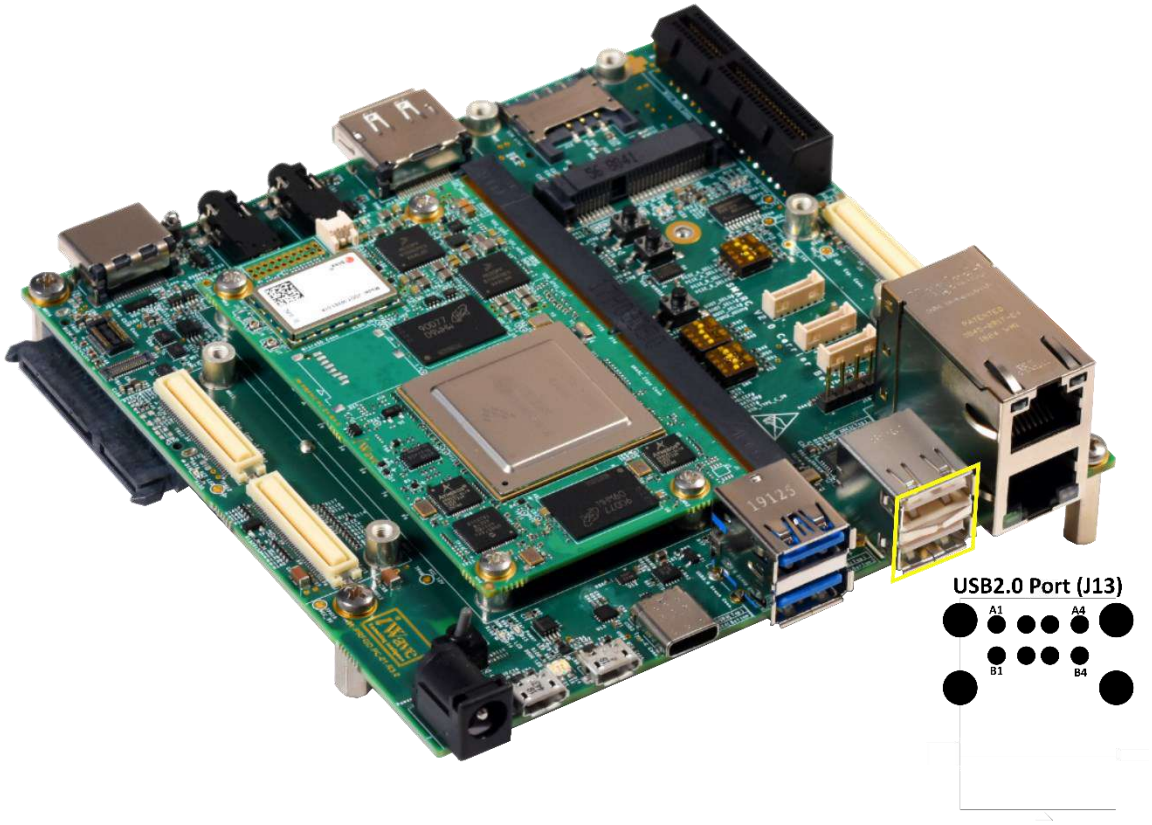


Figure 11: USB2.0 Host

2.6.3 USB2.0 OTG Interface

The SMARC carrier Board supports USB2.0 High Speed OTG interface through i.MX8 CPU's USB0 interface. This USB2.0 Port0 signals of SMARC MXM connector is directly connected to USB2.0 MicroAB connector (J20). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status.

The VBUS power of this USB2.0 connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The connected SMARC SOM detects the USB functionality through USB ID pin and controls the power using the USB0_EN_OC# pin of SMARC MXM connector. In Host mode, USB0_EN_OC# should drive high to enable the power to the connector and in device mode, USB0_EN_OC# should drive low to disable the power to the connector. This USB2.0 OTG connector is physically located at the top of the board as shown below.

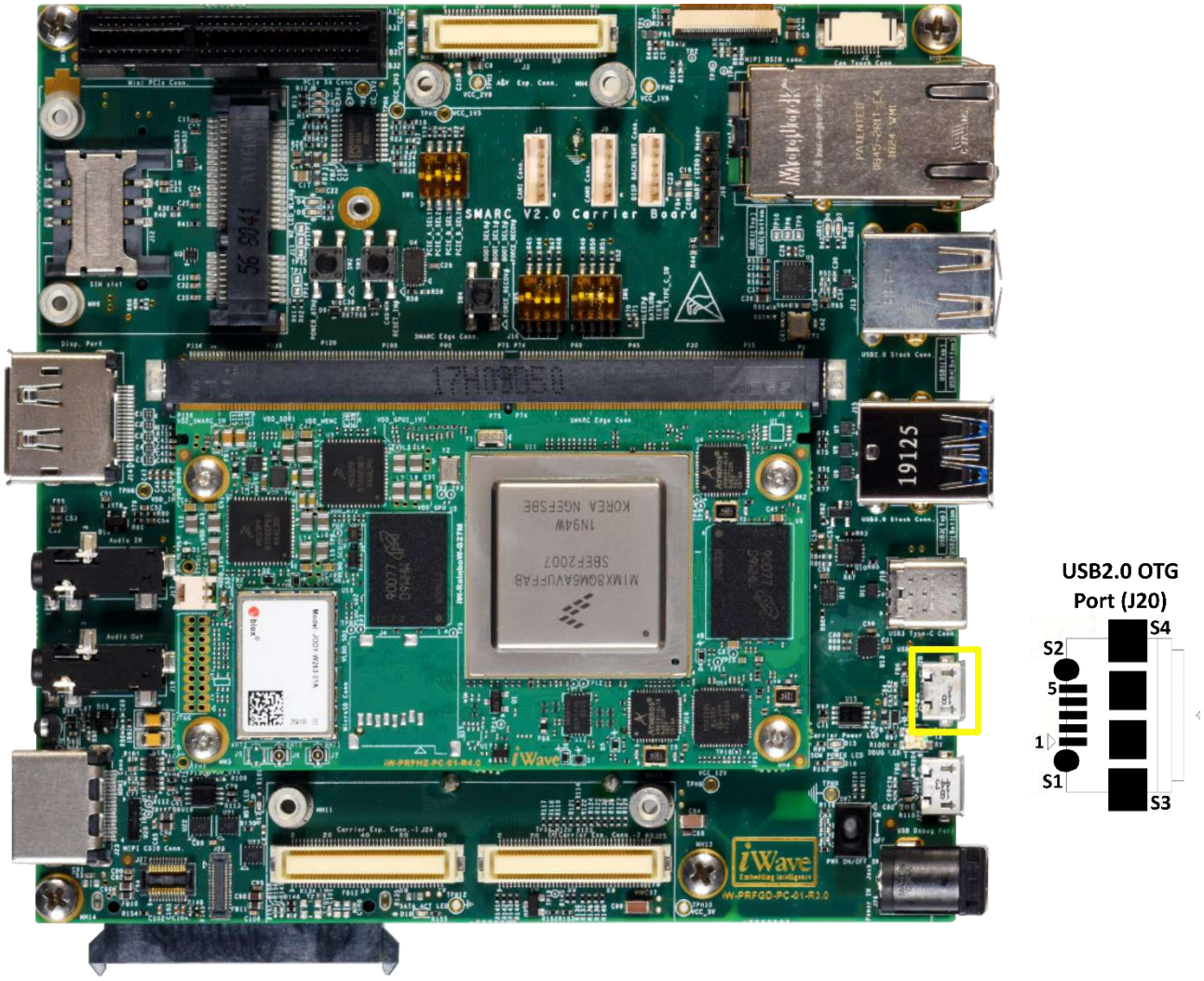


Figure 12: USB2.0 OTG

2.6.4 SDIO Interface

The i.MX8 QM/QP SMARC Carrier Board supports SDIO interface through CPU's uSDHC1 interface. This uSDHC1 signals from SMARC MXM connector is connected to SD connector (J32) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR_EN pin of SMARC MXM connector. The SD connector (J32) is physically located at the bottom of the board.

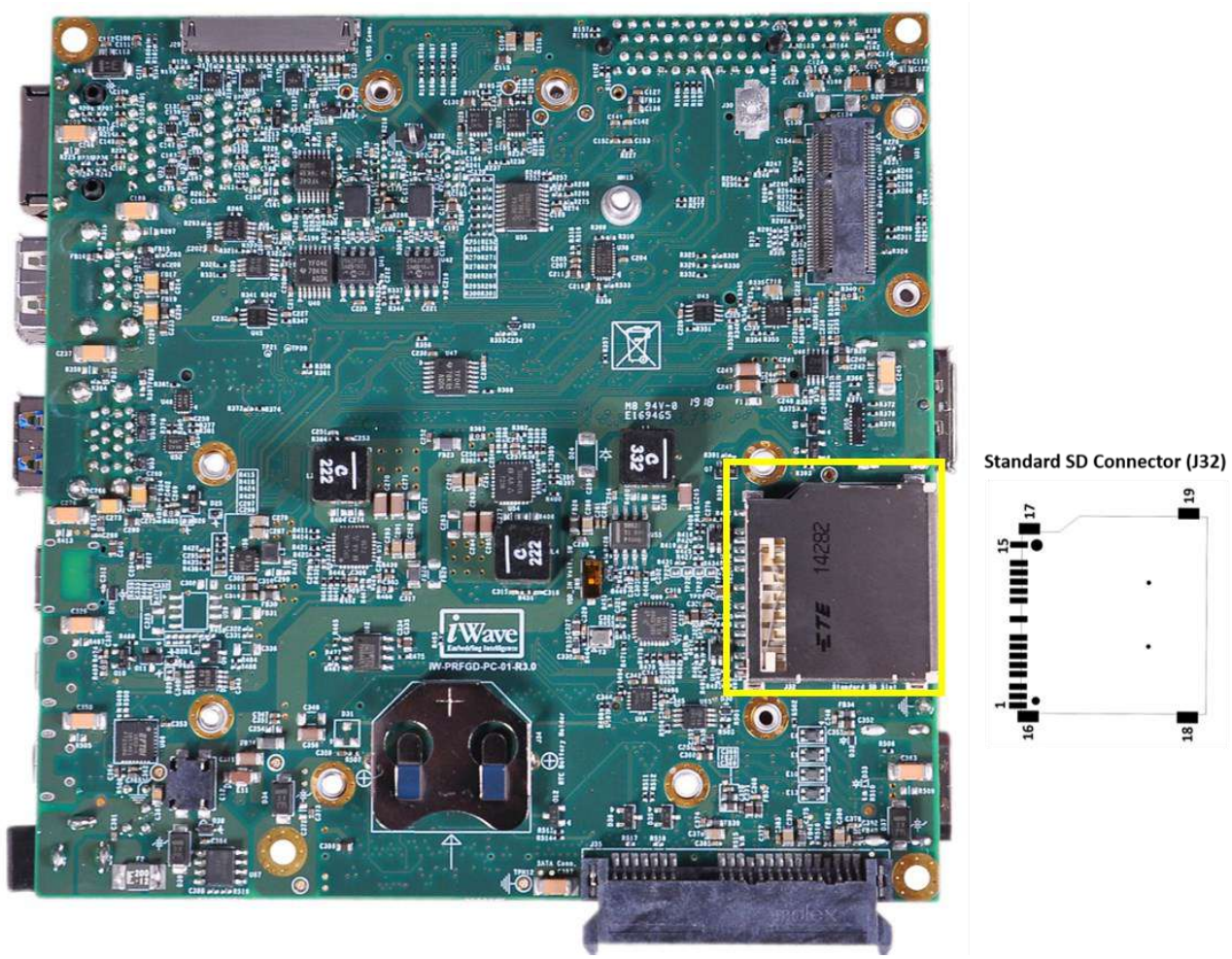


Figure 13:Standard SD Connector

2.6.5 CAN Interface

The SMARC Carrier Board supports two Control Area Network (CAN) Ports. Both CAN0 and CAN1 from the SMARC Edge connector are connected to MCP2562FD-E/SN CAN Transceiver and CANL & CANH of the transceiver are connected to J7 (CAN1) and J8 (CAN0) connectors. Both Connector are placed on Top Side of the Board.

Table 9: CAN0 Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Volatge.*
3	CANL	CAN0_LOW	IO, DIFF	CAN0 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN0_HIGH	IO, DIFF	CAN0 High-Level Voltage I/O
6	GND	GND	Power	Ground.

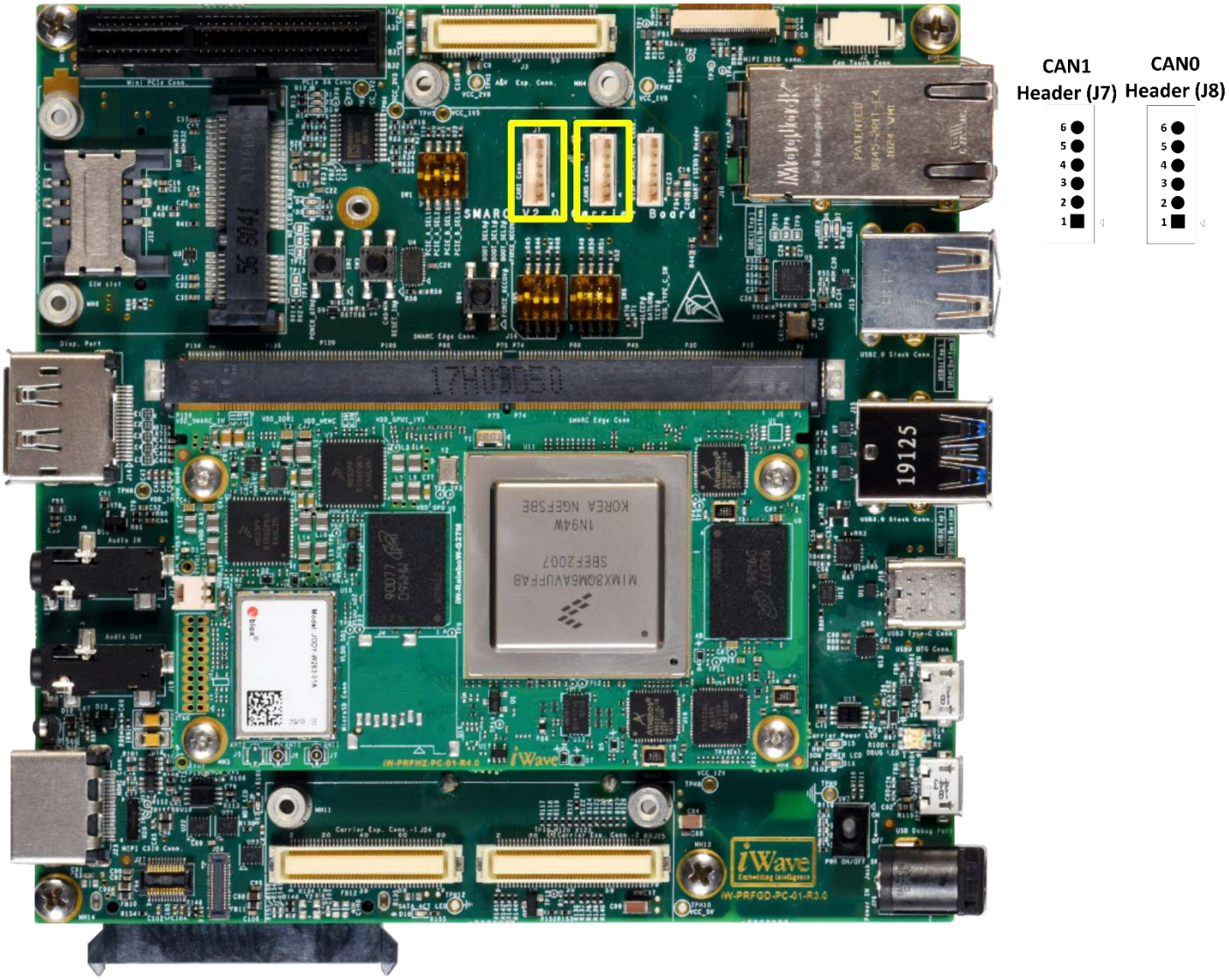


Figure 14: CAN Header

Table 10: CAN1 Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Volatge.*
3	CANL	CAN1_LOW	IO, DIFF	CAN1 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN1_HIGH	IO, DIFF	CAN1 High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.7 Audio/Video Features

2.7.1 HDMI Interface

i.MX8 CPU supports HDMI 2.0 audio/video out. HDMI Signals from the SMARC connector is connected to Standard HDMI Type-A connector with ESD protection circuitry. HDMI Output connector (J23) is physically located on top of the board as shown below.

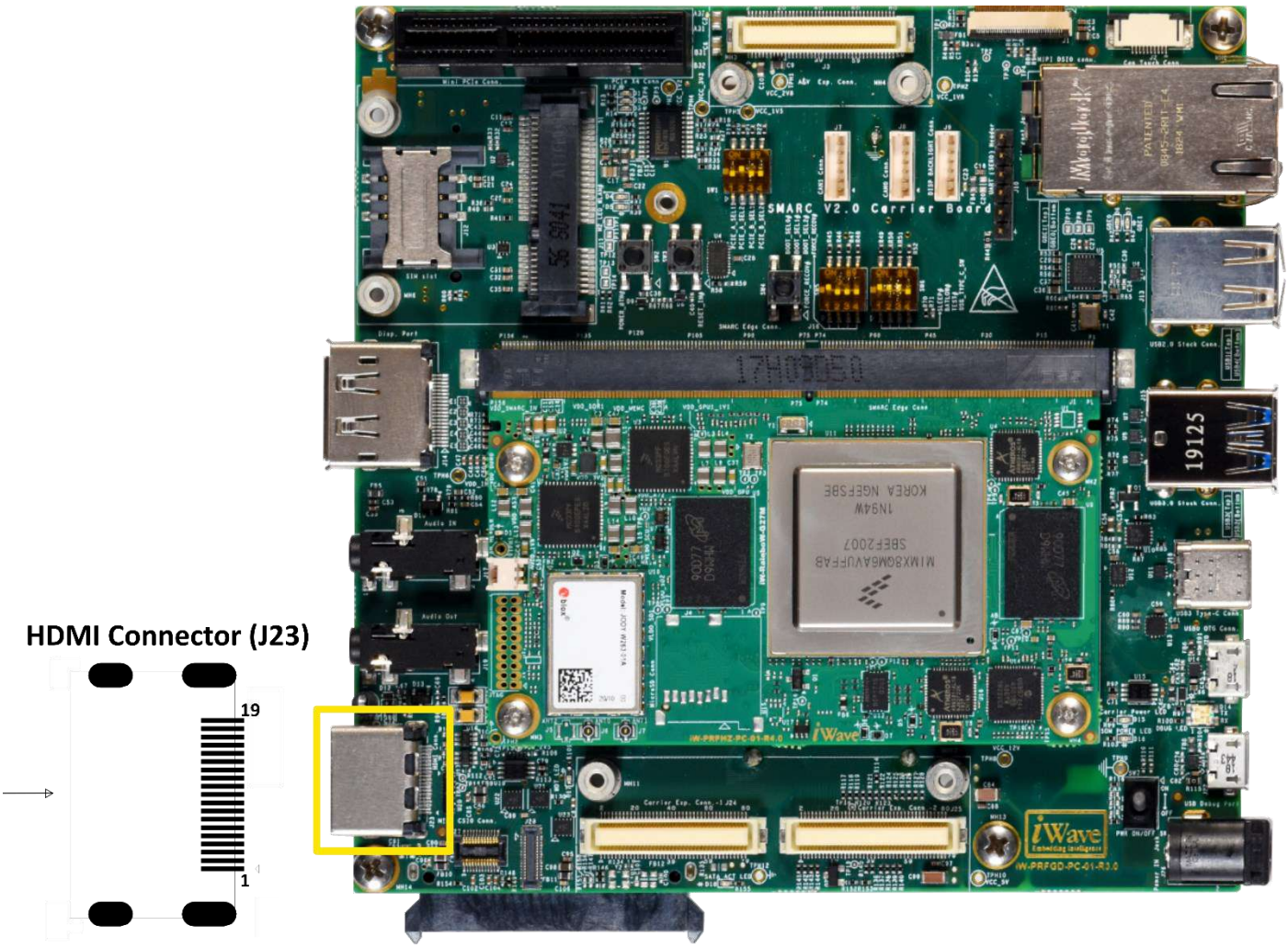


Figure 15: HDMI Output

2.7.2 MIPI DSI Display Interface

The i.MX8 SMARC development board supports 5.49inch, 1080 x 1920 resolution AMOLED Display with Capacitive touch panel MIPI 4 lane display “G1548FH107GG-001” from i-excellence. i.MX8 CPU’s MIPI_DSI0 interface from SMARC MXM connector is used for this LCD interface. This MIPI_DSI0 interface signals are connected to Display connector (J1) via EMI protection circuit and is physically located at the top of board as shown below.

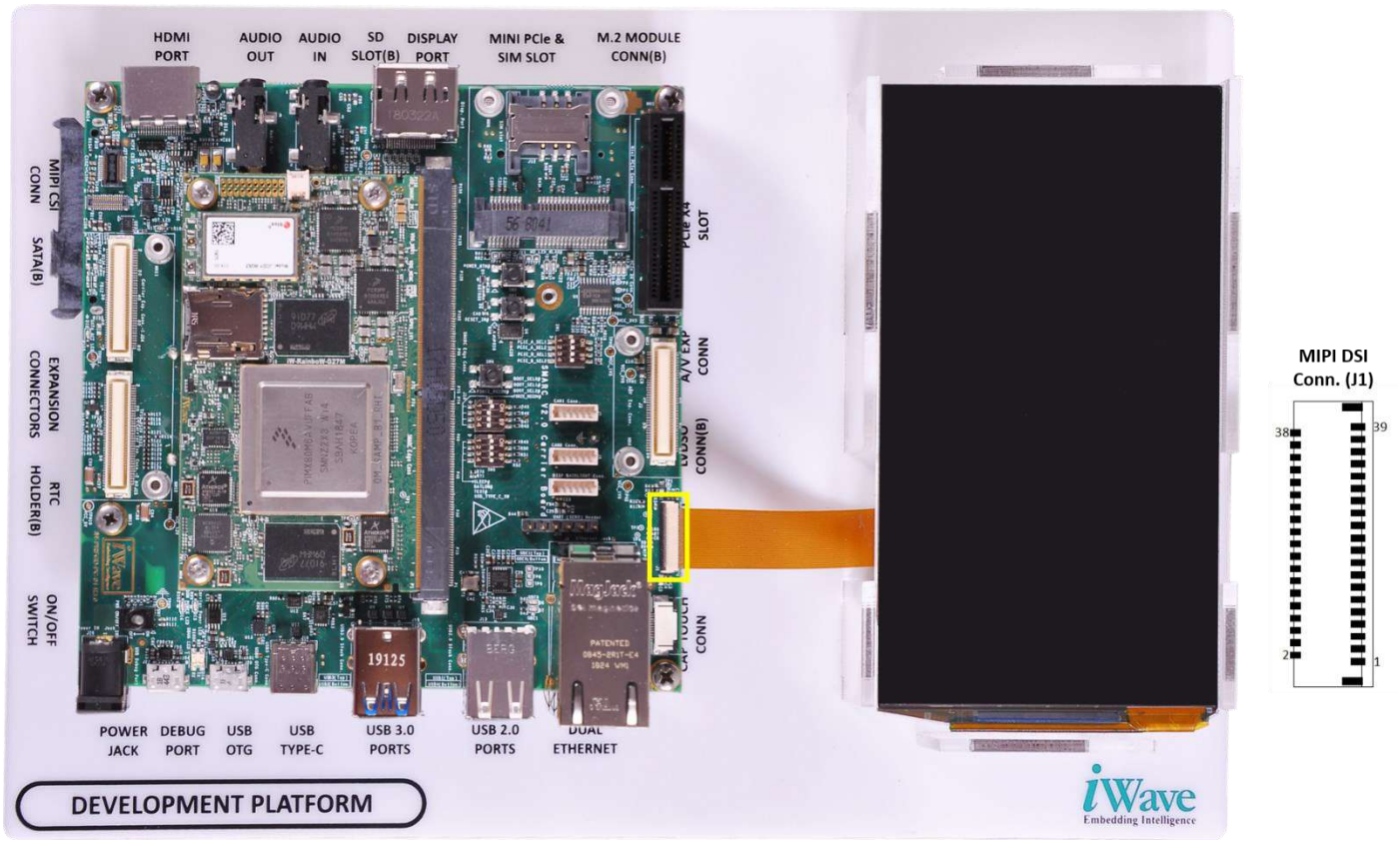


Figure 16: MIPI Display Connector

Table 11: MIPI Display Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.
4	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
5	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
6	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
7	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
8	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
9	GND	GND	Power	Ground.
10	OTPV	NC	NA	NA.
11	NC1	NC	NA	NA.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
12	GND	GND	Power	Ground.
13	D3P	LVDS/DSI0_D3+	O, MIPI	MIPI_DSI DATA Lane3 Positive
14	D3N	LVDS/DSI0_D3-	O, MIPI	MIPI_DSI DATA Lane3 Negative
15	GND	GND	Power	Ground.
16	D0P	LVDS/DSI0_D0+	O, MIPI	MIPI_DSI DATA Lane0 Positive
17	D0N	LVDS/DSI0_D0-	O, MIPI	MIPI_DSI DATA Lane0 Negative
18	GND	GND	Power	Ground.
19	DKP	LVDS/DSI0_CLK+	O, MIPI	MIPI_DSI Clock Positive
20	DKN	LVDS/DSI0_CLK-	O, MIPI	MIPI_DSI Clock Negative
21	GND	GND	Power	Ground.
22	D1P	LVDS/DSI0_D1+	O, MIPI	MIPI_DSI DATA Lane1 Positive
23	D1N	LVDS/DSI0_D1-	O, MIPI	MIPI_DSI DATA Lane1 Negative
24	GND	GND	Power	Ground.
25	D2P	LVDS/DSI0_D2+	O, MIPI	MIPI_DSI DATA Lane2 Positive
26	D2N	LVDS/DSI0_D2-	O, MIPI	MIPI_DSI DATA Lane2 Negative
27	GND	GND	Power	Ground.
28	RESX	DSI_RST1	O, 1,8V CMOS	RESET
29	VDDIO	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Display IO Circuit.
30	VCI	VCI_1	O, 3.3V Power	3.3V Supply voltage for Display Circuit.
31	NC2	NC	NA	NA.
32	GND	GND	Power	Ground.
33	TP_AVDD_3P3V	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for Touch driver Circuit.
34	TP_DVDD_1P8V	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Touch IO Circuit.
35	TP_SDA	I2C_LCD_DAT	IO, 1,8V CMOS	I2C Data for Capacitive Touch
36	TP_SCL	I2C_LCD_CK	O, 1,8V CMOS	I2C Clock for Capacitive Touch
37	TP_RESET	TR1_RST	O, 1,8V CMOS	RESET for Capacitive Touch
38	TP_INT	GPIO_7_TP_INT1	I 1,8V CMOS	Interrupt from Capacitive Touch
39	GND	GND	Power	Ground.

2.7.3 MIPI CSI Camera Interface

The SMARC carrier board supports OV5640 sensor based MIPI CSI camera which supports 5MP of resolution. i.MX8QM CPU's dual lane MIPI CSI0 interface from SMARC MXM connector is used for this Camera interface. This MIPI CSI camera connector (J27) is physically located on top of the board as shown below.

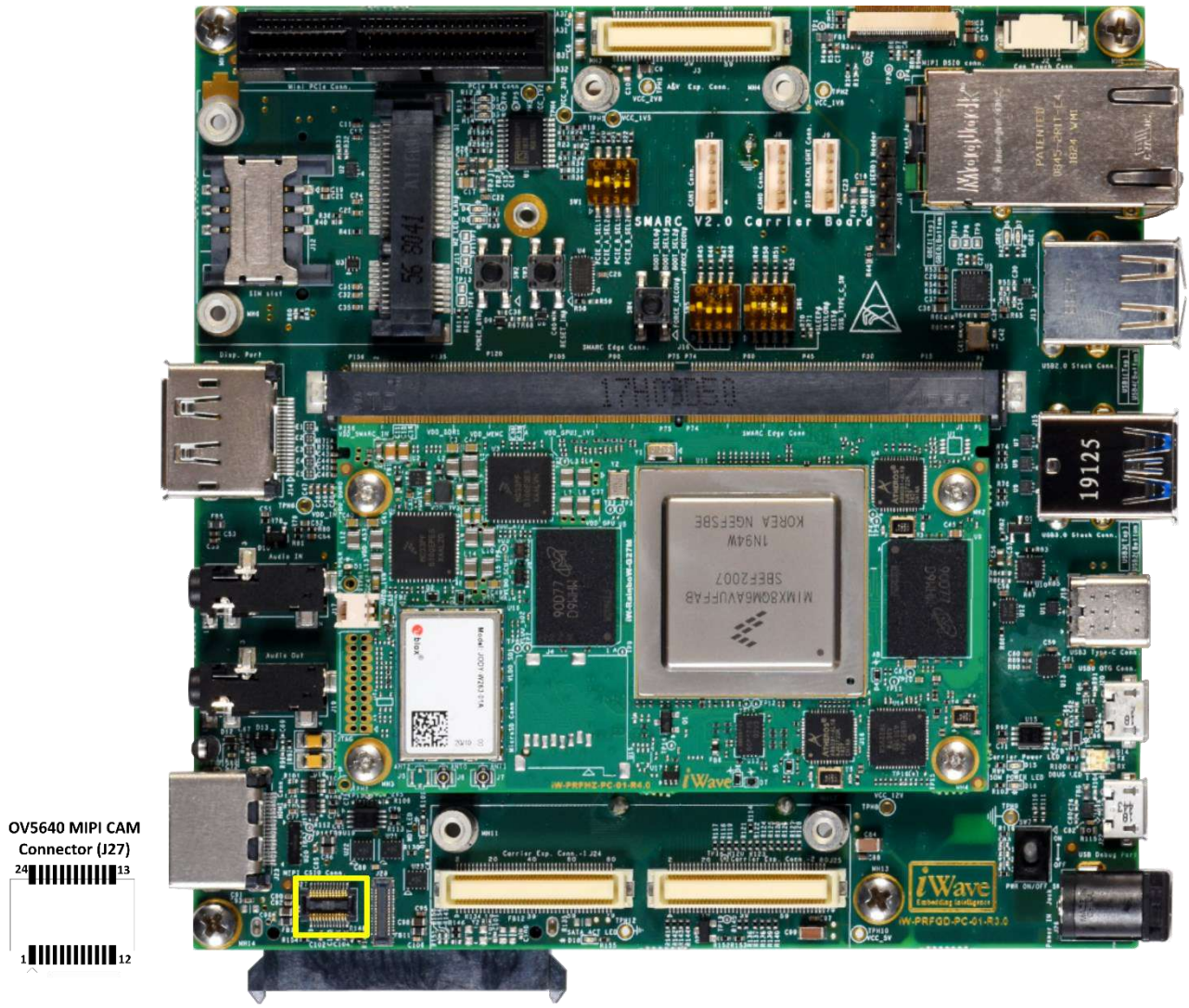


Figure 17: MIPI Camera Connector

Table 12: MIPI Camera Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	Strobe	NC	NA	NA
2	AGND	AGND	Power	Analog Ground.
3	SDA	MIPI_CSI0_I2C0_SDA	IO, 1.8V OD/ 4.7K PU	I2C3 Data for Camera
4	AVDD	AVDD	O, Power	2.8V Supply voltage
5	SCL	MIPI_CSI0_I2C0_SCL	O, 1.8V OD/ 4.7K PU	I2C3 Clock for Camera
6	RESET	SMARC_GPIO_2(GPIO1_28)	O, 1.8V CMOS	GPIO for MIPI CSI Camera reset.
7	NC	NC	NA	NA
8	PWDN	PWDN	O, 1.8V CMOS	Power Down Output
9	NC	NC	NA	NA
10	DVDD	DVDD	O, Power	1.2V Supply voltage

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
11	DOVDD	DOVDD	O, Power	1.8V Supply voltage
12	MDP1	MIPI_CSI0_DATA1_P	I, MIPI	MIPI_CSI0 DATA Lane1 Positive
13	XCLK	XCLK	O, CMOS	Reference Clock to Camera Module
14	MDN1	MIPI_CSI0_DATA1_N	O, MIPI	MIPI_CSI0 DATA Lane1 Negative
15	DGND	GND	Power	Ground.
16	MCP	MIPI_CSI0_CLK_P	I, MIPI	MIPI_CSI0 Clock Positive
17	NC	NC	NA	NA
18	MCN	MIPI_CSI0_CLK_N	I, MIPI	MIPI_CSI0 Clock Negative
19	NC	NC	NA	NA
20	MDP0	MIPI_CSI0_DATA0_P	I, MIPI	MIPI_CSI0 DATA Lane0 Positive
21	NC	NC	NA	NA
22	MDN0	MIPI_CSI0_DATA0_N	I, MIPI	MIPI_CSI0 DATA Lane0 Negative
23	AF-VCC	AF-VCC	O, Power	2.8V Supply voltage
24	AF-AGND	AF-AGND	Power	AF Ground.

2.7.4 I2S Audio Interface

The i.MX8 SMARC carrier board supports Audio IN and OUT through CPU's SAI1 interface which can support I2S format. These four wire I2S signals from SMARC MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input through 3.5mm audio Jack J19 and J17 correspondingly. Also, Headphone detect and Mic detect is supported through GPIO8 (P116th) & GPIO11 (P119th) pin of SMARC MXM connector correspondingly. These Audio Jacks are physically located at the top of the board as shown below.

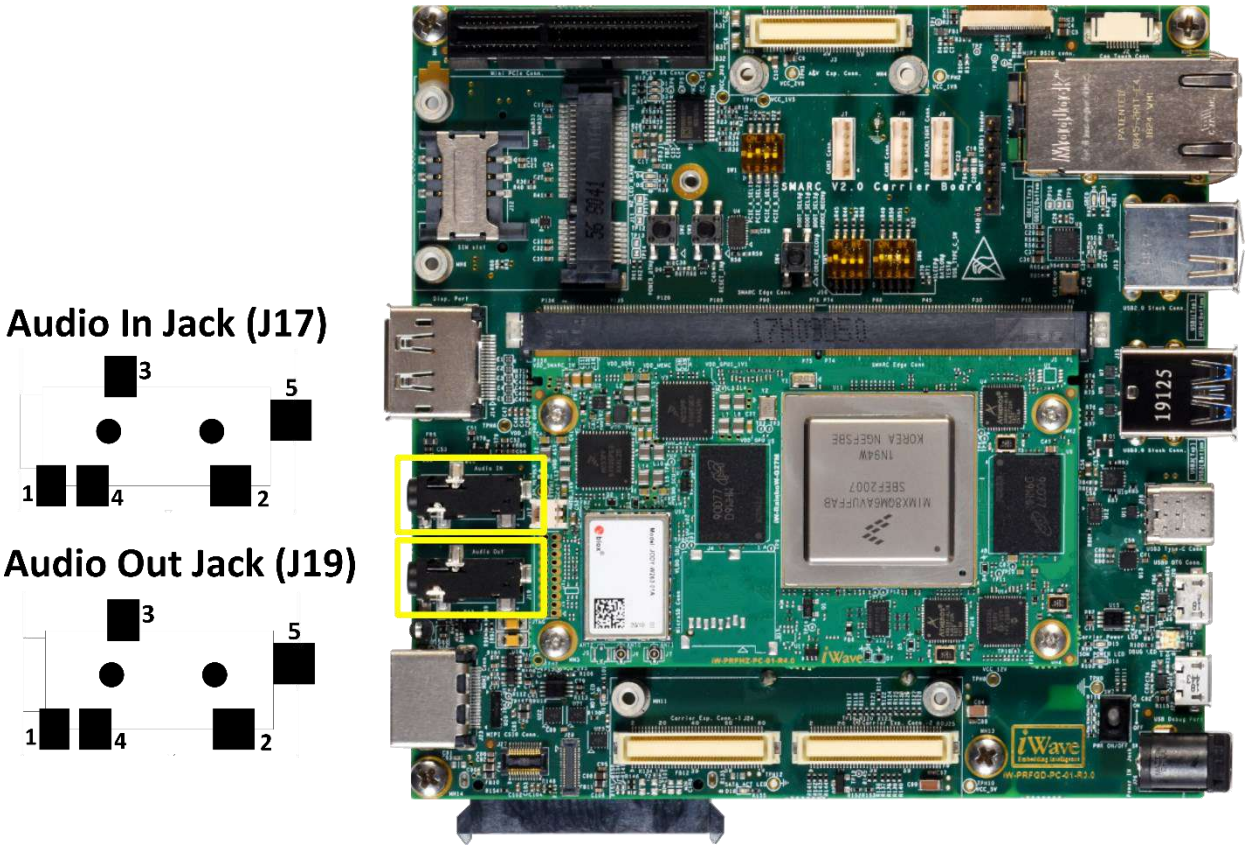


Figure 18: Audio Jack

2.7.5 LVDS Connector (Optional)

The i.MX8 SMARC carrier board supports LVDS Connector (J29) as an optional feature from i.MX8 CPU. The i.MX8 processor supports both LVDS and MIPI DSI Display but SMARC Edge connector supports any one display interface. Contact iWave Support team for LVDS based SOM module. The LVDS Connector (J29) connector is placed on Bottom side of the board.

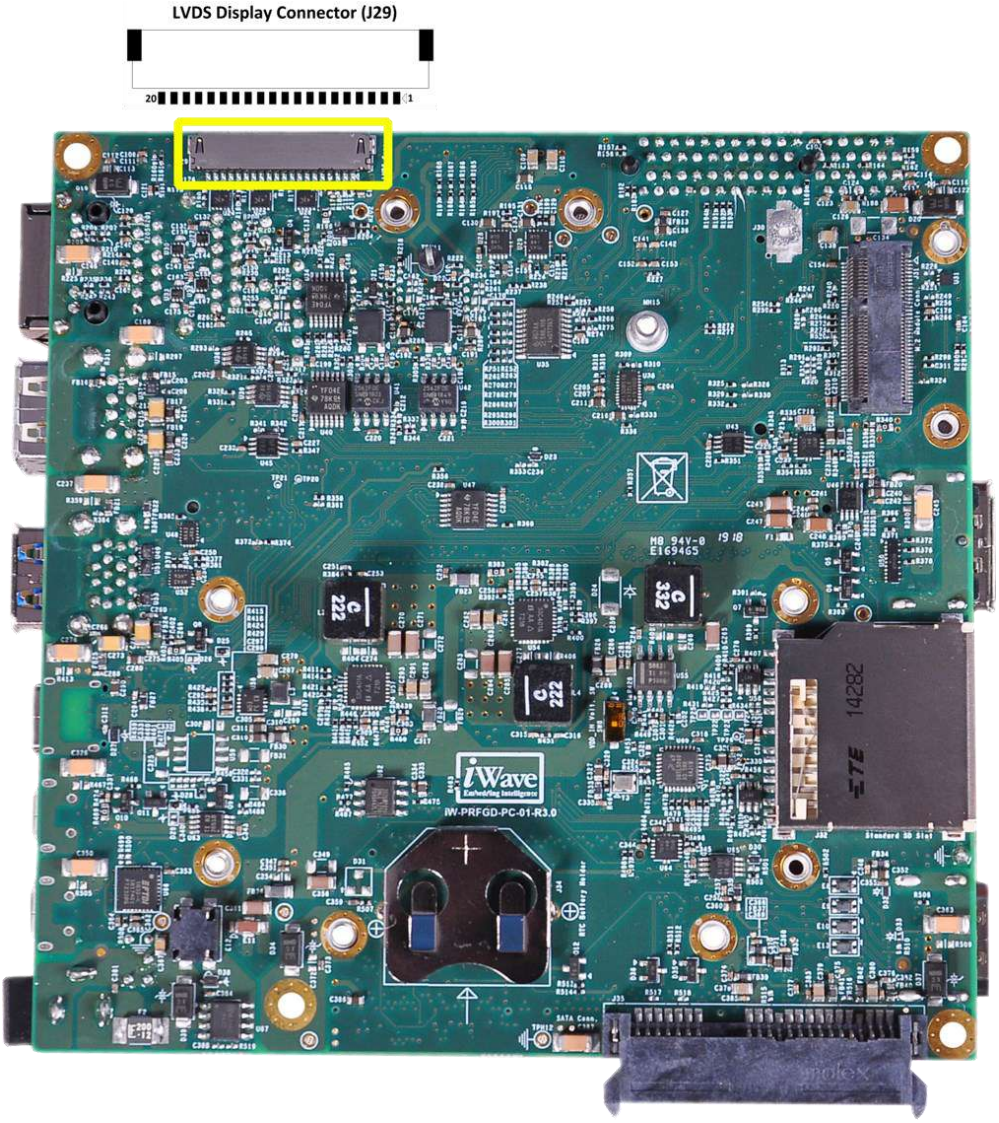


Figure 19: LVDS Display Connector

Table 13: LVDS Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VDD1	VCC_3V3_TFT0	Power	3.3V Supply voltage
2	VDD2	VCC_3V3_TFT0	Power	3.3V Supply voltage
3	GND1	GND	Power	Ground
4	GND2	GND	Power	Ground
5	RIN0-	LVDS _D0-	IO, DIFF	LVDS channel differential pair0 negative

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
6	RIN0+	LVDS_D0+	IO, DIFF	LVDS channel differential pair0 positive
7	GND3	GND	Power	Ground
8	RIN1-	LVDS_D1-	IO, DIFF	LVDS channel differential pair1 negative
9	RIN1+	LVDS_D1+	IO, DIFF	LVDS channel differential pair1 positive
10	GND4	GND	Power	Ground
11	RIN2-	LVDS_D2-	IO, DIFF	LVDS channel differential pair2 negative
12	RIN2+	LVDS_D2+	IO, DIFF	LVDS channel differential pair2 positive
13	GND5	GND	Power	Ground
14	CLKIN-	LVDS_CLK-	IO, DIFF	LVDS channel differential Clock negative
15	CLKIN+	LVDS_CLK+	IO, DIFF	LVDS channel differential Clock positive
16	GND6	GND	Power	Ground
17	RIN3-	LVDS_D3-	IO, DIFF	LVDS channel differential pair3 negative
18	RIN3+	LVDS_D3+	IO, DIFF	LVDS channel differential pair3 positive
19	GND7	GND	Power	Ground
20	GND8	GND	Power	Ground

2.7.6 Display Port (Optional)

The i.MX8 SMARC development board supports Display Port (J14) as an optional feature from i.MX8 CPU. The i.MX8 processor supports either HDMI or Display Port. Contact iWave Support team for Display Port supported SOM. Display Port (J14) connector is placed on Top.

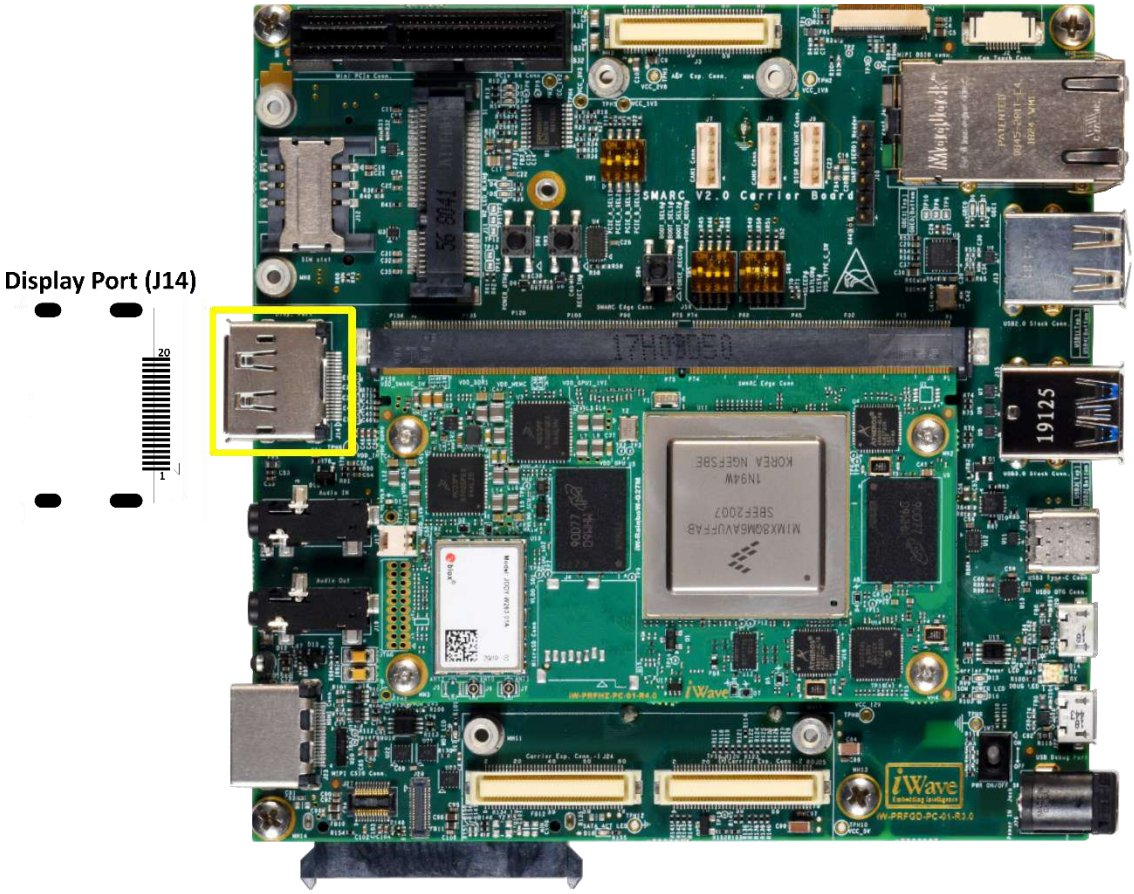


Figure 20: Display Port

2.8 Additional Features

2.8.1 SPI Flash

The i.MX8 SMARC development board supports SPI Flash(U62) through i.MX8 CPU's SPI3 interface. This SPI interface signals from SMARC MXM connector is connected to SPI Flash "IS25WP016D-JNLE" and operating at 1.8V Level.

2.8.2 RTC Coin Cell Holder

The i.MX8 SMARC development board supports Coin Cell Holder to connect "2032" series coin cell. This coin cell voltage is connected to SMARC MXM connector VDD_RTC pin (S147th) for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J34) is physically located on bottom of the board as shown below.

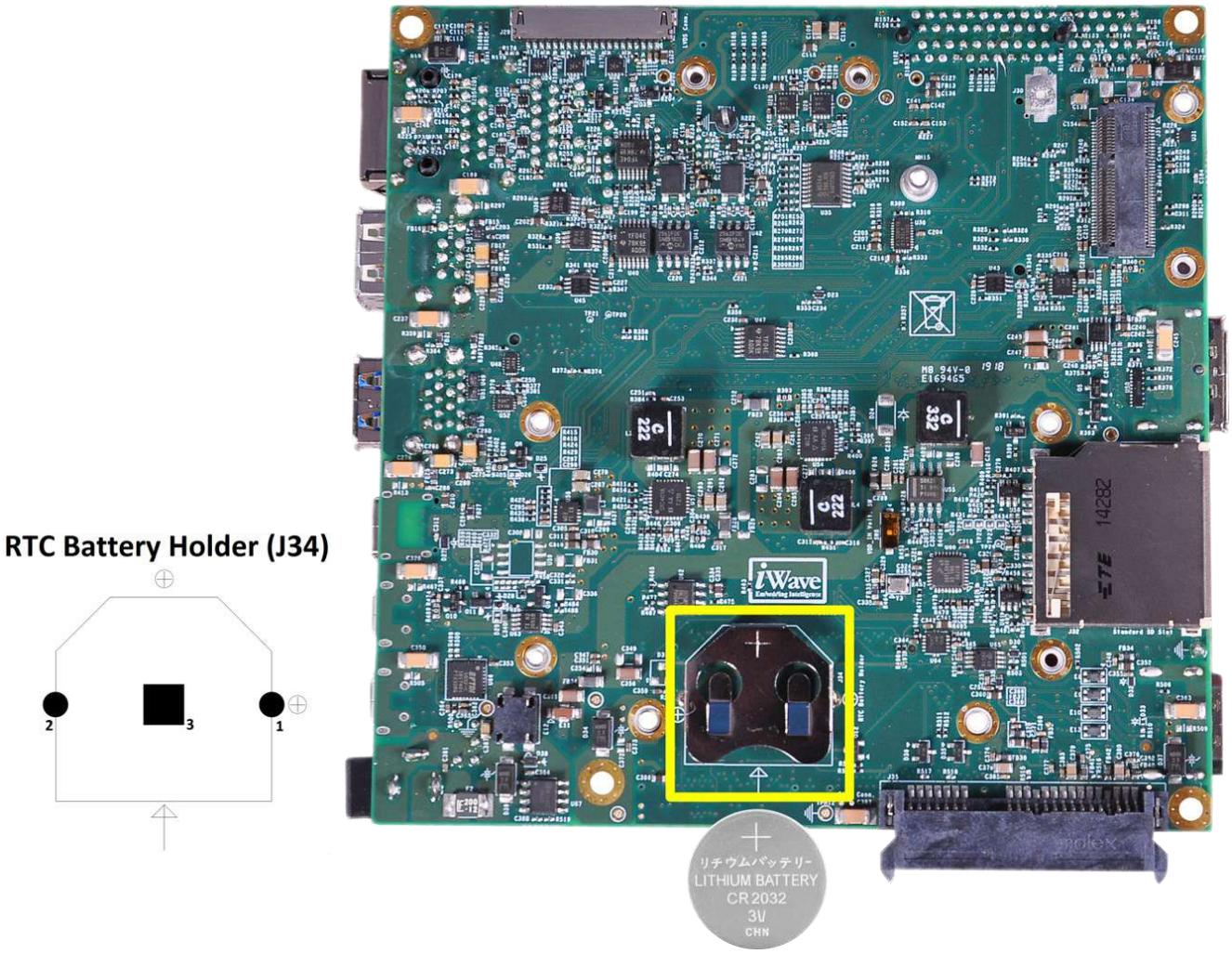


Figure 21: RTC Battery Holder

2.9 On Board Switches

SMARC development board has seven Switches on Top side of carrier card to support generic SMARC features. All the seven switches location is highlight in below image and the switch description is given in the following table.

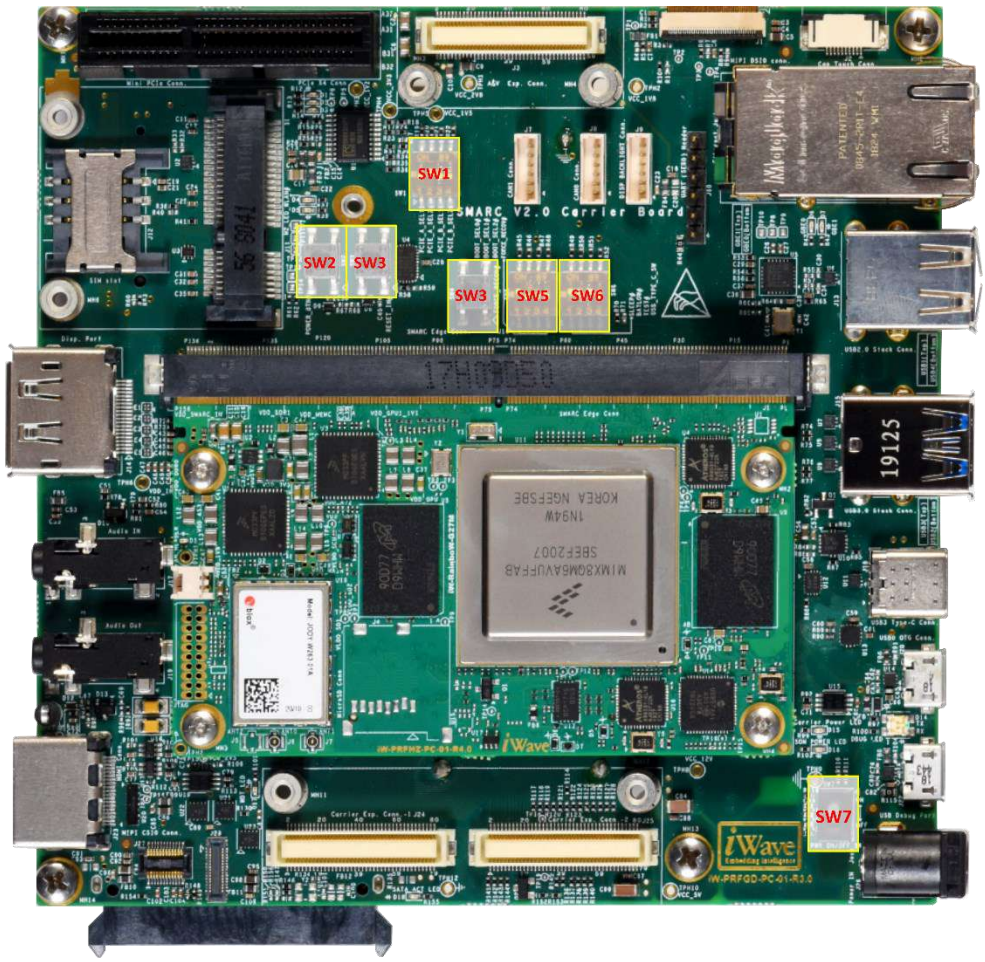


Figure 22: SMARC On Board Switches

Table 14: Board Configuration Switch

<table>
<tr><th rowspan="2">SW Identifier/ (SW Type)</th><th rowspan="2">No. of Bits</th><th rowspan="2">Bit Name</th><th colspan="2">Description</th><th rowspan="2">Remark</th></tr>
<tr><th>ON/Push</th><th>OFF/Release</th></tr>
<tr><td rowspan="2">SW1 (DIP SW)</td><td>1</td><td>PCIe_A_SEL1</td><td colspan="2" rowspan="2"><u>PCIe Channel 0 Connection:</u>
<table><tr><th>State [SEL2,SEL1]</th><th>Select</th><th>Reference image</th></tr><tr><td>00</td><td>Hi-Z</td><td>  </td></tr><tr><td>01</td><td>MINI PCIe</td><td>  </td></tr></table></td><td rowspan="2">1-Switch OFF (Pulled High)
0 -Switch ON (GND)

Note: At a time, do not set Both the PCIe Channel A & B neither to</td></tr>
<tr><td>2</td><td>PCIe_A_SEL2</td></tr>
</table>

<table>
<tr><th>SW Identifier/ (SW Type)</th><th>No. of Bits</th><th>Bit Name</th><th colspan="2">Description</th><th>Remark</th></tr>
<tr><th></th><th></th><th></th><th>ON/Push</th><th>OFF/Release</th><th></th></tr>
<tr><td rowspan="4"></td><td rowspan="3"></td><td rowspan="3"></td><td colspan="2"><table>
<tr><td>10</td><td>M.2</td><td>  </td></tr>
<tr><td>11</td><td>PCIe x4(Lane0)</td><td>  </td></tr>
</table></td><td rowspan="4">mini PCIe nor to M.2 connector.</td></tr>
<tr><td>3</td><td>PCIe_B_SEL1</td><td colspan="2" rowspan="2"><u>PCIe Channel 1 Connection:</u><table>
<tr><th>State [SEL2,SEL1]</th><th>Select</th><th>Reference image</th></tr>
<tr><td>00</td><td>Hi-Z</td><td>  </td></tr>
<tr><td>01</td><td>MINI PCIe</td><td>  </td></tr>
<tr><td>10</td><td>M.2</td><td>  </td></tr>
<tr><td>11</td><td>PCIe x4(Lane1)</td><td>  </td></tr>
</table></td></tr>
<tr><td>4</td><td>PCIe_B_SEL2</td></tr>
<tr><td>SW2 (Push button)</td><td>1</td><td>POWER_BTN#</td><td colspan="2">SOM Power ON - One Press and release
SOM Power OFF - Long Press (above 5sec)</td><td>SOM Power ON/OFF Switch</td></tr>
<tr><td>SW3 (Push button)</td><td>1</td><td>RESET_IN#</td><td colspan="2">SOM Reset – While Pressing
SOM Out of reset – When release</td><td>SOM Reset Switch</td></tr>
<tr><td>SW4 (Push button)</td><td>1</td><td>FORCE_RECOV#</td><td>-</td><td>-</td><td>Not Supported
Note: Same signal is also connected to SW5 4th bit</td></tr>
<tr><td rowspan="4">SW5 (DIP SW)</td><td>1</td><td>BOOT_SEL0#</td><td colspan="2" rowspan="3"><u>BOOT_SEL[2:0]#</u>
000- Boot from SOM FlexSPI (Optional)
001- Boot from SOM eMMC (Default)
011- Boot from SOM microSD (Optional)
110- Boot from Carrier Board SD</td><td rowspan="3">0-Switch OFF (Floating)

1 -Switch ON (GND)</td></tr>
<tr><td>2</td><td>BOOT_SEL1#</td></tr>
<tr><td>3</td><td>BOOT_SEL2#</td></tr>
<tr><td>4</td><td>FORCE_RECOV#</td><td>CPU USB Serial Mode (For</td><td>CPU Normal Boot Mode</td><td>Note: Same signal is also</td></tr>
</table>

SW Identifier/ (SW Type)	No. of Bits	Bit Name	Description		Remark
			ON/Push	OFF/Release	
			programming the SOM boot media)		*connected to SW4*
SW6 (DIP SW)	**1**	LID#/SLEEP#*	-	-	Not Supported
	2	BATLOW#/CHARGING#*	-	-	Not Supported
	3	TEST#/CHARGER_PRSNT#*	-	-	Not Supported
	4	USB_TYPE_C_SW	USB3 port is connected to USB Type A (J15, Top) connector.	USB3 port is connected to USB Type C (J18) connector.	
SW7 (Toggle SW)	**1**	Carrier Power ON/ OFF Switch	Carrier Board Power is ON	Carrier board Power is OFF	Carrier Board Main 12V Power On/Off Switch.

2.10 Audio & Video Expansion Connector

The i.MX8 SMARC Carrier board has 80 pins Audio & Video Expansion Connector (J3). The Audio & Video interface coming from SMARC edge connector and which is not supported on board are taken to this expansion connector. An add-on module can be designed to utilise those features. Audio & Video Expansion connector is physically located at the top of board as shown below.

Connectors Part number : DF17(3.0)-80DS-0.5V(57) from Hirose

Mating Connector : DF17(2.0)-80DP-0.5V(57) from Hirose

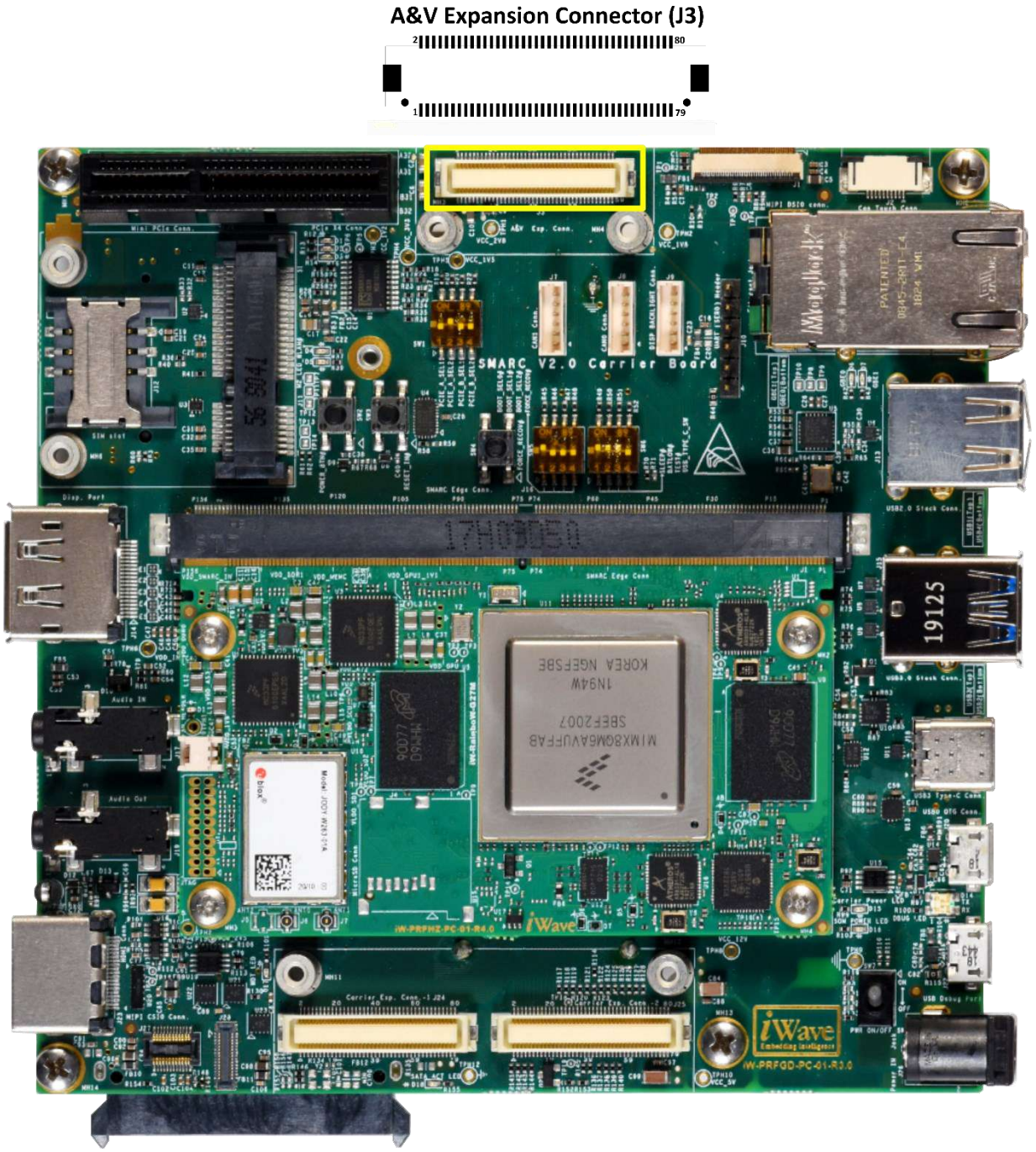


Figure 23: Audio & Video Expansion connector

Table 15: Audio & Video Expansion Connector Pinout

Pin No	Signal Name	Signal Type / Termination	Description
1	VCC_5V	Power	5V Supply voltage
2	VCC_12V	Power	12V Supply voltage
3	VCC_5V	Power	5V Supply voltage
4	VCC_12V	Power	12V Supply voltage
5	GND	Power	Ground.
6	GND	Power	Ground.
7	VCC_2V8	Power	2.8V Supply voltage
8	VCC_3V3	Power	3.3V Supply voltage
9	VCC_2V8	Power	2.8V Supply voltage
10	VCC_3V3	Power	3.3V Supply voltage
11	GND	Power	Ground.
12	VCC_3V3	Power	3.3V Supply voltage
13	VCC_1V5	Power	1.5V Supply voltage
14	GND	Power	Ground.
15	VCC_1V5	Power	1.5V Supply voltage
16	VCC_1V8	Power	1.8V Supply voltage
17	GND	Power	Ground.
18	VCC_1V8	Power	1.8V Supply voltage
19	GND	Power	Ground.
20	VCC_1V8	Power	1.8V Supply voltage
21	GND	Power	Ground.
22	GND	Power	Ground.
23	LVDS0/DSI1_CH1_TX3_N	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 3 negative. *Note: This pin is connected from SMARC Edge connector S121st pin.*
24	VCC_1V2	Power	1.2V Supply voltage
25	LVDS0/DSI1_CH1_TX3_P	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 3 Positive. *Note: This pin is connected from SMARC Edge connector S120th pin.*
26	VCC_1V2	Power	1.2V Supply voltage
27	GND	Power	Ground.
28	GND	Power	Ground.
29	LVDS0/DSI1_CH1_TX2_N	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 2 negative. *Note: This pin is connected from SMARC Edge connector S118th pin.*
30	AUD_SAI0_TXC	O, 1.8V CMOS	I2S /HDA Clock.

Pin No	Signal Name	Signal Type / Termination	Description
			This pin is also connected to M.2 connector (J31) 8th pin for I2S Clock. *Note: This pin is connected from SMARC Edge connector S53rd pin.*
31	LVDS0/DSI1_CH1_TX2_P	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 2 Positive. *Note: This pin is connected from SMARC Edge connector S117th pin.*
32	AUD_SAI0_TXD	O, 1.8V CMOS	I2S /HDA Data out. This pin is also connected to M.2 connector (J31) 12th pin for I2S Data Out. *Note: This pin is connected from SMARC Edge connector S51st pin.*
33	GND	Power	Ground.
34	AUD_SAI0_RXD	I, 1.8V CMOS	I2S /HDA Data IN. This pin is also connected to M.2 connector (J31) 14th pin for I2S Data In. *Note: This pin is connected from SMARC Edge connector S52nd pin*
35	LVDS0/DSI1_CH1_TX1_N	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 1 negative. *Note: This pin is connected from SMARC Edge connector S115th pin*
36	AUD_SAI0_TXFS(SPI2_CS1)	O, 1.8V CMOS	I2S /HAD Left Right Synchronise clock. This pin is also connected to M.2 connector (J31) 10th pin for I2S WS. *Note: This pin is connected from SMARC Edge connector S50th pin.*
37	LVDS0/DSI1_CH1_TX1_P	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 1 Positive. *Note: This pin is connected from SMARC Edge connector S114th pin*
38	GND	Power	Ground.
39	GND	Power	Ground.
40	RSVD6	NA	NC. *Note: This pin is connected from SMARC Edge connector P77th pin*
41	LVDS0/DSI1_CH1_TX0_N	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 0 negative. *Note: This pin is connected from SMARC Edge connector S112rd pin*
42	RSVD7	NA	NA.

Pin No	Signal Name	Signal Type / Termination	Description
			Note: This pin is connected from SMARC Edge connector P78th pin.
43	LVDS0/DSI1_CH1_TX0_P	O, DIFF	LVDS0CH1/MIPI DSI1 differential data lane 0 Positive. *Note: This pin is connected from SMARC Edge connector S111st pin*
44	GND	Power	Ground.
45	GND	Power	Ground.
46	LCD1_VDD_EN	IO, 1.8V CMOS	General Purpose Input / Output
47	LVDS0/DSI1_CH1_CLK_N	O, DIFF	LVDS0CH1/MIPI DSI1 differential Clock negative. *Note: This pin is connected from SMARC Edge connector S109th pin*
48	LCD1_BKLT_EN(GPIO1_15)	O, 1.8V CMOS	General Purpose Input / Output. *Note: This pin is connected from SMARC Edge connector S107th pin.*
49	LVDS0/DSI1_CH1_CLK_P	O, DIFF	LVDS0CH1/MIPI DSI1 differential Clock Positive. *Note: This pin is connected from SMARC Edge connector S108th pin.*
50	LCD1_BL_PWM(GPIO1_10)	IO, 1.8V CMOS	General Purpose Input / Output. *Note: This pin is connected from SMARC Edge connector S122rd pin*
51	GND	Power	Ground.
52	GND	Power	Ground.
53	MIPI_CSI1_DATA3_N	I, DIFF	MIPI CSI1 differential data lane 3 negative. *Note: This pin is connected from SMARC Edge connector P17th pin.*
54	GPIO_RESET_OUT(GPIO0_10)	I, 1.8V CMOS	Reset Out from CPU GPIO. *Note: This pin is connected from SMARC Edge connector P126th pin.*
55	MIPI_CSI1_DATA3_P	I, MIPI	MIPI CSI1 differential data lane 3 Positive. *Note: This pin is connected from SMARC Edge connector P16th pin.*
56	SMARC_GPIO_9(GPIO0_03)	IO, 1.8V CMOS	General Purpose Input / Output. This pin is connected to MIPI Display reset. *Note: This pin is connected from SMARC Edge connector P117th pin.*
57	GND	Power	Ground.
58	GND	Power	Ground.
59	MIPI_CSI1_DATA2_N	I, MIPI	MIPI CSI1 differential data lane 2 negative.

Pin No	Signal Name	Signal Type / Termination	Description
			Note: This pin is connected from SMARC Edge connector P14th pin.
60	RSVD8	-	NC. *Note: This pin is connected from SMARC Edge connector S123rd pin.*
61	MIPI_CSI1_DATA2_P	I, MIPI	MIPI CSI1 differential data lane 2 Positive. *Note: This pin is connected from SMARC Edge connector P13rd pin.*
62	RSVD9	-	NC. *Note: This pin is connected from SMARC Edge connector S142nd pin.*
63	GND	Power	Ground.
64	RSVD5	-	NC. *Note: This pin is connected from SMARC Edge connector P73rd pin.*
65	MIPI_CSI1_DATA1_N	I, MIPI	MIPI CSI1 differential data lane 1 negative. *Note: This pin is connected from SMARC Edge connector P11th pin*
66	RSVD4	-	NC. *Note: This pin is connected from SMARC Edge connector P72rd pin*
67	MIPI_CSI1_DATA1_P	I, MIPI	MIPI CSI1 differential data lane 1 Positive. *Note: This pin is connected from SMARC Edge connector P10th pin.*
68	LVDS_I2C_SDA	IO, 1.8V CMOS	Display and Touch I2C data. This pin is also connected to MIPI DSI connector (J1) 35th pin. *Note: This pin is connected from SMARC Edge connector S140th pin.*
69	GND	Power	Ground.
70	LVDS_I2C_SCL	O, 1.8V CMOS	Display and Touch I2C Clock. This pin is also connected to MIPI DSI connector (J1) 36th pin. *Note: This pin is connected from SMARC Edge connector S139th pin.*
71	MIPI_CSI1_DATA0_N	I, MIPI	MIPI CSI1 differential data lane 0 negative. *Note: This pin is connected from SMARC Edge connector P8th pin.*
72	GND	Power	Ground.
73	MIPI_CSI1_DATA0_P	I, MIPI	MIPI CSI1 differential data lane 0 Positive. *Note: This pin is connected from SMARC Edge connector P7th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
74	MIPI_CSI1_I2C0_SDA	IO, 1.8V CMOS	Camera I2C data. *Note: This pin is connected from SMARC Edge connector S2nd pin.*
75	GND	Power	Ground.
76	MIPI_CSI1_I2C0_SCL	O, 1.8V CMOS	Camera I2C Clock. *Note: This pin is connected from SMARC Edge connector S1st pin.*
77	MIPI_CSI1_CLK_N	I, MIPI	MIPI CSI1 differential Clock negative. *Note: This pin is connected from SMARC Edge connector P4th pin.*
78	SMARC_GPIO_3(GPIO1_31)	IO, 1.8V CMOS	General Purpose Input / Output. *Note: This pin is connected from SMARC Edge connector P111st pin.*
79	MIPI_CSI1_CLK_P	I, MIPI	MIPI CSI1 differential Clock Positive. *Note: This pin is connected from SMARC Edge connector P3rd pin.*
80	GND	Power	Ground.

2.11 Carrier Expansion Connector

The i.MX8 SMARC SOM has 100 pins Expansion connector. All the signals from the SOM expansion connector are directly taken out via two 80 pins carrier expansion J24 and J25 connectors along with few other signals and powers. An add-on module can be designed to utilise those features. Expansion connectors are physically located at the top of board as shown below.

Connectors Part number :DF17(3.0)-80DS-0.5V(57) from Hirose

Mating Connector :DF17(2.0)-80DP-0.5V(57) from Hirose

Note: For SOM expansion connector pinout, refer the i.MX8 SMARC SOM Hardware User Guide.

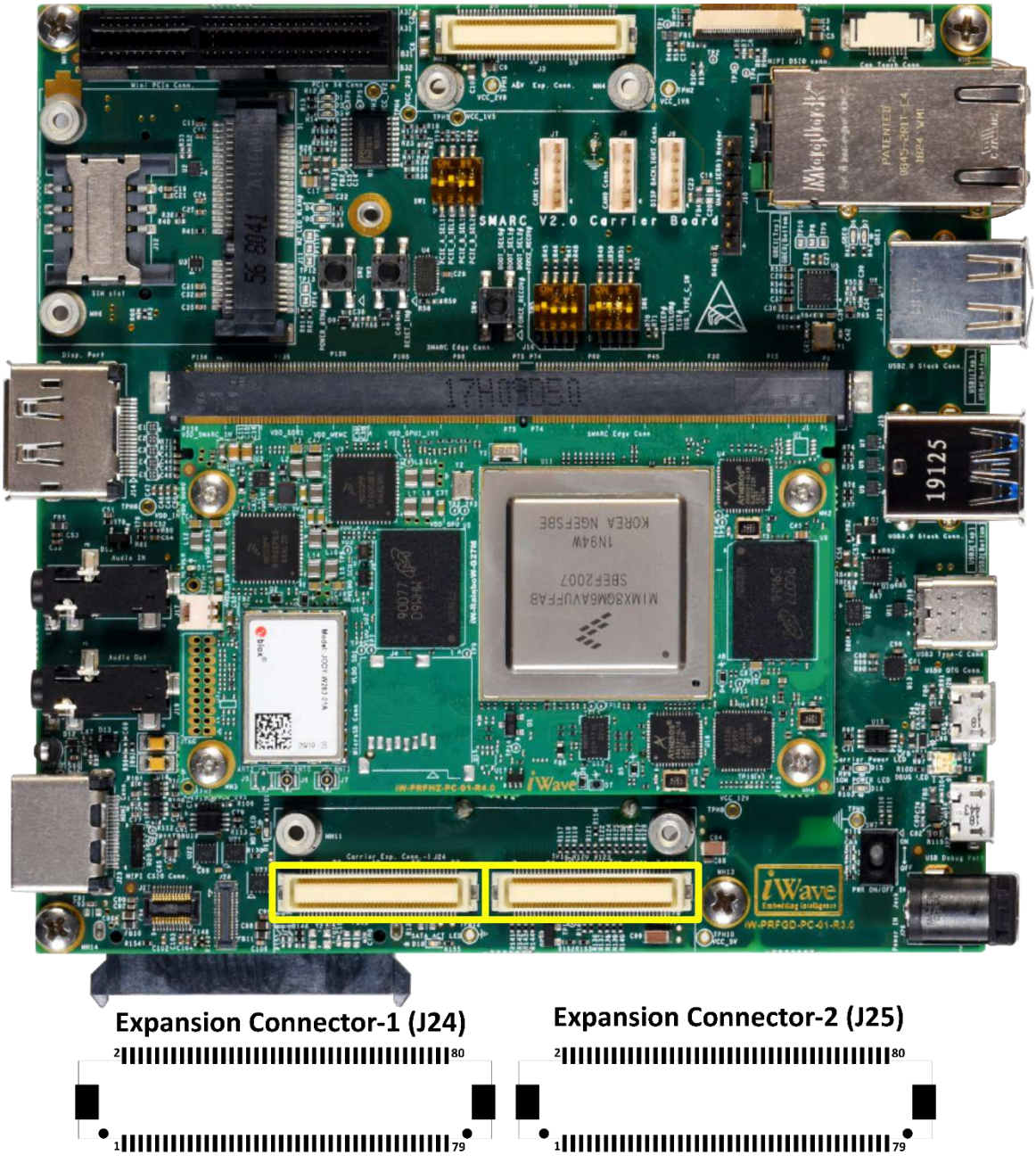


Figure 24: SMARC Expansion Connector

Table 16: Expansion Connector1 Pinout

Pin No	Signal Name	Signal Type / Termination	Description
1	USB3_HUB3_TXP	O, USB SS	USB3.0 Hub Transmit channel 3 positive. *Note: This pin is connected from SOM Expansion connector 2nd pin.*
2	HDMI_RX0_CLK_N	I, TMDS	HDMI RX0 differential Clock negative. *Note: This pin is connected from SOM Expansion connector 1st pin.*
3	USB3_HUB3_TXM	O, DIFF	USB3.0 Hub Transmit channel 3 negative. *Note: This pin is connected from SOM Expansion connector 4th pin.*
4	HDMI_RX0_CLK_P	I, TMDS	HDMI RX0 differential Clock positive. *Note: This pin is connected from SOM Expansion connector 3rd pin.*
5	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 6th pin.*
6	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 5th pin.*
7	USB3_HUB3_RXP	I, USB SS	USB3.0 Hub Receive channel 3 positive. *Note: This pin is connected from SOM Expansion connector 8th pin.*
8	HDMI_RX0_ARC_N	I, TMDS	HDMI RX0 differential Audio Return Channel negative. *Note: This pin is connected from SOM Expansion connector 7th pin.*
9	USB3_HUB3_RXM	I, TMDS	USB3.0 Hub Receive channel 3 negative. *Note: This pin is connected from SOM Expansion connector 10th pin.*
10	HDMI_RX0_ARC_P	I, TMDS	HDMI RX0 differential Audio Return Channel positive. *Note: This pin is connected from SOM Expansion connector 9th pin*
11	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 12th pin.*
12	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 11th pin.*
13	USB3_HUB4_TXP	O, USB SS	USB3.0 Hub Transmit channel 4 positive. *Note: This pin is connected from SOM Expansion connector 14th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
14	HDMI_RX0_DATA0_N	I, TMDS	HDMI RX0 differential data lane 0 negative. *Note: This pin is connected from SOM Expansion connector 13th pin.*
15	USB3_HUB4_TXM	O, USB SS	USB3.0 Hub Transmit channel 4 negative. *Note: This pin is connected from SOM Expansion connector 16th pin.*
16	HDMI_RX0_DATA0_P	I, TMDS	HDMI RX0 differential data lane 0 positive. *Note: This pin is connected from SOM Expansion connector 15th pin.*
17	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 18th pin.*
18	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 17th pin.*
19	USB3_HUB4_RXP	I, USB SS	USB3.0 Hub Receive channel 4 positive. *Note: This pin is connected from SOM Expansion connector 20th pin.*
20	HDMI_RX0_DATA1_N	I, TMDS	HDMI RX0 differential data lane 1 negative. *Note: This pin is connected from SOM Expansion connector 19th pin.*
21	USB3_HUB4_RXM	I, USB SS	USB3.0 Hub Receive channel 4 negative. *Note: This pin is connected from SOM Expansion connector 22nd pin.*
22	HDMI_RX0_DATA1_P	I, TMDS	HDMI RX0 differential data lane 1 positive. *Note: This pin is connected from SOM Expansion connector 21st pin.*
23	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 24th pin.*
24	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 23rd pin.*
25	LVDS1_CH0_CLK_P	O, DIFF	LVDS1 Channel0 Clock positive. *Note: This pin is connected from SOM Expansion connector 26th pin.*
26	HDMI_RX0_DATA2_N	I, DIFF	HDMI RX0 differential data lane 2 negative. *Note: This pin is connected from SOM Expansion connector 25th pin.*
27	LVDS1_CH0_CLK_N	O, DIFF	LVDS1 Channel0 Clock negative. *Note: This pin is connected from SOM Expansion connector 28th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
28	HDMI_RX0_DATA2_P	I, DIFF	HDMI RX0 differential data lane 2 positive. *Note: This pin is connected from SOM Expansion connector 27th pin.*
29	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 30th pin.*
30	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 29th pin.*
31	LVDS1_CH0_TX2_P	O, DIFF	LVDS1 Channel0 Transmit Lane 2 positive. *Note: This pin is connected from SOM Expansion connector 32nd pin.*
32	LVDS1_CH1_TX3_N	O, DIFF	LVDS1 Channel1 Transmit Lane 3 negative. *Note: This pin is connected from SOM Expansion connector 31st pin.*
33	LVDS1_CH0_TX2_N	O, DIFF	LVDS1 Channel0 Transmit Lane 2 negative. *Note: This pin is connected from SOM Expansion connector 34th pin.*
34	LVDS1_CH1_TX3_P	O, DIFF	LVDS1 Channel1 Transmit Lane 3 positive. *Note: This pin is connected from SOM Expansion connector 33rd pin.*
35	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 36th pin.*
36	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 35th pin.*
37	LVDS1_CH0_TX3_P	O, DIFF	LVDS1 Channel0 Transmit Lane 3 positive. *Note: This pin is connected from SOM Expansion connector 38th pin.*
38	LVDS1_CH1_TX2_N	O, DIFF	LVDS1 Channel1 Transmit Lane 2 negative. *Note: This pin is connected from SOM Expansion connector 37th pin.*
39	LVDS1_CH0_TX3_N	O, DIFF	LVDS1 Channel0 Transmit Lane 3 negative. *Note: This pin is connected from SOM Expansion connector 40th pin.*
40	LVDS1_CH1_TX2_P	O, DIFF	LVDS1 Channel1 Transmit Lane 2 positive. *Note: This pin is connected from SOM Expansion connector 39th pin.*
41	GND	Power	NA. *Note: This pin is connected from SOM Expansion connector 42nd pin.*

Pin No	Signal Name	Signal Type / Termination	Description
42	GND	Power	NA. *Note: This pin is connected from SOM Expansion connector 41st pin.*
43	LVDS1_CH0_TX0_P	O, DIFF	LVDS1 Channel0 Transmit Lane 0 positive. *Note: This pin is connected from SOM Expansion connector 44th pin*
44	LVDS1_CH1_TX1_N	O, DIFF	LVDS1 Channel1 Transmit Lane 1 negative. *Note: This pin is connected from SOM Expansion connector 43rd pin.*
45	LVDS1_CH0_TX0_N	O, DIFF	LVDS1 Channel0 Transmit Lane 0 negative. *Note: This pin is connected from SOM Expansion connector 46th pin.*
46	LVDS1_CH1_TX1_P	O, DIFF	LVDS1 Channel1 Transmit Lane 1 positive. *Note: This pin is connected from SOM Expansion connector 45th pin.*
47	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 48th pin.*
48	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 47th pin*
49	LVDS1_CH0_TX1_P	O, DIFF	LVDS1 Channel0 Transmit Lane 1 positive. *Note: This pin is connected from SOM Expansion connector 50th pin.*
50	LVDS1_CH1_TX0_P	O, DIFF	LVDS1 Channel1 Transmit Lane 0 positive. *Note: This pin is connected from SOM Expansion connector 49th pin.*
51	LVDS1_CH0_TX1_N	O, DIFF	LVDS1 Channel0 Transmit Lane 1 negative. *Note: This pin is connected from SOM Expansion connector 52nd pin.*
52	LVDS1_CH1_TX0_N	O, DIFF	LVDS1 Channel1 Transmit Lane 0 negative. *Note: This pin is connected from SOM Expansion connector 51st pin*
53	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 54th pin.*
54	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 53rd pin.*
55	VHDMI_RX_5V	Power	HDMI_RX0 Reference Voltage. *Note: This pin is connected from SOM Expansion connector 56th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
56	LVDS1_CH1_CLK_N	O, DIFF	LVDS1 Channel1 Clock negative. *Note: This pin is connected from SOM Expansion connector 55th pin.*
57	SNVS_TAMPER_IN0	I, 1.8V CMOS, 10K PD	TAMPER INPUT 1. *Note: This pin is connected from SOM Expansion connector 58th pin.*
58	LVDS1_CH1_CLK_P	O, DIFF	LVDS1 Channel1 Clock positive. *Note: This pin is connected from SOM Expansion connector 57th pin.*
59	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 60th pin.*
60	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 59th pin.*
61	MLB_DATA_P	IO, DIFF	Media Local Bus DATA positive. *Note: This pin is connected from SOM Expansion connector 62nd pin.*
62	SNVS_TAMPER_IN1	I, 1.8V CMOS, 10K PD	TAMPER INPUT 2. *Note: This pin is connected from SOM Expansion connector 61st pin*
63	MLB_DATA_N	IO, DIFF	Media Local Bus DATA negative. *Note: This pin is connected from SOM Expansion connector 64th pin*
64	SNVS_TAMPER_OUT1	O, 1.8V CMOS	TAMPER OUTPUT 2. *Note: This pin is connected from SOM Expansion connector 63rd pin.*
65	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 66th pin.*
66	ESAI1_FST	O, 1.8V CMOS	ESAI1 Frame Sync Output. *Note: This pin is connected from SOM Expansion connector 65th pin.*
67	MLB_CLK_P	O, DIFF	Media Local Bus Clock positive. *Note: This pin is connected from SOM Expansion connector 68th pin.*
68	HDMI_RX0_CEC	IO, 3.3V CMOS	HDMI Consumer Electronics Control. *Note: This pin is connected from SOM Expansion connector 67th pin.*
69	MLB_CLK_N	O, DIFF	Media Local Bus Clock negative. *Note: This pin is connected from SOM Expansion connector 70th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
70	HDMI_RX_HPD	O, 5V CMOS	HDMI RX0 Hot Plug Detect. *Note: This pin is connected from SOM Expansion connector 69th pin.*
71	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 72nd pin.*
72	HDMI_RX0_DDC_SDA	IO, 5V CMOS	HDMI RX0 I2C Data. *Note: This pin is connected from SOM Expansion connector 71st pin.*
73	MLB_SIG_P	O, DIFF	Media Local Bus Signal positive. *Note: This pin is connected from SOM Expansion connector 74th pin.*
74	SNVS_TAMPER_OUT0	O, 1.8V CMOS, 10K PD	TAMPER OUTPUT 1. *Note: This pin is connected from SOM Expansion connector 73rd pin.*
75	MLB_SIG_N	O, DIFF	Media Local Bus Signal negative. *Note: This pin is connected from SOM Expansion connector 76th pin.*
76	ESAI1_SCKR	I, 1.8V CMOS	ESAI1 Clock Input *Note: This pin is connected from SOM Expansion connector 75th pin*
77	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 78th pin*
78	ESAI1_FSR	I, 1.8V CMOS	ESAI1 Frame Sync Input. *Note: This pin is connected from SOM Expansion connector 77th pin.*
79	GND	Power	Ground.
80	GND	Power	Ground.

Table 17: Expansion Connector2 Pinout

Pin No	Signal Name	Signal Type / Termination	Description
1	MIPI_CSI0_DATA2_P	I, MIPI	MIPI CSI0 differential data lane 2 positive. *Note: This pin is connected from SOM Expansion connector 80th pin.*
2	HDMI_RX0_DDC_SCL	I, 5V CMOS	HDMI RX0 I2C Clock. *Note: This pin is connected from SOM Expansion connector 79th pin*
3	MIPI_CSI0_DATA2_N	I, MIPI	MIPI CSI0 differential data lane 2 negative. *Note: This pin is connected from SOM Expansion connector 82nd pin*
4	ESAI1_TX0	O, 1.8V CMOS	ESAI1 Transmit 0 *Note: This pin is connected from SOM Expansion connector 81st pin.*
5	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 84th pin.*
6	SPDIF_ETX_CLK	O, 1.8V CMOS	Sony/Philips Digital Interface Clock. *Note: This pin is connected from SOM Expansion connector 83rd pin.*
7	MIPI_CSI0_DATA3_P	I, MIPI	MIPI CS0 differential data lane 3 positive. *Note: This pin is connected from SOM Expansion connector 86th pin.*
8	SPDIF_TX	O, 1.8V CMOS	Sony/Philips Digital Interface Transmit *Note: This pin is connected from SOM Expansion connector 85thpin.*
9	MIPI_CSI0_DATA3_N	I, MIPI	MIPI CSI0 differential data lane 3 negative. *Note: This pin is connected from SOM Expansion connector 88th pin.*
10	ESAI1_TX1	IO, 1.8V CMOS	ESAI1 Transmit 1. *Note: This pin is connected from SOM Expansion connector 87th pin.*
11	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 90th pin.*
12	ESAI1_TX4_RX1	IO, 1.8V CMOS	ESAI1 Transmit 4 or Receive 1. *Note: This pin is connected from SOM Expansion connector 89th pin*
13	ESAI1_SCKT	O, 1.8V CMOS	ESAI1 Clock Out. *Note: This pin is connected from SOM Expansion connector 92nd pin*
14	FLEXCAN2_RX	I, 1.8V CMOS	CAN2 Receiver.

Pin No	Signal Name	Signal Type / Termination	Description
			Note: This pin is connected from SOM Expansion connector 91st pin.
15	SPDIF_RX	I, 1.8V CMOS	Sony/Philips Digital Interface Receive. *Note: This pin is connected from SOM Expansion connector 94th pin.*
16	MLB_DATA	IO, 1.8V CMOS	Media Local Bus Data. *Note: This pin is connected from SOM Expansion connector 93rd pin.*
17	ESAI1_TX3_RX2	IO, 1.8V CMOS	ESAI1 Transmit 3 or Receive 2. *Note: This pin is connected from SOM Expansion connector 96th pin.*
18	MLB_CLK	O, 1.8V CMOS	Media Local Bus Clock. *Note: This pin is connected from SOM Expansion connector 95th pin*
19	ESAI1_TX2_RX3	IO, 1.8V CMOS	ESAI1 Transmit 2 or Receive 3. *Note: This pin is connected from SOM Expansion connector 98th pin.*
20	MLB_SIG	O, 1.8V CMOS	Media Local Bus Signal. *Note: This pin is connected from SOM Expansion connector 97th pin*
21	ESAI1_TX5_RX0	IO, 1.8V CMOS	ESAI1 Transmit 5 or Receive 0. *Note: This pin is connected from SOM Expansion connector 100th pin.*
22	FLEXCAN2_TX	O, 1.8V CMOS	CAN2 Transmitter. *Note: This pin is connected from SOM Expansion connector 99th pin.*
23	NC	NA	NC. *Note: This pin is connected from SMARC Edge connector S156th pin.*
24	SCU_WDOG_OUT	I, 1.8V CMOS	NC. *Note: This pin is connected from SMARC Edge connector S145th pin.*
25	GND	Power	Ground.
26	UART3_RX	I, 1.8V CMOS	UART3 Receiver. *Note: This pin is connected from SMARC Edge connector P135th pin*
27	GPIO3_25	IO, 1.8V CMOS	GPIO3_25 is connected. *Note: This pin is connected from SMARC Edge connector S144th pin.*
28	UART3_TX	O, 1.8V CMOS	UART3 Transmitter. *Note: This pin is connected from SMARC Edge connector P134th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
29	SM_PMIC_I2C_SDA	NA	NC. *Note: Optionally Connected to PMIC_I2C_SDA* *This pin is connected from SMARC Edge connector P122th pin.*
30	GND	Power	Ground.
31	SMARC_GPIO_6(GPIO0_00)	IO, 1.8V CMOS	General Purpose Input / Output. This pin is also Connected to USB Type C Controller Interrupt pin. *Note: This pin is connected from SMARC Edge connector P114th pin.*
32	SM_PMIC_I2C_SCL	NA	NC. *Note: Optionally Connected to PMIC_I2C_SCL.* *This pin is connected from SMARC Edge connector P121st pin.*
33	PCIE_B_RST_B(GPIO5_00)	IO, 3.3V CMOS	General Purpose Input / Output. This pin is also connected to PCIe 1 RESET OUT. *Note: This pin is connected from SMARC Edge connector S76th pin.*
34	SPI3_MISO	I, 1.8V CMOS	SPI3 Chip Master IN Slave Out. This pin is also connected to on board SPI Flash. *Note: This pin is connected from SMARC Edge connector P45th pin.*
35	GND	Power	Ground.
36	SPI3_MOSI	O, 1.8V CMOS	SPI3 Chip Master Out Slave IN. This pin is also connected to on board SPI Flash. *Note: This pin is connected from SMARC Edge connector P46th pin.*
37	MIPI_CSI0_CLK_P	I, MIPI	MIPI CSI0 differential Clock Positive The signal is also connected to on Board Camera connector to avoid the stub unmount R145 Resistor in the Carrier Card. *Note: This pin is connected from SMARC Edge connector S8th pin*
38	SPI3_SCLK	O, 1.8V CMOS	SPI3 Clock. This pin is also connected to on board SPI Flash. *Note: This pin is connected from SMARC Edge connector P44th pin.*
39	MIPI_CSI0_CLK_N	I, MIPI	MIPI CSI0 differential Clock Negative

Pin No	Signal Name	Signal Type / Termination	Description
			The signal is also connected to on Board Camera connector to avoid the stub unmount R136 Resistor in the Carrier Card. *Note: This pin is connected from SMARC Edge connector S9th pin.*
40	GND	Power	Ground.
41	NC	NA	NC. *Note: This pin is connected from SMARC Edge connector S77th pin.*
42	MIPI_CSI0_I2C0_SDA	IO, 1.8V CMOS	Camera I2C data. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S7th pin.*
43	GND	Power	Ground.
44	MIPI_CSI0_MCLK_OUT	O, 1.8V CMOS	MIPI CSI0 Master Clock. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S6th pin.*
45	MIPI_CSI0_DATA0_P	I, MIPI	MIPI CSI0 differential data lane 0 Positive The signal is also connected to on Board Camera connector to avoid the stub unmount R137 Resistor in the Carrier Card. *Note: This pin is connected from SMARC Edge connector S11th pin*
46	I2C_CAM0_CK	O, 1.8V CMOS	Camera I2C CLK. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S5th pin.*
47	MIPI_CSI0_DATA0_N	I, MIPI	MIPI CSI0 differential data lane 0 Negative. The signal is also connected to on Board Camera connector to avoid the stub unmount R135 Resistor in the Carrier Card. *Note: This pin is connected from SMARC Edge connector S12th pin.*
48	GND	Power	Ground.
49	GND	Power	Ground.
50	DMA_I2C1_SCL	O, 1.8V CMOS	General Purpose I2C CLK for carrier board peripherals.

Pin No	Signal Name	Signal Type / Termination	Description
			Note: This pin is connected from SMARC Edge connector S48th pin.
51	MIPI_CSI0_DATA1_P	I, MIPI	MIPI CSI0 differential data lane 1 Positive The signal is also connected to on Board Camera connector to avoid the stub unmount R139 Resistor in the Carrier Card. *Note: This pin is connected from SMARC Edge connector S14th pin.*
52	DMA_I2C1_SDA	IO, 1.8V CMOS	General Purpose I2C Data for carrier board peripherals. *Note: This pin is connected from SMARC Edge connector S49th pin.*
53	MIPI_CSI0_DATA1_N	I, MIPI	MIPI CSI0 differential data lane 1 Negative The signal is also connected to on Board Camera connector to avoid the stub unmount R140 Resistor in the Carrier Card. *Note: This pin is connected from SMARC Edge connector S15th pin.*
54	GND	Power	Ground.
55	QSPI1A_RESET(GPIO4_22)	O, 1.8V CMOS	QSPI1A_RESET(GPIO4_22). *Note: This pin is connected from SMARC Edge connector S58th pin.*
56	QSPI1A_SS0	O, 1.8V CMOS	QSPI1A Chip Select 0. *Note: This pin is connected from SMARC Edge connector P54th pin.*
57	QSPI1A_DATA2	IO, 1.8V CMOS	QSPI1A_DATA2. *Note: This pin is connected from SMARC Edge connector S57th pin.*
58	QSPI1A_SS1	O, 1.8V CMOS	QSPI1A Chip Select 1. *Note: This pin is connected from SMARC Edge connector P55th pin*
59	QSPI1A DATA 3	IO, 1.8V CMOS	QSPI1A DATA 3. *Note: This pin is connected from SMARC Edge connector S56th pin.*
60	QSPI1A_SCLK	O, 1.8V CMOS	QSPI1A Clock. *Note: This pin is connected from SMARC Edge connector P56th pin.*
61	NC	NA	NC. *Note: This pin is connected from SMARC Edge connector S55th pin.*
62	QSPI1A_DATA0	IO, 1.8V CMOS	QSPI1A DATA 0.

Pin No	Signal Name	Signal Type / Termination	Description
			Note: This pin is connected from SMARC Edge connector P58th pin.
63	RSVD1	-	NC. *Note: This pin is connected from SMARC Edge connector S4th pin.*
64	QSPI1A_DATA1	IO, 1.8V CMOS	QSPI1A DATA 1. *Note: This pin is connected from SMARC Edge connector P57th pin.*
65	SMBUS_ALERT(GPIO0_16)	IO, 1.8V CMOS	General Purpose Input / Output GPIO0_16. *Note: This pin is connected from SMARC Edge connector P1st pin.*
66	RSVD3	-	NC. *Note: This pin is connected from SMARC Edge connector S46th pin.*
67	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S43rd pin.*
68	RSVD2	-	NC. *Note: This pin is connected from SMARC Edge connector S45th pin.*
69	SPI3_CS0	O, 1.8V CMOS	SPI0 Chip Select0. This pin is also connected to on board SPI Flash. *Note: This pin is connected from SMARC Edge connector P43rd pin*
70	SPI3_CS1	O, 1.8V CMOS	SPI0 Chip Select1. *Note: This pin is connected from SMARC Edge connector P31st pin.*
71	VCC_1V8	Power	Supply Voltage 1.8V.
72	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S44th pin.*
73	GND	Power	Ground.
74	GND	Power	Ground.
75	VCC_5V	Power	Supply Voltage 5V
76	VCC_3V3	Power	Supply Voltage3.3V
77	VCC_5V	Power	Supply Voltage 5V
78	VCC_3V3	Power	Supply Voltage3.3V
79	VCC_5V	Power	Supply Voltage 5V
80	VCC_3V3	Power	Supply Voltage3.3V

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX8 SMARC Development Platform technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The i.MX8 SMARC Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the SMARC Carrier Board through Power Jack (J26). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. This connector is physically placed at the top of the board as shown below.

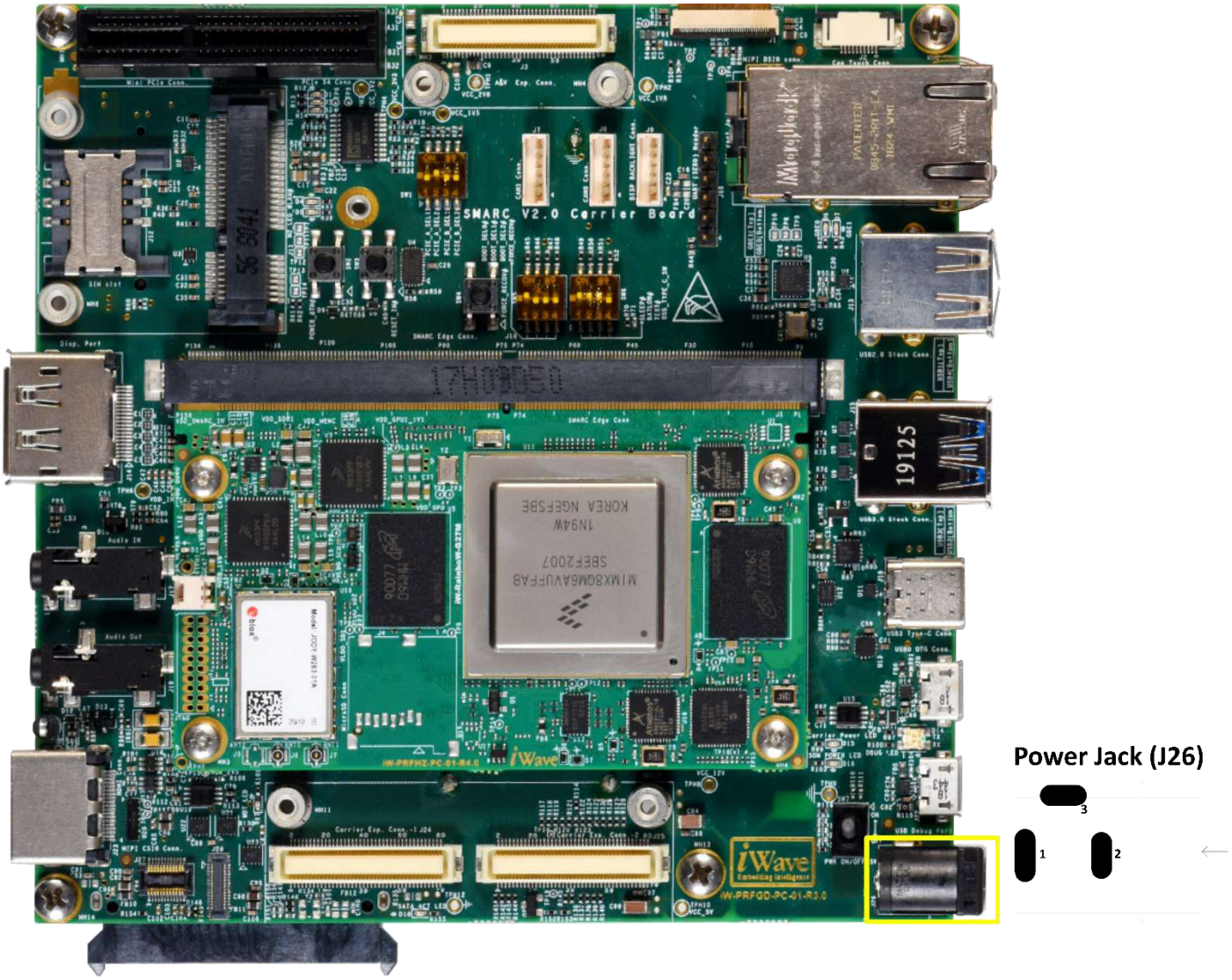


Figure 25: Power Jack

Table 18: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20mV

[1] SMARC Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

[2] This voltage is from Coin cell holder and used as backup power source to RTC circuit of i.MX8 SMARC SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

3.2 Power Output Specification

The i.MX8 SMARC Carrier Board has dedicated power regulator to provide +5V power to SMARC SOM for VIN power supply. Also +3V RTC power from coin cell holder is provided to SMARC SOM for Real time clock support.

The i.MX8 SMARC carrier board also shares different on-board power to Audio & Video connector and Carrier Expansion connector2 for its Add-On Module power.

Table 19: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to SMARC SOM (through SMARC MXM connector)					
1	VIN_5V	4.85V	5V	5.15V	5000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Audio & Video Connector)					
1	VCC_12V	11.75V	12V	12.25V	500mA
2	VCC_5V	4.85V	5V	5.15V	1000mA
3	VCC_3V3	3.15	3.3	3.45	1500mA
4	VCC_2V8	2.5	2.55	2.6	500mA
5	VCC_1V8	1.7	1.8	1.9	500mA
6	VCC_1V5	1.35	1.5	1.65	500mA
7	VCC_1V2	1.1	1.2	1.3	500mA
Power to Add-On Module (through Expansion Connector2)					
1	VCC_5V	4.85V	5V	5.15V	1500mA
2	VCC_3V3	3.15	3.3	3.45	1500mA
3	VCC_1V8	1.7	1.8	1.9	500mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX8 SMARC Development Platform.

Table 20: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	60°C

[1] *iWave guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's i.MX8 SMARC Development Platform is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's i.MX8 SMARC Development Platform is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the Development Platform except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX8 SMARC Carrier Board Mechanical Dimensions

i.MX8 SMARC Development Platform PCB size is 120 mm x 120 mm x 1.6mm. SMARC carrier card mechanical dimensions is shown below. (All dimensions are shown in mm)

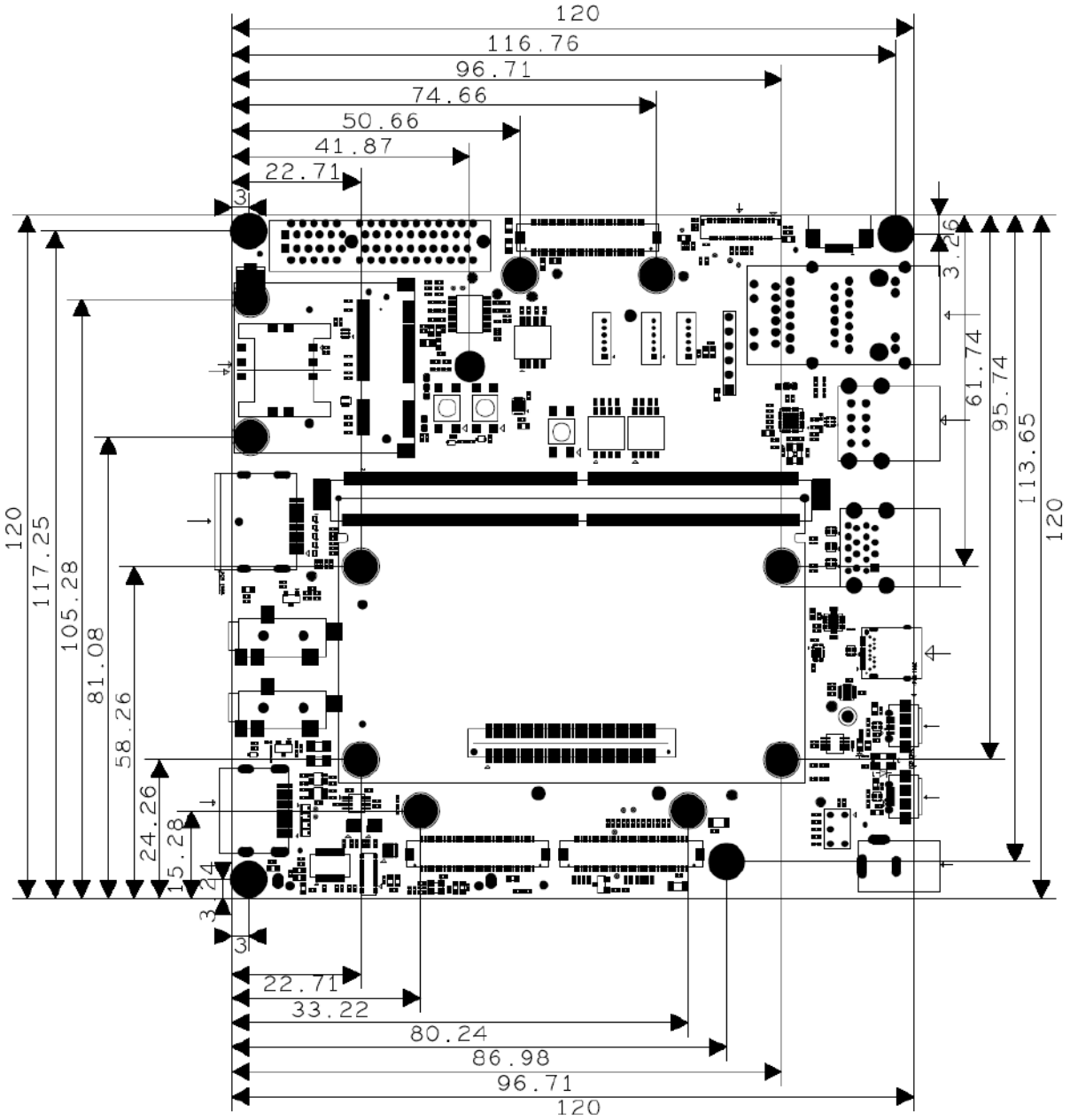


Figure 26: Mechanical dimensions of i.MX8 SMARC Carrier Board- Top View

i.MX8 SMARC Development Platform PCB thickness is 1.6mm±0.16mm, top side maximum height component is connector dual Ethernet Jack J6 (29.34mm) followed by USB3.0 Stack slot J15(15.6mm) and bottom side maximum height component is inductor (7mm). Please refer the below figure which gives height details of the i.MX8 SMARC Development kit.

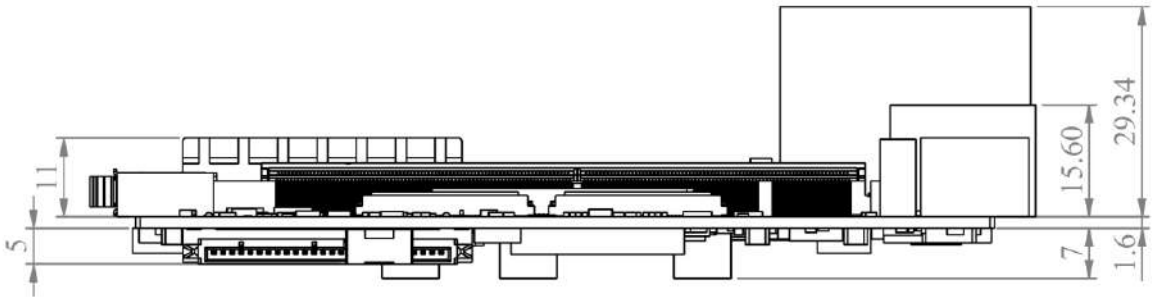


Figure 27: Mechanical dimensions of i.MX8 SMARC Carrier Board - Side View

3.4.2 Guidelines to insert the SMARC SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the SMARC module in to the MXM connector at an angle of 30° as shown in below image.
- Check the Notch position of SMARC module is proper while inserting.
- Once the SMARC module is inserted to the MXM connector properly, press the board vertically down as shown below, such that the board is fixed firmly into the expansion connectors and fix the board by screwing.

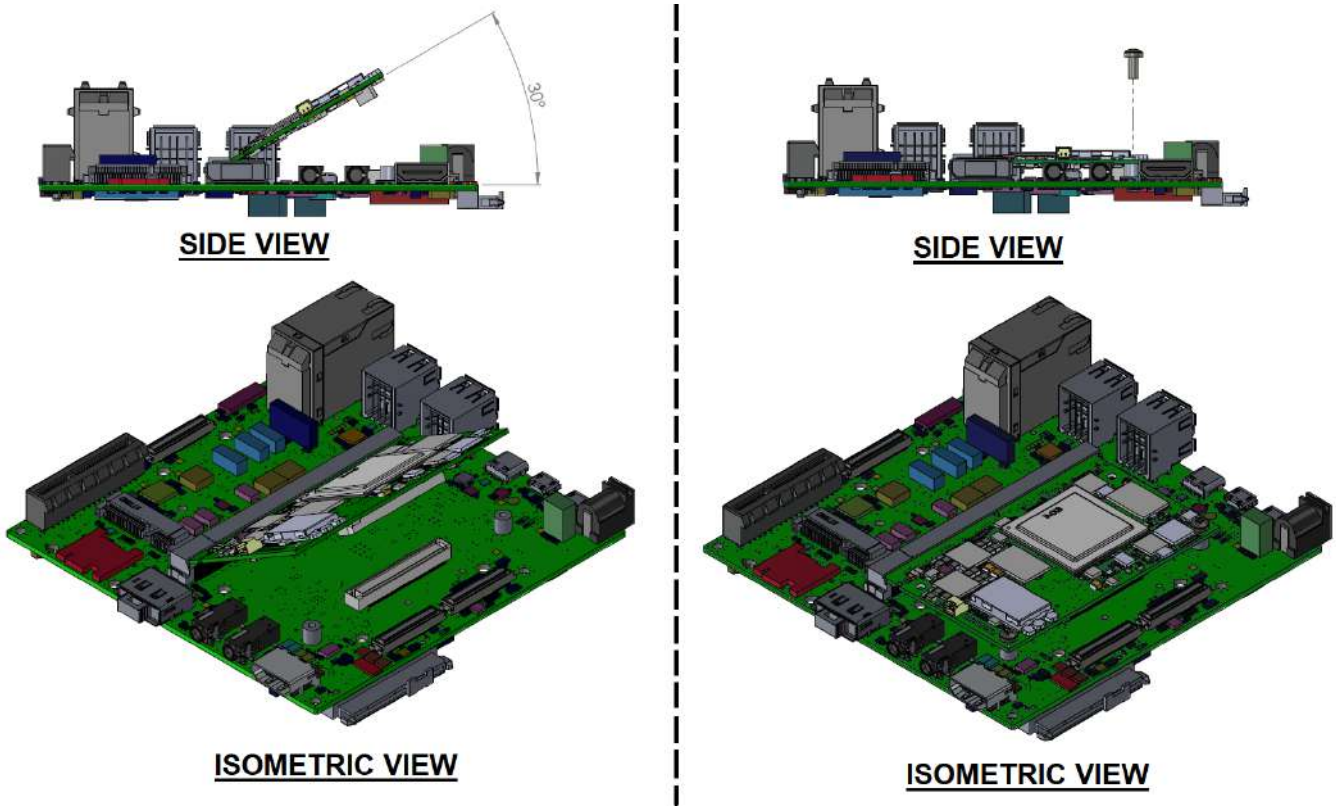


Figure 28: SOM Insertion Guideline

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX8 QM/QP SMARC Development Platform which includes i.MX8 QM/QP SMARC SOM and SMARC carrier board.

Table 21: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G27D-SCQM-4L004G-E016G-LCC	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Linux Kit with LCD display	0°C to 60°C
iW-G27D-SCQM-4L004G-E016G-LCD	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Linux Kit without LCD display	0°C to 70°C
iW-G27D-SCQM-4L004G-E016G-ACC	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Android Kit with LCD display	0°C to 60°C
iW-G27D-SCQM-4L004G-E016G-ACD	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Android Kit without LCD display	0°C to 70°C
iW-G27D-SCQM-4L008G-E032G-LCC	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Linux Kit with LCD display	0°C to 60°C
iW-G27D-SCQM-4L008G-E032G-LCD	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Linux Kit without LCD display	0°C to 70°C
iW-G27D-SCQM-4L008G-E032G-ACC	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Android Kit with LCD display	0°C to 60°C
iW-G27D-SCQM-4L008G-E032G-ACD	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Android Kit without LCD display	0°C to 70°C
iW-G27D-SCQM-4L004G-E016G-LCC	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Linux Kit with LCD display	0°C to 60°C
iW-G27D-SCQM-4L004G-E016G-LCD	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Linux Kit without LCD display	0°C to 70°C
iW-G27D-SCQM-4L004G-E016G-ACC	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Android Kit with LCD display	0°C to 60°C
iW-G27D-SCQM-4L004G-E016G-ACD	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Android Kit without LCD display	0°C to 70°C

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.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